LatticeECP2/M Product Family Qualification Summary

Lattice Document # 25 – 106475 July 2009

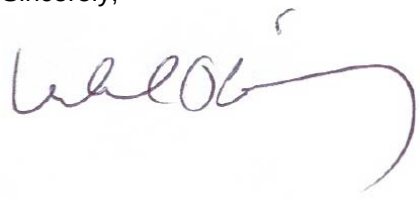
Dear Customer,

Welcome to the Lattice Semiconductor Corp. LatticeECP2/M Product Family Qualification Report. This report reflects our continued commitment to product quality and reliability. The information in this report is drawn from an extensive qualification program of the wafer technology and packaging assembly processes used to manufacture our products. The program adheres to JEDEC and Automotive Industry standards for qualification of the technology and device packaging. This program ensures you only receive product that meets the most demanding requirements for Quality and Reliability.

This report is another member of a new generation of Product Qualification Summary Reports. The information contained in this document is extensive, and represents the entire qualification effort for this device family. Our goal is to provide this information to support your decision making process, and to facilitate the selection and use of our products.

As always, your feedback is valuable to Lattice. Our goal is to continuously improve our systems, including the generation of this report and the data included. Please feel free to forward your comments and suggestions to your local Lattice representative. We will use that feedback carefully and wisely in our effort to maximize customer satisfaction.

Sincerely,



Michael J. Gariepy

VP – Reliability and Quality Assurance
Lattice Semiconductor Corp.
July 17, 2009

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1.0 INTRODUCTION

The Lattice Semiconductor 90 nm product qualification efforts are for the LatticeECP2 and LatticeECP2M FPGA families, built on the Fujitsu baseline 90 nm SRAM process technology. These families redefine the low-cost FPGA category, with high performance DSP blocks, up to 95K LUT capacity, support for DDR2 memory interfaces at 533Mbps, generic LVDS performance up to 840Mbps and high speed SERDES (LatticeECP2M only). By integrating features and capabilities previously only available on higher cost / high performance FPGAs, these families expand the range of applications that can take advantage of low cost FPGAs. These features were achieved through advances in device architecture and the use of 90 nm technology.

The LatticeECP2/M devices are implemented on a cost-effective, production-proven, Low-k, 90 nm CMOS process with copper metallization fabricated by Fujitsu Limited. This process technology, combined with efficient silicon design, results in very small die sizes while providing the new Lattice FPGAs with the most attractive feature set in their class. This report details the reliability qualification results of the LatticeECP2/M product families.

The key parameters for the LatticeECP2 and LatticeECP2M families are show in tables 1.1 and 1.2 respectively.

Table 1.1 LatticeECP2 (Including "S-Series") Product Family Attributes

Product / Attributes	**ECP2-6**	**ECP2-12**	**ECP2-20**	**ECP2-35**	**ECP2-50**	**ECP2-70**
LUTs (K)	6	12	21	32	48	68
Dist RAM (Kbits)	12	24	42	64	96	136
EBR SRAM (Kbits)	55	221	276	332	387	1032
EBR SRAM Blocks	3	12	15	18	21	60
sysDSP Blocks	3	6	7	8	18	22
18x18 Multipliers	12	24	28	32	72	88
GPLL + SPLL + DLL	2+0+2	2+0+2	2+0+2	2+0+2	2+2+2	2+4+2
Maximum Available I/O	190	297	402	450	500	583
Core Voltage	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V
Die Fabrication Site	Fujitsu - Mie	Fujitsu - Mie	Fujitsu - Mie	Fujitsu - Mie	Fujitsu - Mie	Fujitsu - Mie
Process Technology	90 nm CMOS	90 nm CMOS	90 nm CMOS	90 nm CMOS	90 nm CMOS	90 nm CMOS
Die Metallization	Cu	Cu	Cu	Cu	Cu	Cu
Die Interconnect Dielectric	SOG/SiO/SiN	SOG/SiO/SiN	SOG/SiO/SiN	SOG/SiO/SiN	SOG/SiO/SiN	SOG/SiO/SiN
Packages	**Available I/O**					
144-pin TQFP (20x20 mm)	90	93				
208-pin PQFP (28x28 mm)		131	131			
256-ball ftBGA (17x17 mm)	190	193	193			
484-ball fpBGA (23x23 mm)		297	331	331	339	
672-ball fpBGA (27x27 mm)			402	450	500	500
900-ball fpBGA (31x31 mm)						583

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Table 1.2 LatticeECP2M (Including "S-Series") Product Family Attributes

Product / Attributes	ECP2M20	ECP2M35	ECP2M50	ECP2M70	ECP2M100
LUTs (K)	19	34	48	67	95
sysMEM Blocks (18kb)	66	114	225	246	288
Embedded Memory (Kbits)	1217	2101	4147	4534	5308
Distributed Memory (Kbits)	41	71	101	145	202
sysDSP Blocks	6	8	22	24	42
18x18 Multipliers	24	32	88	96	168
GPLL + SPLL + DLL	2+6+2	2+6+2	2+6+2	2+6+2	2+6+2
Maximum Available I/O	304	410	410	436	520
Core Voltage	1.2V	1.2V	1.2V	1.2V	1.2V
Die Fabrication Site	Fujitsu - Mie	Fujitsu - Mie	Fujitsu - Mie	Fujitsu - Mie	Fujitsu - Mie
Process Technology	90 nm CMOS	90 nm CMOS	90 nm CMOS	90 nm CMOS	90 nm CMOS
Die Metallization	Cu	Cu	Cu	Cu	Cu
Die Interconnect Dielectric	SOG/SiO/SiN	SOG/SiO/SiN	SOG/SiO/SiN	SOG/SiO/SiN	SOG/SiO/SiN
Packages	**SERDES I/O Combinations**				
256-ball ftBGA (17x17 mm)	4 / 140	4 / 140			
484-ball fpBGA (23x23 mm)	4 / 304	4 / 303	4 / 270		
672-ball fpBGA (27x27 mm)		4 / 410	8 / 372		
900-ball fpBGA (31x31 mm)			8 / 410	16 / 416	16 / 416
1152-ball fpBGA (35x35 mm)				16 / 436	16 / 520

The LatticeECP2/M FPGA fabric is optimized with high performance and low cost in mind. The LatticeECP2/M devices include LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP blocks and advanced configuration support, including encryption ("S" versions only) and dual boot capabilities.

The LatticeECP2M device family features high speed SERDES with PCS. These high jitter tolerance and low transmission jitter SERDES with PCS blocks can be configured to support an array of popular data protocols including PCI Express, Ethernet (1GbE and SGMII), OBSAI and CPRI. Transmit Pre-emphasis and Receive Equalization settings make SERDES suitable for chip to chip and small form factor backplane applications.

The LatticeECP2/M FPGA products are fabricated on 90nm (SRAM) Fujitsu, Mie process technology and assembled at Advance Semiconductor Engineering, Malaysia (ASEM) and United Test and Assembly Center (UTAC) Singapore.

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2.0 LATTICE PRODUCT QUALIFICATION PROGRAM

Lattice Semiconductor Corp. maintains a comprehensive reliability qualification program to assure that each product achieves its reliability goals. After initial qualification, the continued high reliability of Lattice products is assured through ongoing monitor programs as described in Lattice Semiconductor's Reliability Monitor Program Procedure (Doc. #70-101667). All product qualification plans are generated in conformance with Lattice Semiconductor's Qualification Procedure (Doc. #70-100164) with failure analysis performed in conformance with Lattice Semiconductor's Failure Analysis Procedure (Doc. #70-100166). Both documents are referenced in Lattice Semiconductor's Quality Assurance Manual, which can be obtained upon request from a Lattice Semiconductor sales office. Figure 2.1 shows the Product Qualification Process Flow.

If failures occur during qualification, an 8 Discipline (8D) process is used to find root cause and eliminate the failure mode from the design, materials, or process. The effectiveness of any fix or change is validated through additional testing as required. Final testing results are reported in the qualification reports.

Failure rates in this reliability report are expressed in FITs. Due to the very low failure rate of integrated circuits, it is convenient to refer to failures in a population during a period of 10^9 device hours; one failure in 10^9 device hours is defined as one FIT.

Product families are qualified based upon the requirements outlined in Table 2.2. In general, Lattice Semiconductor follows the current Joint Electron Device Engineering Council (JEDEC) and Military Standard testing methods. Lattice automotive products are qualified and characterized to the Automotive Electronics Council (AEC) testing requirements and methods. Product family qualification will include products with a wide range of circuit densities, package types, and package lead counts. Major changes to products, processes, or vendors require additional qualification before implementation.

The LatticeECP2/M family is the second generation FPGA product family and first 90 nm (CS100A) SRAM Technology based product offering. This family is fabricated at Fujitsu, Mie and assembled at Advance Semiconductor Engineering, Malaysia (ASEM) and United Test and Assembly Center (UTAC) Singapore. The Lattice Semiconductor LatticeECP2/M FPGA product family qualification efforts are based on the first LatticeECP2/M devices in the technology family per the Lattice Semiconductor Qualification Procedure, doc#70-100164.

Lattice Semiconductor maintains a regular reliability monitor program. The current Lattice Reliability Monitor Report can be found at www.latticesemi.com/lit/docs/qa/product_reliability_monitor.pdf .

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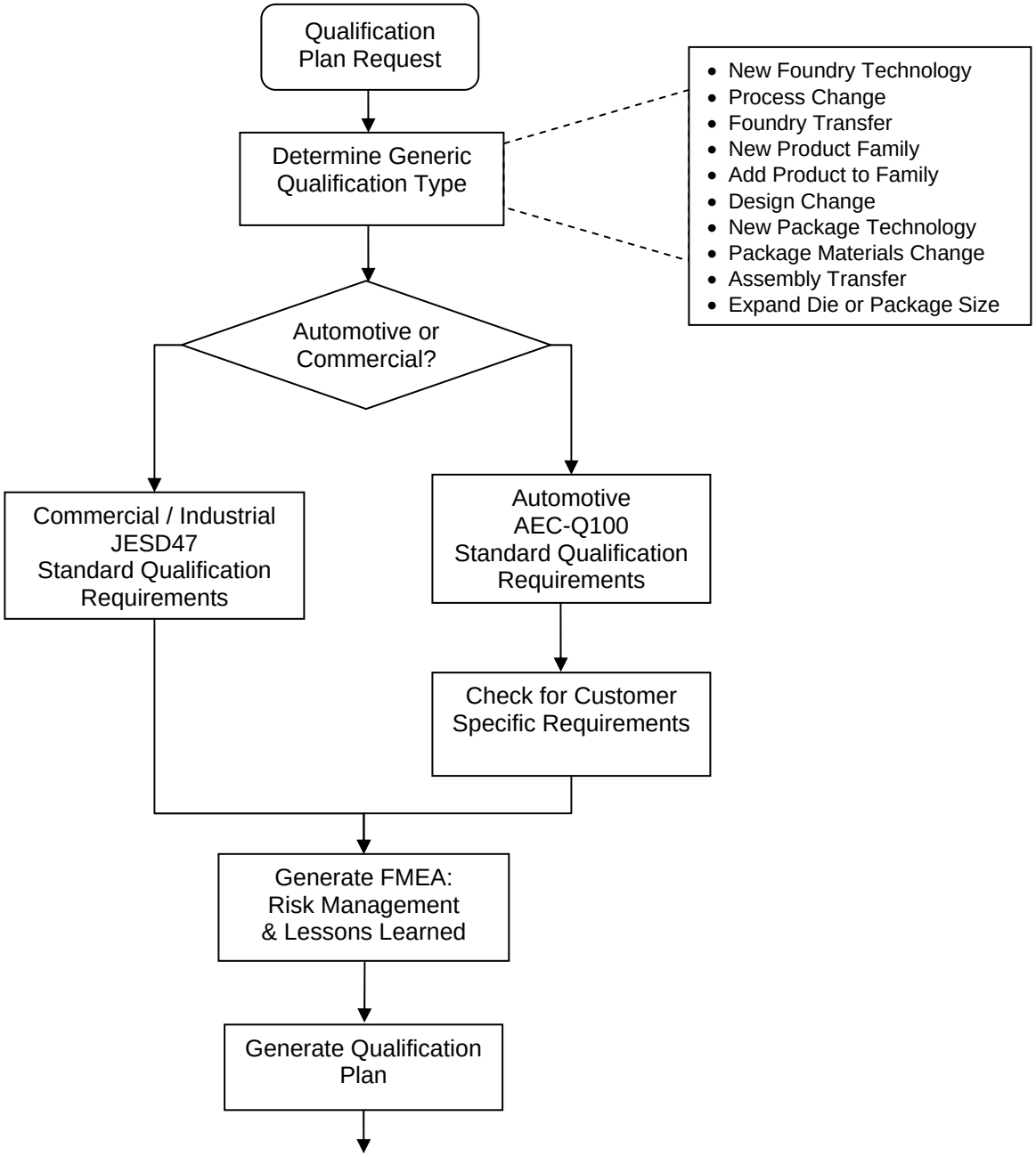
Figure 2.1: LatticeECP2/M Product Qualification Process Flow



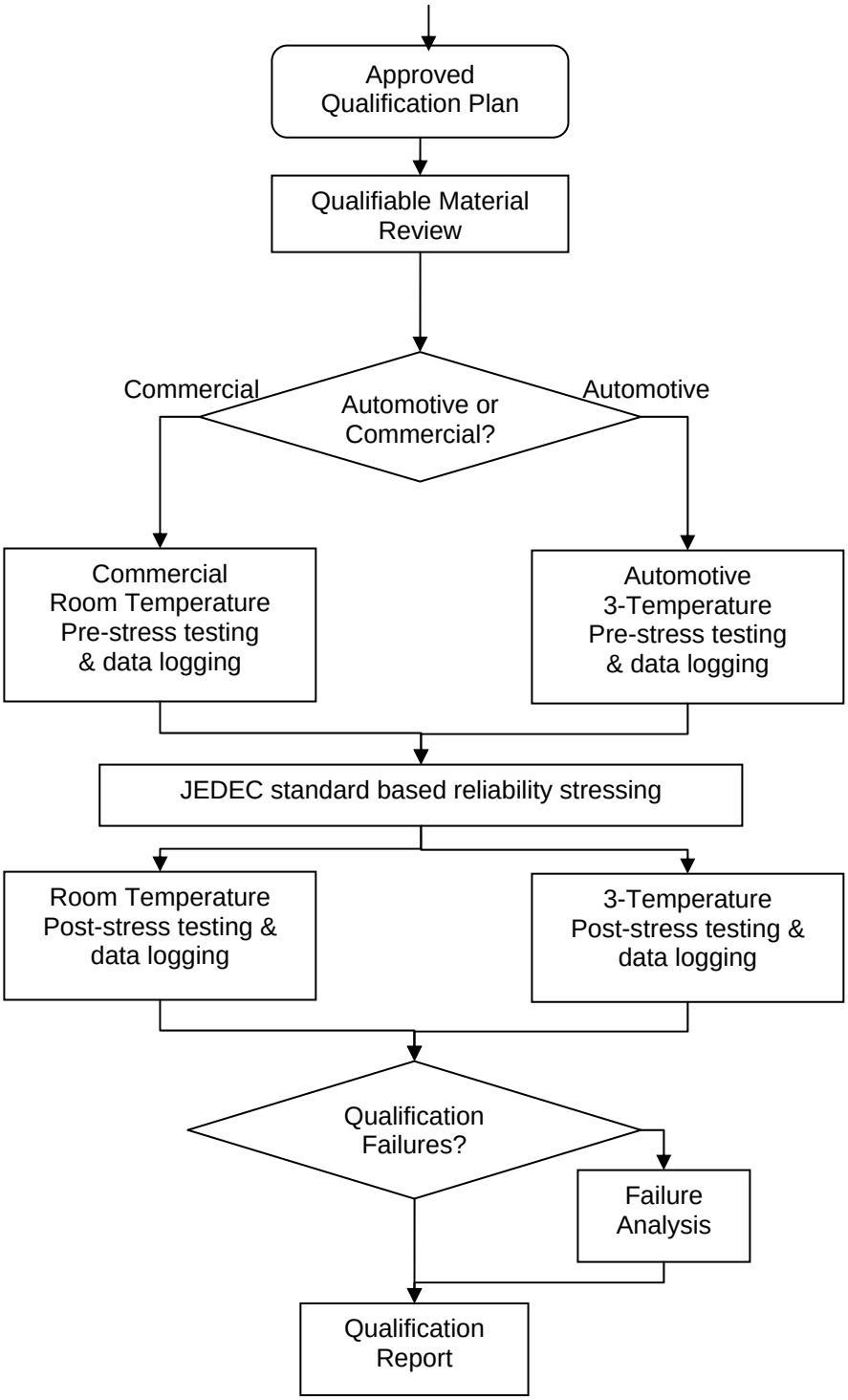


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Table 2.2: Standard Qualification Testing

TEST	STANDARD	TEST CONDITIONS	SAMPLE SIZE (Typ)	PERFORMED ON
High Temperature Operating Life HTOL	Lattice Procedure # 87-101943, MIL-STD-883, Method 1005.8, JESD22-A108C LatticeECP2/M	125° C, Maximum operating Vcc, 168, 500, 1000, 2000 hrs.	77/lot 2-3 lots	Design, Foundry Process, Package Qualification
High Temp Storage Life HTSL	Lattice Procedure # 87-101925, JESD22-A103C LatticeECP2/M	150° C, at 168, 500, 1000, 2000 hours.	77/lot 2-3 lots	Design, Foundry Process, Package Qualification
ESD HBM	Lattice Procedure # 70-100844, MIL-STD-883, Method 3015.7 JESD22-A114E	Human Body Model	3 parts/lot 1-3 lots typical	Design, Foundry Process
ESD CDM	Lattice Procedure # 70-100844, JESD22-C101D	Charged Device model	3 parts/lot 1-3 lots typical	Design, Foundry Process
Latch Up Resistance LU	Lattice Procedure # 70-101570, JESD78A	±100 ma on I/O's, Vcc +50% on Power Supplies. (Max operating temp.)	6 parts/lot 1-3 lots typical	Design, Foundry Process
Surface Mount Pre-conditioning SMPC	Lattice Procedure # 70-103467, IPC/JEDEC J-STD-020D.1 JESD-A113F FPGA - MSL 3	10 Temp cycles, 24 hr 125° C Bake 192hr. 30/60 Soak 3 SMT simulation cycles	All units going into Temp Cycling, UHAST, BHAST, 85/85	Plastic Packages only
Temperature Cycling TC	Lattice Procedure #70-101568, MIL-STD- 883, Method 1010, Condition B JESD22-A104C	(1000 cycles) Repeatedly cycled between -55° C and +125° C in an air environment	45 parts/lot 2-3 lots	Design, Foundry Process, Package Qualification
Unbiased HAST UHAST	Lattice Procedure # 70-104285 JESD22-A118	2 atm. Pressure, 96 hrs, 130 C, 85% Relative Humidity	45 parts/lot 2-3 lots	Foundry Process, Package Qualification Plastic Packages only
Moisture Resistance Temperature Humidity Bias 85/85 THBS or Biased HAST BHAST	Lattice Procedure # 70-101571, JESD22-A101B JESD22-A110B	Biased to maximum operating Vcc, 85° C, 85% Relative Humidity, 1000 hours or Biased to maximum operating Vcc, 2atm. Pressure, 96 hrs, 130 C, 85% Relative Humidity	45 devices/lot 2-3 lots	Design, Foundry Process, Package Qualification Plastic Packages only
Physical Dimensions	Lattice Procedure # 70-100211, MIL-STD- 883 Method 2016 or applicable LSC case outline drawings	Measure all dimensions listed on the case outline.	5 devices	Package Qualification

TEST	STANDARD	TEST CONDITIONS	SAMPLE SIZE (Typ)	PERFORMED ON
Ball Shear	Lattice Procedure # 70-104056 # 70-100433	Per Package Type	3 devices per package / 30 balls each unit	Package Qualification

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3.0 QUALIFICATION DATA FOR 90nm (CS100A) PROCESS TECHNOLOGY

The LatticeECP2/M devices are implemented on a cost-effective, production-proven, Low-k, 90 nm (a.k.a CS100A) CMOS process with copper metallization fabricated by Fujitsu Limited. This process technology, combined with efficient silicon design, results in very small die sizes while providing the new Lattice FPGAs with the most attractive feature sets in their class. This report details the reliability qualification results of the initial LatticeECP2/M Product Families introduction.

Product Family: ECP2/M
Packages offered: TQFP, PQFP, ftBGA, fpBGA
Process Technology Node: 90 nm (CS100A)

3.1 CS100A Process Technology Life Data

High Temperature Operating Life (HTOL) Test

The High Temperature Operating Life test is used to thermally accelerate those wear out and failure mechanisms that would occur as a result of operating the device continuously in a system application. Consistent with JEDEC JESD22-A108 "Temperature, Bias, and Operating Life", a pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at V_{CC} 1.14 V/ V_{CCIO25} 2.63 V /V_{CCIO33} 3.47 V and 105°C ambient or V_{CC} 1.26 V/ V_{CCIO25} 2.63 V /V_{CCIO33} 3.47 V and 105°C ambient.

ECP2/M Life Test (HTOL) Conditions:
Stress Duration: 168, 500, 1000, 2000 hours.
Stress Conditions ECP2/M (LFE2): V_{CC}=1.26V/ V_{CCIO}=3.47, $T_{AMBIENT}$ = 105°C
Method: Lattice Document # 87-101943 and JESD22-A108

Table 3.1.1: ECP2/M Product Family Life Results

Product Name	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	Cumulative Hours
LFE2-50SE	Lot #1	68	0	0	0	68000
LFE2-50SE	Lot #3	72	0	0	0	72000
LFE2-50SE	Lot #4	46	0	0	0	46000
LFE2-50SE	Lot #5	22	0	0	0	22000
LFE2-50SE	Lot #6	58	0	0		29000
LFE2-50SE	Lot#7	17	0	0	0	17000
LFE2-50SE	Lot #8	44	0	0	0	44000
LFE2-50SE	Lot #9	74	0	0	0	74000
LFE2-50SE	Lot #17	77	0	0	0	77000
LFE2-50SE	Lot #18	77	0	0	0	77000
LFE2-50SE	Lot#20	77	0	0	0	77000
LFE2-12SE	Lot#1	81	0	0	0	81000
LFE2-12SE	Lot#2	82	0	0	0	82000
LFE2M35SE	Lot#2	46	0	0	0	46000
LFE2M35SE	Lot#3	55	0	0	0	55000
LFE2M35SE	Lot#6	77	0	0	0	77000

ECP2/M Cumulative Device Hours = 944,000
ECP2/M Cumulative Sample Size = 0 / 973
ECP2/M FIT Rate = 37 FIT

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Low Temperature Operating Life (LTOL) Test

The Low Temperature Operating Life test is used to accelerate transistor performance degradation due to hot electron effects. A pattern specifically designed to exercise the maximum amount of circuitry is programmed into the device and this pattern is continuously exercised at V_{CC} 1.26 V/ V_{CCIO} 3.6 V and -40°C.

ECP2/M Life Test (LTOL) Conditions:

Stress Duration: 168, 500, 1000, 2000 hours.
Stress Conditions ECP2/M (LFE2): V_{CC}=1.26V/ V_{CCIO}=3.47, $T_{AMBIENT}$ = -40°C
Method: Lattice Document # 87-101943 and JESD22-A108

Product Name	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	Cumulative Hours
LFE2-50SE	Lot #3	22	0	0	0	68000

ECP2/M Cumulative Device Hours = 22,000
ECP2/M Cumulative Sample Size = 0 / 22

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3.2 ECP2/M Product Family High Temperature Storage Life (HTSL) Data

High Temperature Storage Life (HTSL)

The High Temperature Storage Life test is used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms. Consistent with JEDEC JESD22-A103C, the devices are subjected to high temperature storage Condition B: +150 (-0/+10) °C for 1000 hours.

ECP2/M High Temperature Storage Life (HTSL) Conditions:
Stress Duration: 168, 500, 1000 hours.
Temperature: 150°C (ambient)
Method: Lattice Document # 87-101925 and JESD22-A103

Table 3.2.1: ECP2/M High Temperature Storage Life (HTSL) Results

Product Name	Package	Assembler	Lot #	Qty	168 Hrs Result	500 Hrs Result	1000 Hrs Result	Cumulative Hours
LFE2-12SE	208 PQFP	ASEM	Lot #7	47	0	0	0	47000
LFE2-12SE	208 PQFP	ASEM	Lot #8	47	0	0	0	47000
LFE2-12SE	208 PQFP	ASEM	Lot #9	46	0	0	0	46000
LFE2-50SE	900 fpBGA	ASEM	Lot #3	30	0	0	0	30000
LFE2-50SE	900 fpBGA	ASEM	Lot #10	48	0	0	0	48000
LFE2-50SE	900 fpBGA	ASEM	Lot#11	48	0	0	0	48000
LFE2-50SE	900 fpBGA	ASEM	Lot#12	45	0	0	0	45000
LFE2-50SE	900 fpBGA	ASEM	Lot#18	45	0	0	0	45000
LFE2-50SE	900 fpBGA	ASEM	Lot#19	45	0	0	0	45000
LFE2-50SE	900 fpBGA	ASEM	Lot#20	45	0	0	0	45000
LFE2M35SE	672 fpBGA	ASEM	Lot#1	60	0	0	0	60000
LFE2M35SE	672 fpBGA	ASEM	Lot#4	45	0	0	0	45000
LFE2M70SE	900 fpBGA	ASEM	Lot#1	25	0	0	0	25000
LFE2M70SE	900 fpBGA	ASEM	Lot#2	24	0	0	0	24000
LFXP2-5E	144 TQFP	UTAC	Lot #1	77			0	77000
LFXP2-5E	144 TQFP	UTAC	Lot #2	77			0	77000
LFXP2-5E	144 TQFP	UTAC	Lot #3	77			0	77000
LAXP2-8E	256 ftbGA	UTAC	Lot #1	77			0	77000
LAXP2-8E	256 ftbGA	UTAC	Lot #2	77			0	77000
LAXP2-8E	256 ftbGA	UTAC	Lot #3	77			0	77000

ECP2/M Cumulative HTSL Failure Rate = 0 / 1,062
ECP2/M Cumulative HTSL Device Hours = 1,062,000

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3.3 ECP2/M Product Family – ESD and Latch UP Data

Electrostatic Discharge-Human Body Model:

ECP2/M product family was tested per the JESD22-A114 Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM) procedure and Lattice Procedure # 70-100844.
All units were tested at 25^0C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.3.1 ECP2 ESD-HBM Data

Product / Package	144-TQFP	208-PQFP	256-fpBGA	484-fpBGA	672-fpBGA	900-fpBGA
ECP2-70						>1000V Class 1C
ECP2-50				>1000V Class 1C	>1000V Class 1C	
ECP2-35				>1000V Class 1C	>1000V Class 1C	
ECP2-20		>1000V Class 1C	>1000V Class 1C	>1000V Class 1C	>1000V Class 1C	
ECP2-12	>1000V Class 1C	>1000V Class 1C	>1000V Class 1C	>1000V Class 1C		
ECP2-6	>1000V Class 1C		>1000V Class 1C			

Table 3.3.2 ECP2M ESD-HBM Data

Product / Package	256-fpBGA	484-fpBGA	672-fpBGA	900-fpBGA	1152-fpBGA
ECP2M-100				>1000V Class 1C	>1000V Class 1C
ECP2M-70				>1000V Class 1C	>1000V Class 1C
ECP2M-50		>1000V Class 1C	>1000V Class 1C	>1000V Class 1C	
ECP2M-35	>1000V Class 1C	>1000V Class 1C	>1000V Class 1C		
ECP2M-20	>1000V Class 1C	>1000V Class 1C			

HBM classification for Commercial/Industrial products, per JESD22-A114
** HBM is worst case on smallest packages and smaller power rails.
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Electrostatic Discharge-Charged Device Model:

ECP2/M product family was tested per the JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components procedure and Lattice Procedure # 70-100844.

All units were tested at 25^0C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.3.3 ECP2 ESD-CDM Data

Product / Package	144-TQFP	208-PQFP	256-fpBGA	484-fpBGA	672-fpBGA	900-fpBGA
ECP2-70						>500V Class III
ECP2-50				>500V Class III	>500V Class III	
ECP2-35				>500V Class III	>500V Class III	
ECP2-20		>500V Class III	>500V Class III	>500V Class III	>500V Class III	
ECP2-12	>500V Class III	>500V Class III	>500V Class III	>500V Class III		
ECP2-6	>500V Class III		>500V Class III			

Table 3.3.4 ECP2M ESD-CDM Data

Product / Package	256-fpBGA	484-fpBGA	672-fpBGA	900-fpBGA	1152-fpBGA
ECP2M-100				>500V Class III	>500V Class III
ECP2M-70				>500V Class III	>500V Class III
ECP2M-50		>500V Class III	>500V Class III	>500V Class III	
ECP2M-35	>500V Class III	>500V Class III	>500V Class III		
ECP2M-20	>500V Class III	>500V Class III			

CDM classification for Commercial/Industrial products, per JESD22-C101
** CDM performance is worst case on the larger package.

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Latch-Up:

ECP2/M product family was tested per the JEDEC EIA/JESD78A IC Latch-up Test procedure and Lattice Procedure # 70-101570.

All units were tested at 25^0C prior to reliability stress and after reliability stress. No failures were observed within the passing classification.

Table 3.3.5 ECP2 I/O Latch Up >100mA

Product / Package	144-TQFP	208-PQFP	256-fpBGA	484-fpBGA	672-fpBGA	900-fpBGA
ECP2-70						>100mA Class II, Level A
ECP2-50				>100mA Class II, Level A	>100mA Class II, Level A	
ECP2-35				>100mA Class II, Level A	>100mA Class II, Level A	
ECP2-20		>100mA Class II, Level A	>100mA Class II, Level A	>100mA Class II, Level A	>100mA Class II, Level A	
ECP2-12	>100mA Class II, Level A	>100mA Class II, Level A	>100mA Class II, Level A	>100mA Class II, Level A		
ECP2-6	>100mA Class II, Level A		>100mA Class II, Level A			

Table 3.3.6 ECP2M I/O Latch Up >100mA

Product / Package	256-fpBGA	484-fpBGA	672-fpBGA	900-fpBGA	1152-fpBGA
ECP2M-100				>100mA Class II, Level A	>100mA Class II, Level A
ECP2M-70				>100mA Class II, Level A	>100mA Class II, Level A
ECP2M-50		>100mA Class II, Level A	>100mA Class II, Level A	>100mA Class II, Level A	
ECP2M-35	>100mA Class II, Level A	>100mA Class II, Level A	>100mA Class II, Level A		
ECP2M-20	>100mA Class II, Level A	>100mA Class II, Level A			

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Table 3.3.7 ECP2 Vcc Latch Up Data

Product / Package	144-TQFP	208-PQFP	256-fpBGA	484-fpBGA	672-fpBGA	900-fpBGA
ECP2-70						1.5xVcc Class II
ECP2-50				1.5xVcc Class II	1.5xVcc Class II	
ECP2-35				1.5xVcc Class II	1.5xVcc Class II	
ECP2-20		1.5xVcc Class II	1.5xVcc Class II	1.5xVcc Class II	1.5xVcc Class II	
ECP2-12	1.5xVcc Class II	1.5xVcc Class II	1.5xVcc Class II	1.5xVcc Class II		
ECP2-6	1.5xVcc Class II		1.5xVcc Class II			

Table 3.3.8 ECP2M Vcc Latch Up Data

Product / Package	256-fpBGA	484-fpBGA	672-fpBGA	900-fpBGA	1152-fpBGA
ECP2M-100				1.5xVcc Class II	1.5xVcc Class II
ECP2M-70				1.5xVcc Class II	1.5xVcc Class II
ECP2M-50		1.5xVcc Class II	1.5xVcc Class II	1.5xVcc Class II	
ECP2M-35	1.5xVcc Class II	1.5xVcc Class II	1.5xVcc Class II		
ECP2M-20	1.5xVcc Class II	1.5xVcc Class II			

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4.0 PACKAGE QUALIFICATION DATA FOR ECP2/M PRODUCT FAMILY

The ECP2/M product family is offered in TQFP, PQFP, ftBGA and fpBGA packages. This report details the package qualification results of the initial LatticeECP2/M product introductions. Package qualification tests including, Temperature Cycling (T/C), Un-biased HAST (UHAST) and Biased HAST (BHAST). Mechanical evaluation tests include Scanning Acoustic Tomography (SAT) and visual package inspection.

The generation and use of generic data is applied across a family of products or packages emanating from one base wafer foundry or assembly process is a Family Qualification, or Qualification by Extension. For the package stresses BHAST and UHAST, these are considered generic for a given Package Technology. T/C is considered generic up to an evaluated die size + package size + 10%, for a given Package Technology. Surface Mount Pre-Conditioning (SMPC) is considered generic up to an evaluated Peak Reflow temperature, for a given Package Technology. The following table demonstrates the package qualification matrix.

Table 4.0 Product-Package Qualification-By-Extension Matrix

Product / Package	Test	ASEM/ UTAC		ASEM				
		144-TQFP	208-PQFP	256-fpBGA	484-fpBGA	672-fpBGA	900-fpBGA	1152-fpBGA
ECP2M-100	SMPC	Packages not offered		Packages not offered			Qual by Extension	MSL3
	T/C							1000 Cyc
	BHAST							By Exten
	UHAST							By Exten
	HTSL							By Exten
ECP2M-70	SMPC	Packages not offered		Packages not offered			MSL3	Qual by Extension
	T/C						1000 Cyc	
	BHAST						By Exten	
	UHAST						By Exten	
	HTSL						By Exten	
ECP2-70	SMPC	Packages not offered		Packages not offered			MSL3	Package not offered
	T/C						1000 Cyc	
	BHAST						By Exten	
	UHAST						By Exten	
	HTSL						1000 Hrs	
ECP2M-50	SMPC	Packages not offered		Package not offered	Qual by Extension	Qual by Extension	Qual by Extension	Package not offered
	T/C							
	BHAST							
	UHAST							
	HTSL							
ECP2-50	SMPC	Packages not offered		Package not offered	Qual by Extension	Qual by Extension	MSL3	Packages not offered
	T/C						1000 Cyc	
	BHAST						96 Hrs	
	UHAST						96 Hrs	
	HTSL						1000 Hrs	
ECP2M-35	SMPC	Packages not offered		Qual by Extension	Qual by Extension	MSL3	Packages not offered	
	T/C					1000 Cyc		
	BHAST					By Exten		
	UHAST					96 Hours		
	HTSL					1000 Hrs		
ECP2-35	SMPC	Packages not offered		Package not	Qual by Extension	Qual by Extension	Packages not offered	
	T/C							

	BHAST			offered			
	UHAST						
	HTSL						
ECP2M-20	SMPC	Packages not offered		Qual by Extension	Qual by Extension	Packages not offered	
	T/C						
	BHAST						
	UHAST						
	HTSL						
ECP2-20	SMPC	Package not offered	MSL3	Qual by Extension	Qual by Extension	Qual by Extension	Packages not offered
	T/C		1000 Cyc				
	BHAST		By Exten				
	UHAST		By Exten				
	HTSL		By Exten				
ECP2-12	SMPC	MSL3	MSL3	Qual by Extension	Qual by Extension	Packages not offered	
	T/C	1000 Cyc	1000 Cyc				
	BHAST	By Exten	96 Hours				
	UHAST	By Exten	96 Hours				
	HTSL	By Exten	1000 Hrs				
ECP2-6	SMPC	Qual by Extension	Package not offered	Qual by Extension	Packages not offered		
	T/C						
	BHAST						
	UHAST						
	HTSL						

Note – Qualified by extension is from the largest die/package combination

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4.1 ECP2/M Product Family Surface Mount Preconditioning Testing

The Surface Mount Preconditioning (SMPC) Test is used to model the surface mount assembly conditions during component solder processing. All devices stressed through Temperature Cycling, Un-biased HAST and Biased HAST were preconditioned. This preconditioning is consistent with JEDEC JESD22-A113 “Preconditioning Procedures of Plastic Surface Mount Devices Prior to Reliability Testing”, Moisture Sensitivity Level 3 (MSL3) package moisture sensitivity and dry-pack storage requirements.

Surface Mount Preconditioning (MSL3)
(10 Temperature Cycles, 24 hours bake @ 125°C, 30°C/60% RH, soak 192 hours, Reflow Simulation, 3 passes) performed before all package tests.
MSL3 Packages: TQFP, PQFP, fpBGA, ftBGA
Method: Lattice Procedure # 70-103467, J-STD-020D.1 and JESD22-A113F

Table 4.1.1 Surface Mount Precondition Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Reflow Temperature
LFE2-50E	900 fpBGA	ASEM	Lot #1	135	0	250°C
LFE2-50E	900 fpBGA	ASEM	Lot #2	45	0	250°C
LFE2-50E	900 fpBGA	ASEM	Lot #3	90	0	250°C
LFE2-50E	900 fpBGA	ASEM	Lot #4	50	0	250°C
LFE2-50E	900 fpBGA	ASEM	Lot #5	48	0	250°C
LFE2-50E	900 fpBGA	ASEM	Lot #18	131	0	250°C
LFE2-50E	900 fpBGA	ASEM	Lot #19	130	0	250°C
LFE2-50E	900 fpBGA	ASEM	Lot #20	135	0	250°C
LFE2-12E	144 TQFP	ASEM	Lot#1	76	0	260°C
LFE2-12E	144 TQFP	ASEM	Lot#2	77	0	260°C
LFE2-12SE	208 PQFP	ASEM	Lot #7	92	0	250°C
LFE2-12SE	208 PQFP	ASEM	Lot #8	94	0	250°C
LFE2-12SE	208 PQFP	ASEM	Lot #9	94	0	250°C
LFE2-12SE	208 PQFP	ASEM	Lot #7	117	0	245°C
LFE2-12SE	208 PQFP	ASEM	Lot #8	47	0	245°C
LFE2-12SE	208 PQFP	ASEM	Lot #9	47	0	245°C
LFE2-12SE	208 PQFP	ASEM	Lot #10	81	0	245°C
LFE2-12SE	208 PQFP	ASEM	Lot #11	77	0	245°C
LFE2-12E	208 PQFP	ASEM	Lot#1	45	0	245°C
LFE2-12E	208 PQFP	ASEM	Lot#2	45	0	245°C
LFE2-12E	208 PQFP	ASEM	Lot#3	45	0	245°C
LFE2-20E	208 PQFP	ASEM	Lot#6	45	0	245°C
LFE2-20E	208 PQFP	ASEM	Lot#7	45	0	245°C
LFE2M35E	672 fpBGA	ASEM	Lot#1	91	0	250°C
LFE2M35E	672 fpBGA	ASEM	Lot#2	46	0	250°C
LFE2-70E	900 fpBGA	ASEM	Lot#1	78	0	250°C
LFE2-70E	900 fpBGA	ASEM	Lot#2	77	0	250°C
LFE2M70SE	900 fpBGA	ASEM	Lot#1	25	0	250°C
LFE2M70SE	900 fpBGA	ASEM	Lot#2	24	0	250°C
LFE2M100SE	1152 fpBGA	ASEM	Lot#2	33	0	250°C

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Reflow Temperature
LFE2M100SE	1152 fpBGA	ASEM	Lot #3	29	0	250°C
LFE2M100SE	1152 fpBGA	ASEM	Lot #5	44	0	250°C
LFE2M100SE	1152 fpBGA	ASEM	Lot #6	45	0	250°C
LFE2M100SE	1152 fpBGA	ASEM	Lot #7	45	0	250°C
LFXP2-5E	144 TQFP	UTAC	Lot #1	77	0	260°C
LFXP2-5E	144 TQFP	UTAC	Lot #2	77	0	260°C
LFXP2-5E	144 TQFP	UTAC	Lot #3	77	0	260°C
LFE2-12E	144 TQFP	UTAC	Lot #4	77	0	260°C
LFE2-12E	144 TQFP	UTAC	Lot #5	77	0	260°C
LFE2-12E	144 TQFP	UTAC	Lot #6	77	0	260°C
LFXP2-8E	256 ftBGA	UTAC	Lot #1	77	0	260°C
LFXP2-8E	256 ftBGA	UTAC	Lot #2	77	0	260°C
LFXP2-8E	256 ftBGA	UTAC	Lot #3	77	0	260°C
LFXP2-8E	132 csBGA	UTAC	Lot #1	77	0	260°C
LFXP2-8E	132 csBGA	UTAC	Lot #2	77	0	260°C
LFXP2-8E	132 csBGA	UTAC	Lot #3	77	0	260°C
LFE2M35SE	256 ftBGA	UTAC	Lot #1	77	0	260°C
LFE2M35SE	256 ftBGA	UTAC	Lot #2	77	0	260°C

Cumulative SMPC Failure Rate = 0 / 3,560

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4.2 – ECP2/M Product Family Temperature Cycling Data

The Temperature Cycling test is used to accelerate those failures resulting from mechanical stresses induced by differential thermal expansion of adjacent films, layers and metallurgical interfaces in the die and package. Devices are tested at 25°C after exposure to repeated cycling between -55°C and +125°C in an air environment consistent with JEDEC JESD22-A104 "Temperature Cycling", Condition B temperature cycling requirements. Prior to Temperature Cycling testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: TQFP, PQFP, ftBGA, fpBGA
Stress Duration: 1000 cycles
Stress Conditions: Temperature cycling between -55°C to 125°C
Method: Lattice Procedure # 70-101568 and JESD22-A104

Table 4.2.1: Temperature Cycling Data

Product Name	Package	Assembly Site	Lot Number	Quantity	250 Cycles	500 Cycles	1000 Cycles
LFE2-50E	900 fpBGA	ASEM	Lot #1	44	0	0	0
LFE2-50E	900 fpBGA	ASEM	Lot #2	45	0	0	0
LFE2-50E	900 fpBGA	ASEM	Lot #18	45	0	0	0
LFE2-50E	900 fpBGA	ASEM	Lot #19	45	0	0	0
LFE2-50E	900 fpBGA	ASEM	Lot #20	45	0	0	0
LFE2M35E	672 fpBGA	ASEM	Lot#1	46	0	0	0
LFE2M35E	672 fpBGA	ASEM	Lot#2	46	0	0	0
LFE2-70E	900 fpBGA	ASEM	Lot#1	78	0	0	0
LFE2-70E	900 fpBGA	ASEM	Lot#2	77	0	0	0
LFE2M70SE	900 fpBGA	ASEM	Lot#1	25	0	0	0
LFE2M70SE	900 fpBGA	ASEM	Lot#2	24	0	0	0
LFE2M100SE	1152 fpBGA	ASEM	Lot#2	33	0	0	0
LFE2M100SE	1152 fpBGA	ASEM	Lot#3	29	0	0	0
LFE2M100SE	1152 fpBGA	ASEM	Lot#5	44	0	0	0
LFE2M100SE	1152 fpBGA	ASEM	Lot#6	45	0	0	0
LFE2M100SE	1152 fpBGA	ASEM	Lot#7	45	0	0	0
LFE2-20E	208 PQFP	ASEM	Lot#6	45	0	0	0
LFE2-20E	208 PQFP	ASEM	Lot#7	45	0	0	0
LFE2-12E	144 TQFP	ASEM	Lot#1	76	0	0	0
LFE2-12E	144 TQFP	ASEM	Lot#1	77	0	0	0
LFE2-12E	144 TQFP	UTAC	Lot #4	77	0	0	0
LFE2-12E	144 TQFP	UTAC	Lot #5	77	0	0	0
LFE2-12E	144 TQFP	UTAC	Lot #6	77	0	0	0
LFE2M35SE	256 ftBGA	UTAC	Lot #1	77	0	0	0
LFE2M35SE	256 ftBGA	UTAC	Lot #2	77	0	0	0

Cumulative Temp Cycle Failure Rate = 0 / 1,498

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4.3 Unbiased HAST Data

Unbiased Highly Accelerated Stress Test (HAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Unbiased HAST test is designed to detect ionic contaminants present within the package or on the die surface, which can cause chemical corrosion. Consistent with JEDEC JESD22-A118, "Accelerated Moisture Resistance - Unbiased HAST," the Unbiased HAST conditions are 96 hour exposure at 130°C, 85% relative humidity, and 2 atmospheres of pressure. Prior to Unbiased HAST testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: TQFP, PQFP, fpBGA
Stress Duration: 96 Hrs
Stress Conditions: 130°C, 15psig, 85% RH
Method: Lattice Procedure # 70-104285 and JESD22-A118

Table 4.3.1: Unbiased HAST Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Stress Duration
LFE2-50E	900 fpBGA	ASEM	Lot #1	45	0	96 Hrs
LFE2-50E	900 fpBGA	ASEM	Lot #2	45	0	96 Hrs
LFE2-50E	900 fpBGA	ASEM	Lot #3	45	0	96 Hrs
LFE2-50E	900 fpBGA	ASEM	Lot #18	45	0	96 Hrs
LFE2-50E	900 fpBGA	ASEM	Lot #19	44	0	96 Hrs
LFE2-50E	900 fpBGA	ASEM	Lot #20	45	0	96 Hrs
LFE2-12SE	208 PQFP	ASEM	Lot #7	46	0	96 Hrs
LFE2-12SE	208 PQFP	ASEM	Lot #8	47	0	96 Hrs
LFE2-12SE	208 PQFP	ASEM	Lot #9	47	0	96 Hrs
LFE2M35E	672 fpBGA	ASEM	Lot#1	45	0	96 Hrs
LFXP2-8E	132 csBGA	UTAC	Lot #1	77	0	96 Hrs
LFXP2-8E	132 csBGA	UTAC	Lot #2	77	0	96 Hrs
LFXP2-8E	132 csBGA	UTAC	Lot #3	77	0	96 Hrs

Cumulative Unbiased HAST failure Rate = 0 / 685

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4.4 THB: Biased HAST Data

Highly Accelerated Stress Test (HAST) testing uses both pressure and temperature to accelerate penetration of moisture into the package and to the die surface. The Biased HAST test is used to accelerate threshold shifts in the MOS device associated with moisture diffusion into the gate oxide region as well as electrochemical corrosion mechanisms within the device package. Consistent with JEDEC JESD22-A110B "Highly-Accelerated Temperature and Humidity Stress Test (HAST)", the biased HAST conditions are with Vcc bias and alternate pin biasing in an ambient of 130°C, 85% relative humidity, and 2 atmospheres of pressure. Prior to Biased HAST testing, all devices are subjected to Surface Mount Preconditioning.

MSL3 Packages: ftBGA, fpBGA
Stress Conditions: Vcc= 1.26V/ V_{CCIO} = 3.3V, 130°C / 85% RH, 15 psig
Stress Duration: 96 hours
Method: Lattice Procedure # 70-101571 and JESD22-A110B

Table 4.4.1: Biased HAST Data

Product Name	Package	Assembly Site	Lot Number	Quantity	# of Fails	Stress Duration
LFE2-50E	900 fpBGA	ASEM	Lot #1	45	0	96 Hrs
LFE2-50E	900 fpBGA	ASEM	Lot #4	40	0	96 Hrs
LFE2-50E	900 fpBGA	ASEM	Lot #5	41	0	96 Hrs
LFE2-50E	900 fpBGA	ASEM	Lot #18	41	0	96 Hrs
LFE2-50E	900 fpBGA	ASEM	Lot #19	41	0	96 Hrs
LFE2-50E	900 fpBGA	ASEM	Lot #20	45	0	96 Hrs
LFE2-12SE	208 PQFP	ASEM	Lot #7	46	0	96 Hrs
LFE2-12SE	208 PQFP	ASEM	Lot #8	47	0	96 Hrs
LFE2-12SE	208 PQFP	ASEM	Lot #9	47	0	96 Hrs
LFE2-12SE	208 PQFP	ASEM	Lot #10	81	0	96 Hrs
LFE2-12SE	208 PQFP	ASEM	Lot #11	77	0	96 Hrs
LFE2-12SE	208 PQFP	ASEM	Lot #7	71	0	96 Hrs
LFE2-12E	208 PQFP	ASEM	Lot#1	45	0	96 Hrs
LFE2-12E	208 PQFP	ASEM	Lot#2	45	0	96 Hrs
LFE2-12E	208 PQFP	ASEM	Lot#3	45	0	96 Hrs
LFXP2-5E	144 TQFP	UTAC	Lot #1	77	0	96 Hrs
LFXP2-5E	144 TQFP	UTAC	Lot #2	77	0	96 Hrs
LFXP2-5E	144 TQFP	UTAC	Lot #3	77	0	96 Hrs
LFXP2-8E	256 ftBGA	UTAC	Lot #1	77	0	96 Hrs
LFXP2-8E	256 ftBGA	UTAC	Lot #2	77	0	96 Hrs
LFXP2-8E	256 ftBGA	UTAC	Lot #3	77	0	96 Hrs

Cumulative BHAST failure Rate = 0 / 1,219

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5.0 ECP2/M Process Reliability Wafer Level Review

Several key fabrication process related parameters have been identified by the foundry that would affect the Reliability of the End-Product. These parameters are tested during the Development Phase of the Technology. Passing data (a 10yr lifetime at the reliability junction temperature) must be obtained for three lots minimum for each parameter before release to production. Normal operating conditions are defined in the Electrical Design Rules (EDR). These parameters are:

Hot Carrier Immunity (**HCI**): Effect is a reduction in transistor Idsat. Worst case is low temperature.
Time Dependent Dielectric Breakdown (**TDDB**): Transistor and capacitor oxide shorts or leakage.
Negative Bias Temperature Instability (**NBTI**): Symptom is a shift in Vth (also a reduction in Idsat).
Electromigration Lifetime (**EML**): Symptom is opens within, or shorts between, metal conductors.
Stress Migration (**SM**): Symptom is a void (open) in a metal Via due to microvoid coalescence.

Table 5.1 – Wafer Level Reliability Results

HCI

Device	LVN	LVP	HVN	HVP
delta Ids	-10%	-10%	-10%	-10%
Celsius	25	25	25	25
Vgstress	Vd	Vd	Vd/2	Vd/2
Vds	1.26	-1.26	3.465	-3.465
TTF	5 lots>27yr	4 lots>840yr	5 lots>20yr	2 lots>22yr

TDDB

Device	LVN	LVP	HVN	HVP	Intermediate IMD
Celsius	125	125	125	125	125
Vg	1.26	-1.26	3.465	-3.465	3.465
Max Area	0.054cm^2	0.13cm^2	0.5cm^2	0.02cm^2	L/S=140nm
0.1% TTF	3 lots>10yr	4 lots>65yr	3 lots>1300yr	3 lots>17yr	6 lots>40yr

NBTI

Device	LVP	HVP
delta Vth	50mv	100mv
Celsius	125	125
Vg	-1.26	-3.465
TTF	3 lots>210yr	3 lots>124yr

EML

Device	Intermediate	Semi-Global	Global	Top Al
Celsius	125	125	125	125
delta R	+5%	+5%	+5%	+5%
Jmax	3e5A/cm^2	3e5A/cm^2	3e5A/cm^2	2.5e5A/cm^2
0.1% TTF	6 lots>14yr	6 lots>16yr	6 lots>24yr	4 lots>14yr

SM

Device	Intermediate	Semi-Global	Global
delta R	+100%	+100%	+100%
Celsius	125	125	125
TTF	6 lots>118yr	6 lots>36yr	6 lots>48yr

Note: Reliability life times are based on listed temperature and used conditions. Detailed WLR test conditions are available upon request.

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6.0 ECP2/M Soft Error Rate Data

Soft Error Rate testing is conducted to characterize the sensitivity of SRAM storage and device logic elements to High Energy Neutron and Alpha Particle radiation. Charge induced by the impact of these particles can collect at sensitive nodes in the device, and result in changes in the internal electrical states of the device. While these changes do not cause physical damage to the device, they can cause a logical error in device operation.

All testing conforms to JEDEC JESD-89.

Table 6.1 ECP2/M SER Results

ECP2/M MEASURED FITs / Mb	CONFIGURATION BITS	EBR BITS
Neutron	99	168
Alpha	173	273

Note: Detailed SER data is available upon request.

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7.0 ECP2/M ADDITIONAL FAMILY DATA

Table 7.1: ECP2/M Package Assembly Data – fpBGA / ftBGA

Package Attributes / Assembly Sites	ASEM
Die Family (Product Line)	ECP2/M
Fabrication Process Technology	90nm CMOS (CS100A)
Package Assembly Site	Malaysia
Package Type	ftbGA / fpBGA
Ball Counts	256/484/672/900/1152
Die Preparation/Singulation	wafer saw, full cut
Die Attach Material	Ablebond 2100 Series
Mold Compound Supplier/ID	Hitachi 9750HF Series
Wire Bond Material	Gold (Au)
Wire Bond Methods	Thermosonic Ball
Substrate Material	Bismaleimide Triazine HL83X Series
Lead Finish Plating or BGA Ball	Sn96.5/Ag3.0/Cu0.5
Marking	Laser

Table 7.2: ECP2/M Package Assembly Data – TQFP/PQFP

Package Attributes / Assembly Sites	ASEM
Die Family (Product Line)	ECP2/M
Fabrication Process Technology	90nm CMOS (CS200A)
Package Assembly Site	Malaysia
Package Type	TQFP / PQFP
Ball Counts	144 / 208
Die Preparation/Singulation	wafer saw, full cut
Die Attach Material	Ablebond 3230
Mold Compound Supplier/ID	Hitachi 9510HF Series
Wire Bond Material	Gold (Au)
Wire Bond Methods	Thermosonic Ball
Lead Frame Material	Cu Alloy
Lead Finish	Matte Sn (annealed)
Marking	Laser

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Lattice Semiconductor Corporation
5555 NE Moore Court
Hillsboro, Oregon 97124 U.S.A.
Telephone: (503) 268-8000, FAX: (503) 268-8556
www.latticesemi.com

www.latticesemi.com