Product Brief
January 2002

ORCA® Series 3C and 3T Field-Programmable Gate Arrays

Features

- High-performance, cost-effective, 0.35 µm and 0.3 µm 4-level metal technology (4- or 5-input look-up table delay of 1.2 ns with -7 speed grade in 0.3 µm).
- Same basic architecture as lower-voltage, advanced process technology Series 3 architecture (see *ORCA* Series 3LxxxB FPGAs documentation).
- Up to 186,000 usable system gates.
- Up to 452 user I/Os. (OR3Txxx I/Os are 5 V tolerant to allow interconnection to both 3.3 V and 5 V devices, selectable on a per-pin basis.)
- Pin-selectable I/O clamping diodes provide 5 V or 3.3 V PCI compliance and 5 V tolerance on OR3Txxx devices.
- Twin-quad programmable function unit (PFU) architecture with eight 16-bit look-up tables (LUTs) per PFU, organized in two nibbles for use in nibble- or byte-wide functions. Allows for mixed arithmetic and logic functions in a single PFU.
- Nine user registers per PFU, one following each LUT, plus one extra. All have programmable clock enable and local set/reset, plus a global set/reset that can be disabled per PFU.
- Flexible input structure (FINS) of the PFUs provides a routability enhancement for LUTs with shared inputs and the logic flexibility of LUTs with independent inputs.
- Fast-carry logic and routing to adjacent PFUs for nibble-, byte-wide, or longer arithmetic functions, with the **new** option to register the PFU carry-out.
- Softwired LUTs (SWL) allow fast cascading of up to three levels of LUT logic in a single PFU for up to 40% speed improvement.
- Supplemental logic and interconnect cell (SLIC) provides 3-statable buffers, up to 10-bit decoder, and *PAL**-like AND-OR-INVERT (AOI) in each programmable logic cell (PLC), with over 50% speed improvement typical.
- Abundant hierarchical routing resources based on routing two data nibbles and two control lines per set provide for faster place and route implementations and less routing delay.
- TTL or CMOS input levels programmable per pin for the OR3Cxxx (5.0 V) devices.
- Individually programmable drive capability: 12 mA sink/6 mA source or 6 mA sink/3 mA source.
- Built-in boundary scan (*IEEE* †1149.1 JTAG) and TS_ALL testability function to 3-state all I/O pins.
- Enhanced system clock routing for low-skew, high-speed clocks originating on-chip or at any I/O.
- Up to four ExpressCLK inputs allow extremely fast clocking of signals on- and off-chip plus access to internal general clock routing.
- StopCLK feature to glitchlessly stop/start the ExpressCLKs independently by user command.
- Programmable I/O (PIO) has:
  - — Fast-capture input latch and input flip-flop (FF)/latch for reduced input setup time and zero hold time.
  - — Capability to (de)multiplex I/O signals.
  - — Fast access to SLIC for decodes and *PAL*-like functions.
  - — Output FF and two-signal function generator to reduce CLK to output propagation delay.
  - — Fast open-drain drive capability.
  - — Capability to register 3-state enable signal.
- Baseline FPGA family used in Series 3+ FPSCs (field-programmable system chips) which combine FPGA logic and standard-cell logic on one device.

* *PAL* is a trademark of Advanced Micro Devices, Inc.
† *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Table 1. *ORCA* Series 3C and 3T FPGAs

Device	System Gates‡	LUTs	Registers	Max User RAM	User I/Os	Array Size	Process Technology
OR3T20	36K	1152	1872	18K	196	12 x 12	0.3 µm/4 LM
OR3T30	48K	1568	2436	25K	228	14 x 14	0.3 µm/4 LM
OR3C/3T55	80K	2592	3780	42K	292	18 x 18	0.3 µm/4 LM
OR3C/3T80	116K	3872	5412	62K	356	22 x 22	0.3 µm/4 LM
OR3T125	186K	6272	8400	100K	452	28 x 28	0.3 µm/4 LM

‡ The system gate counts range from a logic-only gate count to a gate count assuming 30% of the PFUs/SLICs being used as RAMs. The logic-only gate count includes each PFU/SLIC (counted as 108 gates/PFU), including 12 gates per LUT/FF pair (eight per PFU), and 12 gates per SLIC/FF pair (one per PFU). Each of the four PIOs per PIC is counted as 16 gates (three FFs, fast-capture latch, output logic, CLK, and I/O buffers). PFUs used as RAM are counted at four gates per bit, with each PFU capable of implementing a 32 x 4 RAM (or 512 gates) per PFU.

System-Level Features

System-level features reduce glue logic requirements and make a system on a chip possible. These features in the *ORCA* OR3C/Txxx include:

- Full PCI local bus compliance.
- Dual-use microprocessor interface (MPI) can be used for configuration, readback, device control, and device status, as well as for a general-purpose interface to the FPGA. Glueless interface to *i960* * and *PowerPC*† processors with user-configurable address space provided.
- Parallel readback of configuration data capability with the built-in microprocessor interface.
- Programmable clock manager (PCM) adjusts clock phase and duty cycle for input clock rates from 5 MHz to 120 MHz. The PCM may be combined with FPGA logic to create complex functions, such as digital phase-locked loops (DPLL), frequency counters, and frequency synthesizers or clock doublers. Two PCMs are provided per device.
- True, internal, 3-state, bidirectional buses with simple control provided by the SLIC.
- 32 x 4 RAM per PFU, configurable as single- or dual-port at >164 MHz (-7 speed). Create large, fast RAM/ROM blocks (128 x 8 in only eight PFUs) using the SLIC decoders as bank drivers.

* *i960* is a registered trademark of Intel Corporation.
† *PowerPC* is a registered trademark of International Business Machines Corporation.

Table 2. *ORCA* OR3C/Txxx System Performance

Parameter	# PFUs	Speed				Unit
		-4	-5	-6	-7	
16-bit Loadable Up/Down Counter	2	76	99	129	140	MHz
16-bit Accumulator	2	76	99	129	140	MHz
8 x 8 Parallel Multiplier:						
Multiplier Mode, Unpipelined[1]	11.5	19	24	31	33	MHz
ROM Mode, Unpipelined[2]	8	50	65	82	88	MHz
Multiplier Mode, Pipelined[3]	15	74	101	126	135	MHz
32 x 16 RAM (synchronous):						
Single-port, 3-state Bus[4]	4	94	122	153	164	MHz
Dual-port[5]	4	122	158	200	214	MHz
128 x 8 RAM (synchronous):						
Single-port, 3-state Bus[4]	8	86	112	140	150	MHz
Dual-port[5]	8	86	112	140	150	MHz
8-bit Address Decode (internal):						
Using Softwired LUTs	0.25	4.87	3.66	2.58	2.37	ns
Using SLICs[6]	0	2.35	1.85	1.27	1.17	ns
32-bit Address Decode (internal):						
Using Softwired LUTs	2	16.06	12.07	8.87	8.19	ns
Using SLICs[7]	0	6.91	5.47	4.15	3.85	ns
36-bit Parity Check (internal)	2	16.06	12.07	8.87	8.19	ns

1. Implemented using 8 x 1 multiplier mode (unpipelined), register-to-register, two 8-bit inputs, one 16-bit output.
2. Implemented using two 32 x 4 RAMs and one 12-bit adder, one 8-bit input, one fixed operand, one 16-bit output.
3. Implemented using 8 x 1 multiplier mode (fully pipelined), two 8-bit inputs, one 16-bit output (7 of 15 PFUs contain only pipelining registers).
4. Implemented using 32 x 4 RAM mode with read data on 3-state buffer to bidirectional read/write bus.
5. Implemented using 32 x 4 dual-port RAM mode.
6. Implemented in one partially occupied SLIC with decoded output set up to CE in same PLC.
7. Implemented in five partially occupied SLICs.

Note: Shaded values apply only to OR3Txxx devices. -4 speed grade applies only to OR3Cxx devices.

Support

- *ORCA* Foundry Development System support.
- Supported by industry-standard CAE tools for design entry, synthesis, simulation, and timing analysis.

Description

FPGA Overview

The *ORCA* Series 3 FPGAs are a new generation of SRAM-based FPGAs built on the successful OR2C/TxxA FPGA (Series 2) , with enhancements and innovations geared toward today's high-speed designs and tomorrow's systems on a single chip. Designed from the start to be synthesis friendly and to reduce place and route times while maintaining the complete routability of the *ORCA* Series 2 devices, the Series 3 family more than doubles the logic available in each logic block and incorporates system-level features that can further reduce logic requirements and increase system speed. *ORCA* Series 3 devices contain many new patented enhancements and are offered in a variety of packages, speed grades, and temperature ranges.

The *ORCA* Series 3 FPGAs consist of three basic elements: programmable logic cells (PLCs), programmable input/output cells (PICs), and system-level features. An array of PLCs is surrounded by PICs. Each PLC contains a programmable function unit (PFU), a supplemental logic and interconnect cell (SLIC), local routing resources, and configuration RAM. Most of the FPGA logic is performed in the PFU (see Figure 1), but decoders, *PAL*-like functions, and 3-state buffering can be performed in the SLIC (see Figure 2). The PICs provide device inputs and outputs and can be used to register signals and to perform input demultiplexing, output multiplexing, and other functions on two output signals (see Figure 3). Some of the system-level functions include the new microprocessor interface (MPI) and the programmable clock manager (PCM).

PLC Logic

Each PFU within a PLC contains eight 4-input (16-bit) look-up tables (LUTs), eight latches/flip-flops (FFs), and one additional flip-flop that may be used independently or with arithmetic functions.

The PFU is organized in a twin-quad fashion: two sets of four LUTs and FFs that can be controlled independently. LUTs may also be combined for use in arithmetic functions using fast-carry chain logic in either 4-bit or 8-bit modes. The carry-out of either mode may be registered in the ninth FF for pipelining. Each PFU may also be configured as a synchronous 32 x 4 single- or dual-port RAM or ROM. The FFs (or latches) may obtain input from LUT outputs or directly from invertible PFU inputs, or they can be tied high or tied low. The FFs also have programmable clock polarity, clock enables, and local set/reset.

The SLIC is connected to PLC routing resources and to the outputs of the PFU. It contains 3-state, bidirectional buffers and logic to perform up to a 10-bit AND function for decoding, or an AND-OR with optional INVERT to perform *PAL*-like functions. The 3-state drivers in the SLIC and their direct connections to the PFU outputs make fast, true 3-state buses possible within the FPGA, reducing required routing and allowing for real-world system performance.

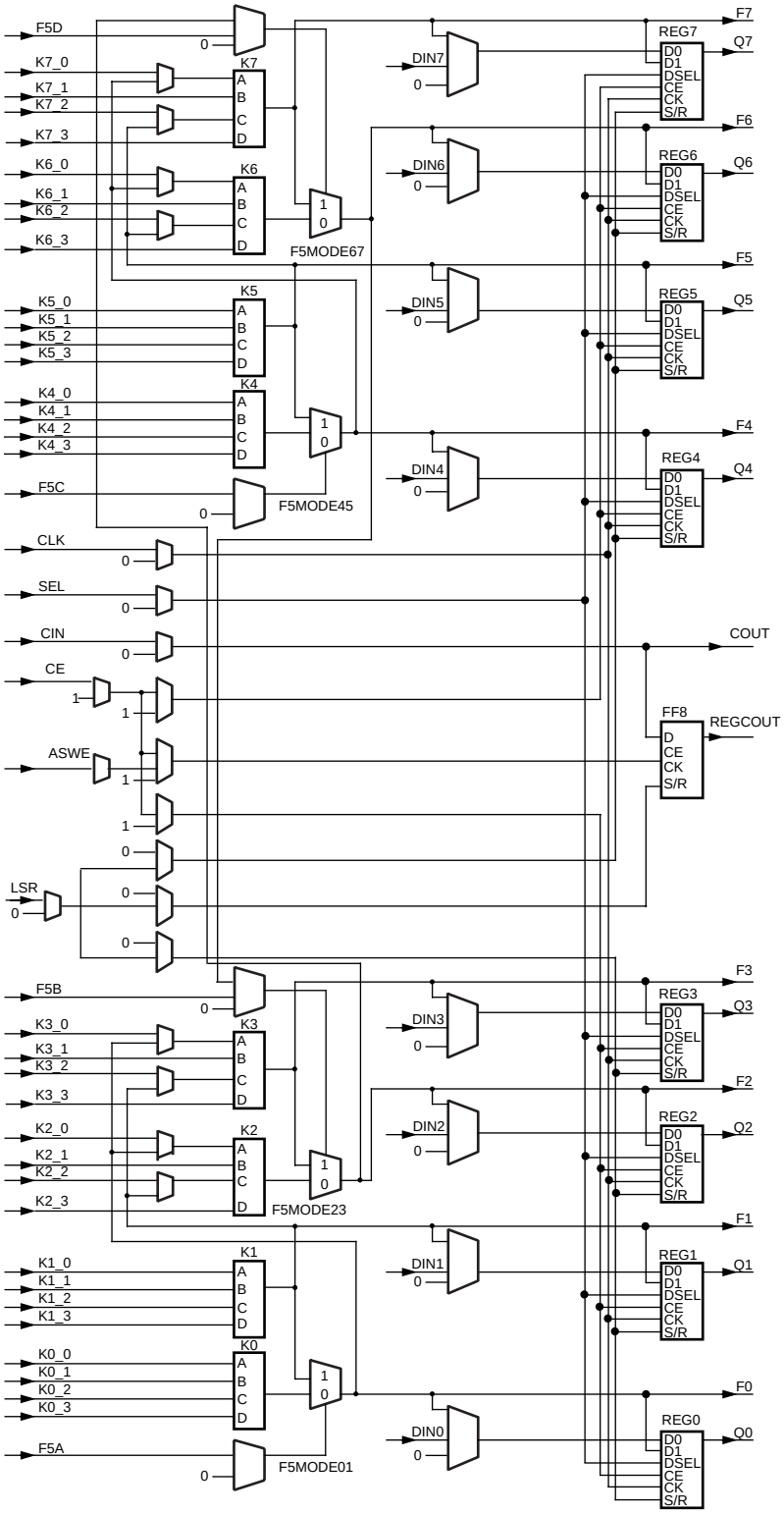
PIC Logic

The OR3C/Txxx PIC addresses the demand for ever-increasing system clock speeds. Each PIC contains four programmable inputs/outputs (PIOs) and routing resources. On the input side, each PIO contains a fast-capture latch that is clocked by an ExpressCLK. This latch is followed by a latch/FF that is clocked by a system clock from the internal general clock routing. The combination provides for very low setup requirements and zero hold times for signals coming on-chip. It may also be used to demultiplex an input signal, such as a multiplexed address/data signal, and register the signals without explicitly building a demultiplexer. Two input signals are available to the PLC array from each PIO, and the *ORCA* Series 2 capability to use any input pin as a clock or other global input is maintained.

On the output side of each PIO, two outputs from the PLC array can be routed to each output flip-flop, and logic can be associated with each I/O pad. The output logic associated with each pad allows for multiplexing of output signals and other functions of two output signals.

The output FF, in combination with output signal multiplexing, is particularly useful for registering address signals to be multiplexed with data, allowing a full clock cycle for the data to propagate to the output. The I/O buffer associated with each pad is very similar to the *ORCA* Series 2 buffer with a new, fast, open-drain option for ease of use on system buses. The output buffer signal can be inverted, and the 3-state control can be made active-high, active-low, or always enabled. In addition, this 3-state signal can be registered or nonregistered.

Description (continued)



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Note: All multiplexers without select inputs are configuration selector multiplexers.

Figure 1. Simplified PFU Diagram

Description (continued)

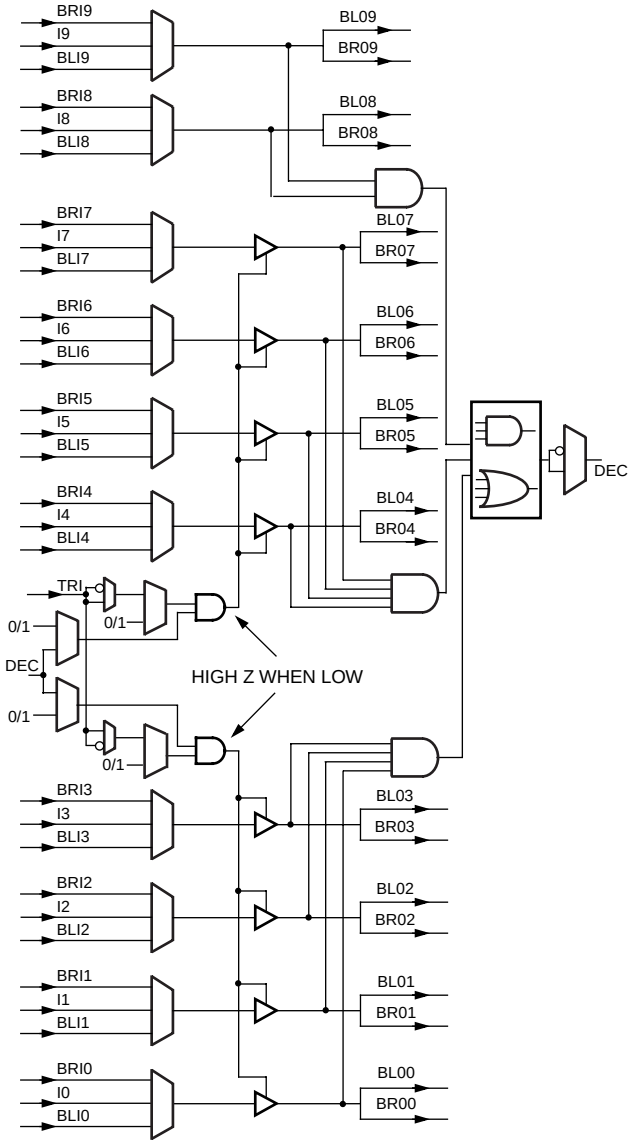

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Figure 2. SLIC Diagram (All Modes)

Description (continued)

System Features

The Series 3 also provides system-level functionality by means of its dual-use microprocessor interface (MPI) and its innovative programmable clock manager (PCM). These functional blocks allow for easy glueless system interfacing and the capability to adjust to varying conditions in today's high-speed systems.

The MPI provides a glueless interface between the FPGA and *PowerPC* and *i960* microprocessors. It can be used for configuration and readback, as well as for monitoring FPGA status. The MPI also provides a general-purpose microprocessor interface to the FPGA user-defined logic following configuration.

Two PCMs are provided on each Series 3 device. Each PCM can be used to manipulate the frequency, phase, and duty cycle of a clock signal. Clocks may be input from the dedicated corner ExpressCLK input (in the same corner as the PCM block) or from general routing. Output clocks from the PCM can be sent to the system clock spines and/or to the ExpressCLK and fast clock spines on the edges of the device adjacent to the PCM. ExpressCLK/fast clock and system clock output frequencies can differ by up to a factor of 8 to allow slow I/O clocking with fast internal processing (or vice versa). Each PCM is capable of manipulating clocks from 5 MHz to 120 MHz. Frequencies can be adjusted from 1/8x to 64x the input clock frequency, and duty cycles and phase delays can be adjusted from 3.125% to 96.875%.

Routing

The abundant routing resources of the Series 3 FPGAs are organized to route signals individually or as buses with related control signals. Clocks are routed on a low-skew, high-speed distribution network and may be sourced from PLC logic, externally from any I/O pad, or from the very fast ExpressCLK pins. ExpressCLKs may be glitchlessly and independently enabled and disabled with a programmable control signal using the new StopCLK feature. The improved PIC routing resources are now similar to the patented intra-PLC routing resources and provide great flexibility in moving signals to and from the PIOs. This flexibility translates into an improved capability to route designs at the required speeds when the I/O signals have been locked to specific pins.

Configuration

The FPGA's functionality is determined by internal configuration RAM. The FPGA's internal initialization/configuration circuitry loads the configuration data at powerup or under system control. The RAM is loaded by using one of several configuration modes. The configuration data resides externally in an EEPROM or any other storage media. Serial EEPROMs provide a simple, low pin count method for configuring FPGAs. A new, easy method for configuring the devices is through the microprocessor interface.

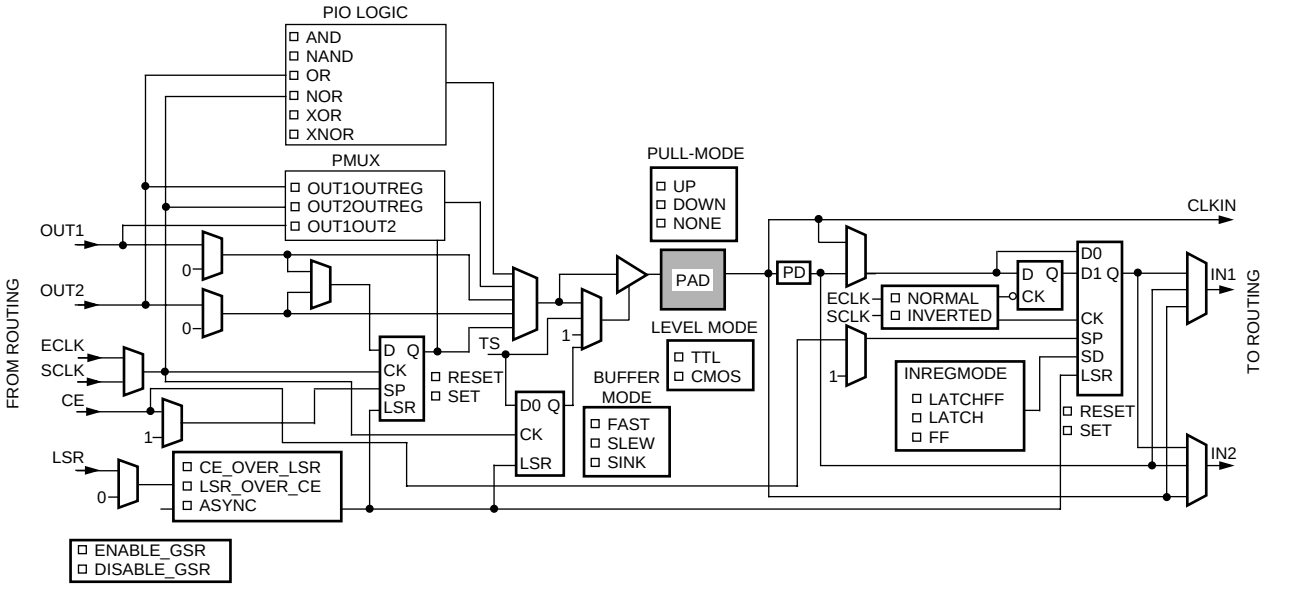


Figure 3. Series 3 Programmable Input/Output (PIO) Image from *ORCA* Foundry

Description (continued)

ORCA Foundry Development System

The *ORCA* Foundry Development System is used to process a design from a netlist to a configured FPGA. This system is used to map a design onto the *ORCA* architecture and then place and route it using *ORCA* Foundry's timing-driven tools. The development system also includes interfaces to, and libraries for, other popular CAE tools for design entry, synthesis, simulation, and timing analysis.

The *ORCA* Foundry Development System interfaces to front-end design entry tools and provides the tools to produce a configured FPGA. In the design flow, the user defines the functionality of the FPGA at two points in the design flow: at design entry and at the bit stream generation stage.

Following design entry, the development system's map, place, and route tools translate the netlist into a routed FPGA. A static timing analysis tool is provided to determine device speed and a back-annotated netlist can be created to allow simulation.

Timing and simulation output files from *ORCA* Foundry are also compatible with many third-party analysis tools. Its bit stream generator is then used to generate the configuration data which is loaded into the FPGA's internal configuration RAM.

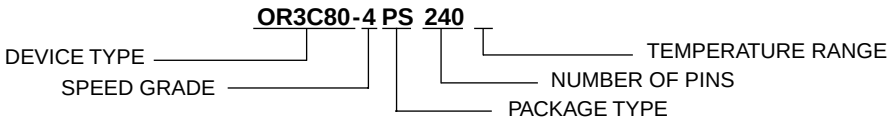
When using the bit stream generator, the user selects options that affect the functionality of the FPGA. Combined with the front-end tools, *ORCA* Foundry produces configuration data that implements the various logic and routing options discussed in this product brief.

Additional Information

Contact your local Lattice representative for additional information regarding the *ORCA* Series 3 FPGA devices, or visit our website at **http://www.latticesemi.com**

Ordering Information

Example:



OR3C80, -4 Speed Grade, 240-pin Power Quad Shrink Flat Package (SQFP2), Commercial Temperature.

Table 3. Voltage Options

Device	Voltage
OR3Cxx	5.0 V
OR3Txxx	3.3 V

Table 4. Temperature Options

Symbol	Description	Temperature
(Blank)	Commercial	0 °C to 70 °C
I	Industrial	–40 °C to +85 °C

Table 5. Package Options

Symbol	Description
BA	Plastic Ball Grid Array (PBGA)
BC	Enhanced Ball Grid Array (EBGA)
PS	Power Quad Shrink Flat Package (SQFP2)
S	Shrink Quad Flat Package (SQFP)

Table 6. *ORCA* Series 3 Package Matrix

Packages	208-Pin EIAJ SQFP	208-Pin EIAJ/SQFP2	240-Pin EIAJ SQFP	240-Pin EIAJ/SQFP2	256-Pin PBGA	352-Pin PBGA	432-Pin EBGA	600-Pin EBGA
	S208	PS208	S240	PS240	BA256	BA352	BC432	BC600
OR3T20	CI	—	CI	—	CI	CI	—	—
OR3T30	CI	—	CI	—	CI	CI	—	—
OR3C/T55	—	CI	—	CI	CI	CI	—	—
OR3C/T80	—	CI	—	CI	—	CI	CI	—
OR3T125	—	CI	—	CI	—	CI	CI	CI

Note: C = commercial, I = industrial.

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PN99-058FPGA (Replaces PN98-012FPGA)