Product Brief
January 2002

ORCA® ORT4622 Field-Programmable System Chip (FPSC) Four Channel x 622 Mbits/s Backplane Transceiver

Introduction

Lattice Semiconductor has developed a solution for designers who need the many advantages of FPGA-based design implementation, coupled with high-speed serial backplane data transfer. The 622 Mbits/s backplane transceiver offers a clockless, high-speed interface for interdevice communication on a board or across a backplane. The built-in clock recovery of the ORT4622 allows for higher system performance, easier-to-design clock domains in a multiboard system, and fewer signals on the backplane. Network designers will benefit from the backplane transceiver as a network termination device. The backplane transceiver offers SONET scrambling/descrambling of data and streamlined SONET framing, pointer moving, and transport overhead handling, plus the programmable logic to terminate the network into proprietary systems. For non-SONET applications, all SONET functionality is hidden from the user and no prior networking knowledge is required.

Embedded Core Features

- Implemented in an *ORCA* Series 3 FPGA array.
- Allows wide range of applications for SONET network termination application as well as generic data moving for high-speed backplane data transfer.
- No knowledge of SONET/SDH needed in generic applications. Simply supply data, 78 MHz clock, and a frame pulse.
- High-speed interface (HSI) function for clock/data recovery serial backplane data transfer without external clocks.
- HSI function uses a proven 622 Mbits/s serial interface core.
- Four-channel HSI function provides 622 Mbits/s serial interface per channel for a total chip bandwidth of 2.5 Gbits/s (full duplex).
- LVDS I/Os compliant with *EIA**-644, support hot insertion.
- 8:1 data multiplexing/demultiplexing for 77.76 MHz byte-wide data processing in FPGA logic.
- On-chip phase-lock loop (PLL) clock meets B jitter tolerance specification of ITU-T Recommendation G.958 (0.6 UIp-p at 250 kHz).
- Powerdown option of HSI receiver on a per-channel basis.
- Highly efficient implementation with only 3% overhead vs. 25% for 8B10B coding.
- In-Band management and configuration.
- Streamlined pointer processor (pointer mover) for 8 kHz frame alignment to system clocks.
- Built-in boundry scan (*IEEE* † 1149.1 JTAG).

* *EIA* is a registered trademark of Electronic Industries Association.
† *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Table 1. *ORCA* ORT4622—Available FPGA Logic

Device	Usable System Gates*	Number of LUTs	Number of Registers	Max User RAM	Max User I/Os	Array Size	Number of PFUs
ORT4622	60K—120K	4032	5304	64K	259	18 x 28	504

* The embedded core and interface are not included in the above gate counts. The usable gate count range from a logic-only gate count to a gate count assuming 30% of the PFUs/SLICs being used as RAMs. The logic-only gate count includes each PFU/SLIC (counted as 108 gates per PFU/SLIC), including 12 gates pre-LUT/FF pair (eight per PFU), and 12 gates per SLC/FF pair (one per PFU). Each of the four PIOs per PIC is counted as 16 gates (two FFs, fast-capture latch, output logic, CLK drivers, and I/O buffers). PFUs used as RAM are counted at four gates per bit, with each PFU capable of implementing a 32 x 4 RAM (or 512 gates) per PFU.

Embedded Core Features (continued)

- FIFOs align incoming data across all four channels for STS-48 (2.5 Gbits/s) operation (in quad STS-12 format).
- 1 + 1 protection supports STS-12/STS-48 redundancy by either software or hardware control for protection switching applications.
- Pseudo-SONET protocol including A1/A2 framing.
- SONET scrambling and descrambling for required ones density (optional).
- Selected transport overhead (TOH) bytes insertion and extraction for interdevice communication via the TOH serial link.

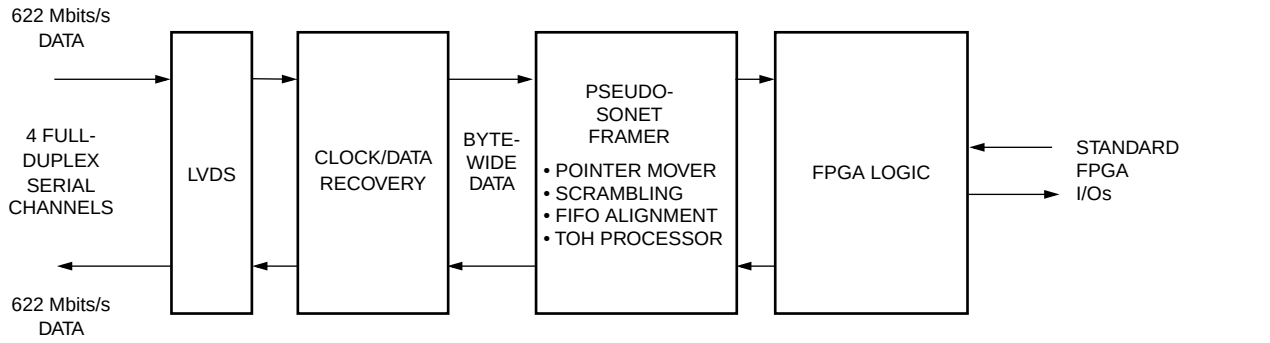

Figure 1. *ORCA* ORT4622 Block Diagram

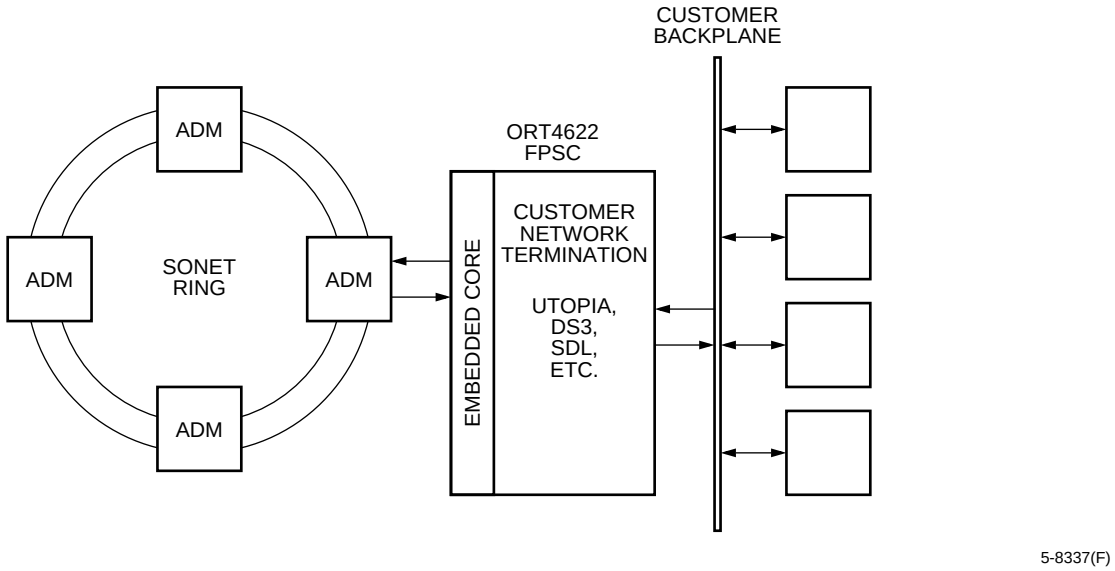

Figure 2. SONET Network Terminaton Application

Embedded Core Features (continued)

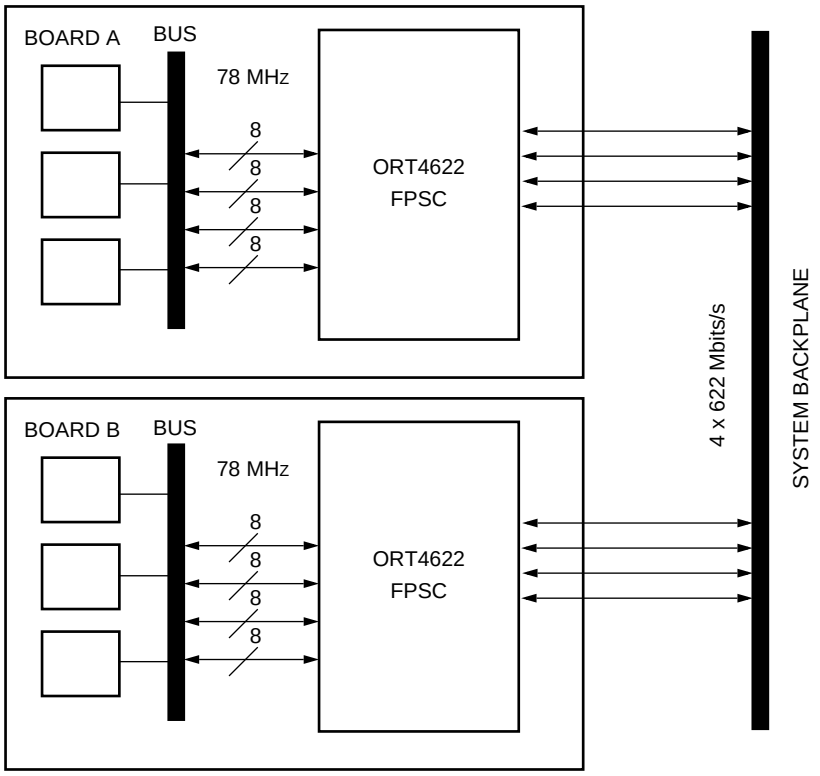

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Figure 3. High-Speed Backplane Data Transfer

FPSC Highlights

- Implemented as an embedded core in the *ORCA* Series 3+ FPSC architecture.
- Allows the user to integrate the core with up to 120K gates of programmable logic (all in one device) and provides up to 242 user I/Os in addition to the embedded core I/O pins.
- FPGA portion retains all of the features of the *ORCA* Series 3 FPGA architecture:
  - — High-performance, cost-effective, 0.25 µm, 5-level metal technology.
  - — Twin-quad programmable function unit (PFU) architecture with eight 16-bit look-up tables (LUTs) per PFU, organized in two nibbles for use in nibble- or byte-wide functions. Allows for mixed arithmetic and logic functions in a single PFU.
  - — Softwired LUTs (SWL) allow fast cascading of up to three levels of LUT logic in a single PFU.
  - — Supplemental logic and interconnect cell (SLIC) provides 3-statable buffers, up to 10-bit decoder, and *PAL**-like AND-OR-INVERT (AOI) in each programmable logic cell (PLC).
  - — Up to three ExpressCLK inputs allow extremely fast clocking of signals on- and off-chip plus access to internal general clock routing.
  - — Dual-use microprocessor interface (MPI) can be used for configuration, as well as for a general-purpose interface to the FPGA. Glueless interface to *i960*† and *PowerPC*‡ processors with user-configurable address space provided.

† *i960* is a registered trademark of Intel Corporation.
‡ *PowerPC* is a registered trademark of International Business Machines Corporation.

  - — Programmable clock manager (PCM) adjusts clock phase and duty cycle for input clock rates from 5 MHz to 120 MHz. The PCM may be combined with FPGA logic to create complex functions, such as digital phase-locked loops, frequency counters, and frequency synthesizers or clock doublers. Two PCMs are provided per device.
  - — True internal 3-state, bidirectional buses with simple control provided by the SLIC.
  - — 32 x 4 RAM per PFU, configurable as single or dual port. Create large, fast RAM/ROM blocks (128 x 8 in only eight PFUs) using the SLIC decoders as bank drivers.
  - — Built-in boundary scan (*IEEE* 1149.1 JTAG) and TS_ALL testability function to 3-state all I/O pins.
- High-speed on-chip interface provided between FPGA logic and embedded core to reduce bottlenecks typically found when interfacing off-chip.

Software Support

- Supported by *ORCA* Foundry software and third-party CAE tools for implementing *ORCA* Series 3+ devices and simulation/timing analysis with the embedded core functions.
- Embedded core configuration options and simulation netlists generated by the FPSC Configuration Manager utility.

Ordering Information

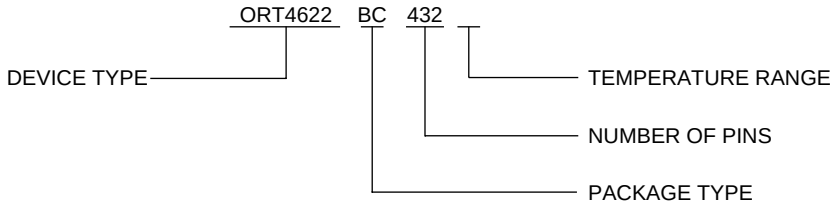

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Table 2. Voltage Options

Device	Voltage
ORT4622	2.5 V/3.3 V

Table 3. Temperature Options

Symbol	Description	Temperature
(Blank)	Commercial	0 ˚C to 70 ˚C
I	Industrial	–40 ˚C to +85 ˚C

Table 4. Package Type Options

Symbol	Description
BC	Enhanced Ball Grid Array (EBGA)
BM	Plastic Ball Grid Array, Multilayer

Table 5. *ORCA* Series 3+ Package Matrix

Device	Package	
	432-Pin EBGA	680-Pin PBGAM
	BC432	BM680
ORT4622	CI	CI

Key: C = commercial, I = industrial.

www.latticesemi.com

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PN00-072FPGA (Replaces DS99-143FPGA-1)

Lattice® Semiconductor Corporation