ispXP Technology

E² Non-Volatility + SRAM Reconfigurability = eXpanded Programmability

Lattice's new ispXP™ (eXpanded Programmability) technology combines the best features of E² and SRAM technologies. ispXP utilizes a combination of E²PROM non-volatile cells and SRAM technology to deliver a single-chip solution supporting "instant-on" start-up and infinite reconfigurability. A non-volatile E² array distributed within an ispXP device stores the device configuration. At power-up this information is transferred in a massively parallel fashion into SRAM bits that control the operation of the device. ispXP technology is available in the new ispXPGA™ family of FPGAs and the ispXPLD™ family of XPLDs.

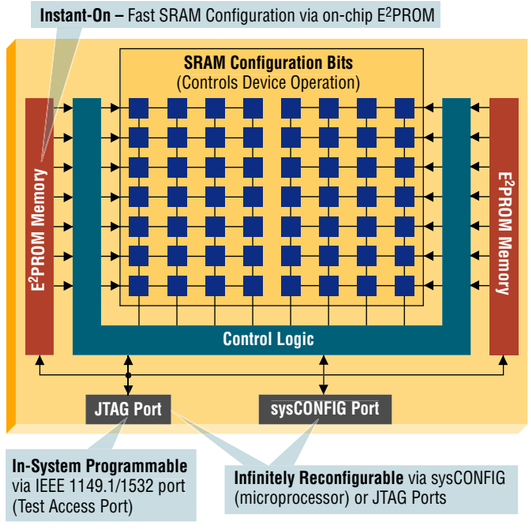
The ispXPGA family is the world's first FPGA to offer non-volatility and infinite reconfigurability. Other FPGA solutions force a compromise, being either reconfigurable or non-volatile. The ispXPGA family offers *both* of these capabilities with a mainstream architecture containing the features required for today's system-level design.

The ispXPLD 5000MX family represents a new class of devices called eXpanded Programmable Logic Devices (XPLDs). ispXPLD devices are built around a new building block, the Multi-Function Block (MFB). These blocks can be configured as SuperWIDE™ (136-input) logic, single- or dual-port memory, FIFO, or CAM depending on the user's application. This unparalleled PLD flexibility is combined with sysIO™ interfaces and sysCLOCK™ PLLs to ease the design process and speed time-to-market.

Key Features and Benefits

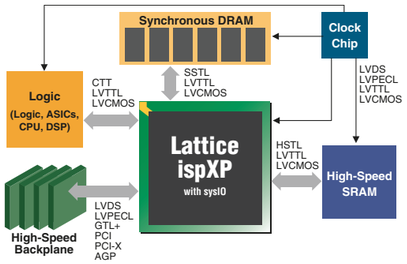
- **Instant-on at Power-up**
  - Availability of the PLD logic within 200µs of power-up
  - PLD logic available before microprocessor reset release
  - Superior solution for microprocessor glue logic and decoder logic
  - Supports power-up control applications
- **High Security – Eliminates External Configuration Bitstream**
  - Excellent for military and security-sensitive applications
  - Non-volatile security bits protect PLD pattern
- **Single-Chip Solution Eliminates Need for Boot PROM or External Storage Device**
  - Simplified design process
  - Reduced board space
  - Reduced inventory, handling and manufacturing costs
  - Improved reliability
- **Available in Two High-Performance Families Supporting 1.8, 2.5 or 3.3V Power Supplies**
  - ispXPGA Family of FPGAs
  - ispXPLD Family of XPLDs
- **Infinitely Reconfigurable SRAM via IEEE 1532 or sysCONFIG™ (Microprocessor) Interface**
- **In-System Programmable E²PROM via IEEE 1532 Port**
- **Boundary Scan Testable via IEEE 1149.1 (JTAG) Port**

ispXP Programming and Configuration



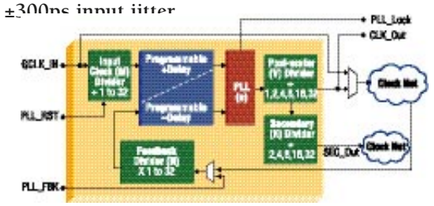
sysIO Interfaces

- On-board sysIO Banks allow ispXP devices to support a wide range of I/O standards
- Each sysIO Bank has its own separate I/O supply voltage and reference voltage



sysCLOCK PLL for Timing Control

- 10 to 320 MHz PLL operation
- ±100ps cycle-to-cycle jitter
- ±150ps period jitter
- ±300ps input jitter

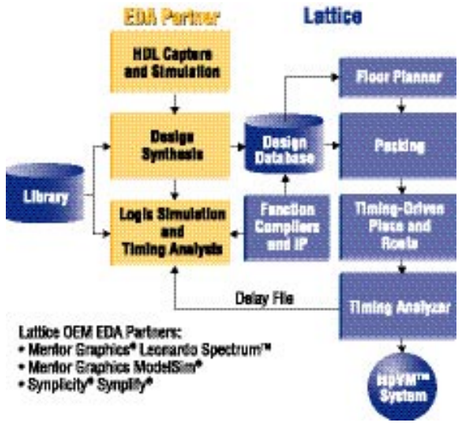


ispLEVER™ Software Support

ispLEVER, Lattice's new generation of full-featured PLD design tools, supports both the ispXPGA and ispXPLD product families. ispLEVER software offers:

- Fully integrated synthesis, RTL and timing simulation tools
- Complete design flow for all Lattice device families
- Advanced timing-driven placement and routing
- IP manager and module generator
- Fast, efficient run times and competitive device performance

ispLEVER Design Software Flow Chart



ispXPGA Family*

Core Voltage: ispXPGA xxxxB = 3.3 or 2.5V; ispXPGA xxxxC = 1.8V

Family Member	System Gates	PFUs	LUT-4	Logic FFs	Block RAM	Distributed RAM	sysHSI™** Channels	PLLs	User I/O
ispXPGA 125/E	139K	484	1,936	3.8K	92K	30K	4	8	176
ispXPGA 200/E	210K	676	2,704	5.4K	111K	43K	8	8	208
ispXPGA 500/E	476K	1,764	7,056	14.1K	184K	112K	12	8	336
ispXPGA 1200/E	1.25M	3,844	15,376	30.8K	414K	246K	20	8	496

* Preliminary Information

** "E" series does not support sysHSI.

ispXPLD 5000MX Family*

Core Voltage: ispXPLD 5000MC = 1.8V; ispXPLD 5000MB = 2.5V; ispXPLD 5000MV = 3.3V

Family Member	System Gates	Macrocells	Memory	CAM	PLLs	User I/O	t_{PD}	t_S	t_{CO}	F_{MAX}
ispXPLD 5256MX	75K	256	128K	48K	2	141	4.0ns	2.5ns	2.8ns	285MHz
ispXPLD 5512MX	150K	512	256K	96K	2	253	4.5ns	2.9ns	3.0ns	250MHz
ispXPLD 5768MX	225K	768	384K	144K	2	317	5.0ns	3.6ns	3.8ns	225MHz
ispXPLD 51024MX	300K	1,024	512K	192K	2	381	5.0ns	3.6ns	3.8ns	225MHz

* Preliminary Information

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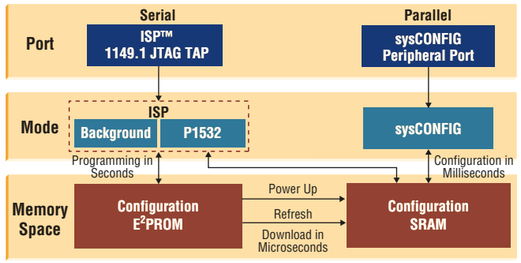
ispXP Overview

ispXP Technology

Non-volatile and infinitely reconfigurable, ispXP devices give logic designers a superior programmable solution. ispXP devices provide logic availability within microseconds of power-up/reconfiguration, reprogrammability and high security ... all in one chip. Significant savings accrue in board space, system design effort, inventory costs, handling costs, and manufacturing costs. Improve time-to-market and lower costs with Lattice ispXPGA and ispXPLD devices.

Flexible Programming and Configuration Modes

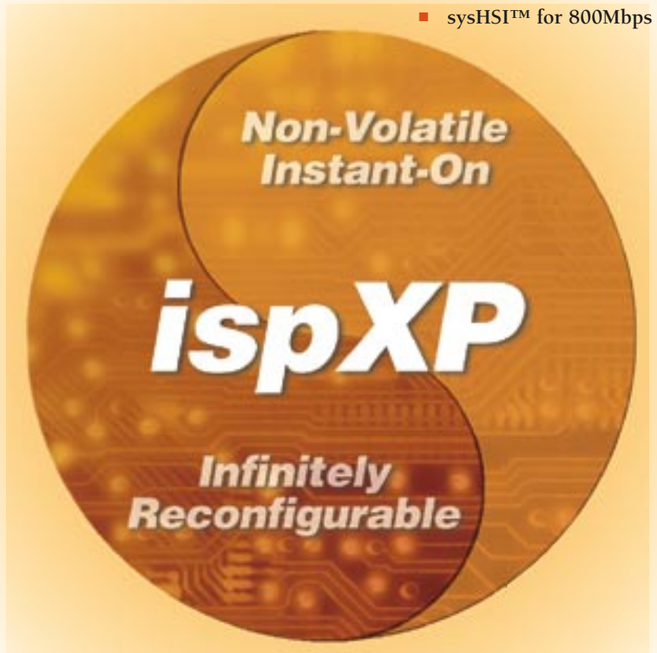


Self-Configuration in Micro-seconds

- Instant-on (less than 200µS)
- PLD logic available within microseconds of power-up
- Reliable configuration by design

High Security

- ispXP devices include security bits to prevent readback
- No external bitstream
- Totally secure from bitstream "snooping"
- Excellent solution for security-sensitive applications



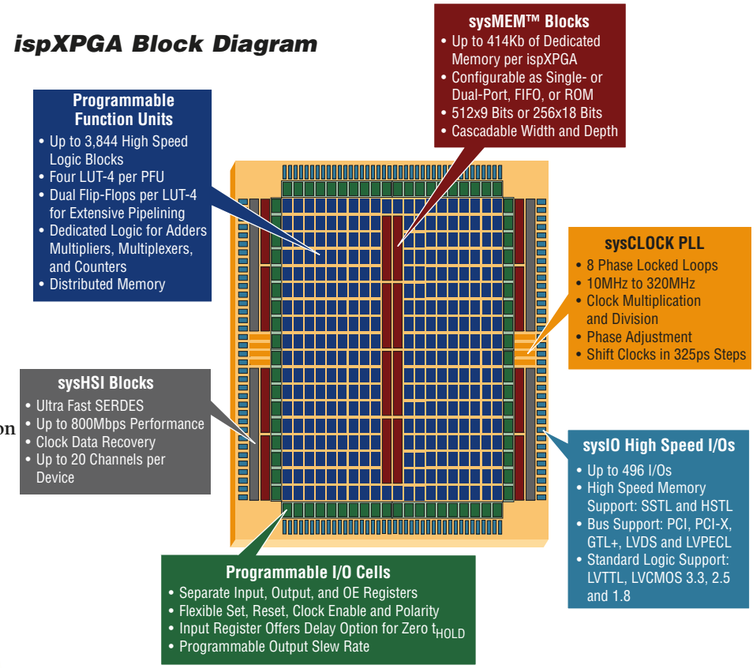
Single Chip Solution

- No external Boot PROM needed for configuration
  - No Boot PROM noise issues
  - No Boot PROM reliability issues
  - No Boot PROM board space concerns
- Single-chip solution reduces inventory, handling, and manufacturing costs
- Simplified design

ispXPGA Family

- High-performance FPGAs
- System-level integration
  - 1.25M system gates
  - 496 I/Os
  - 414Kb embedded memory
- High performance logic blocks (PFUs)
- Block and distributed memory
- sysCLOCK PLLs for clock management
- sysIO for high performance interfacing
- Two options available
  - High performance sysHSI (standard part #)
  - Low-cost, no sysHSI ("E" series)
  - 414Kb embedded memory
- sysHSI™ for 800Mbps serial communication

ispXPGA Block Diagram



ispXPLD Family

- High-performance 3rd generation PLDs
- Flexible Multi-Function Block (MFB) archit
  - SuperWIDE logic
  - Arithmetic support
  - Single- or dual-port RAM
  - Asynchronous FIFO
  - Ternary CAM
- High-Speed: 4.0ns pin-to-pin delays
- Low Power: Static power as low as 20mA
- sysCLOCK PLLs and sysIO

ispXPLD 5000MX Block Diagram