Non-Volatile Instant-On

Infinitely Reconfigurable

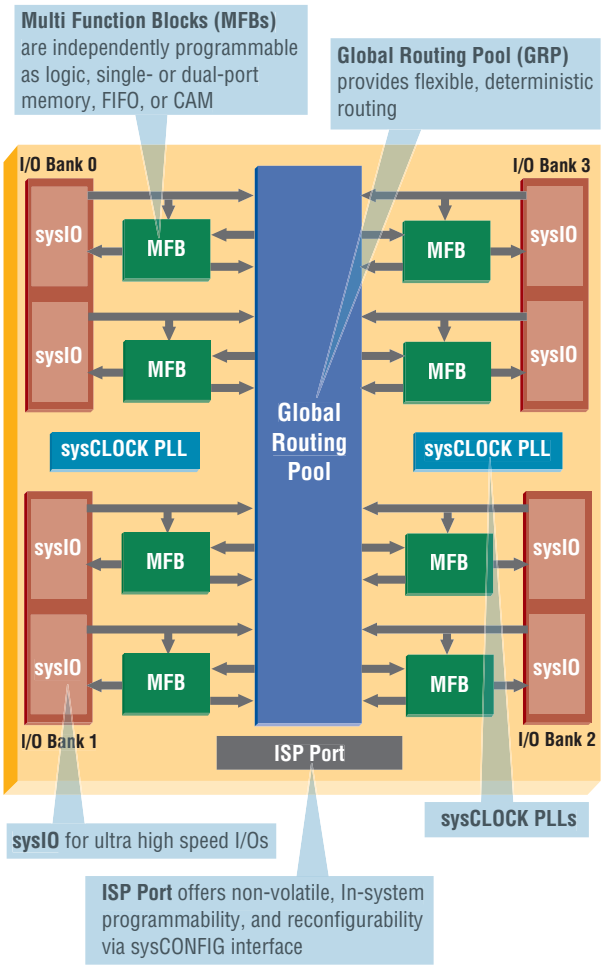
ispXPLD 5000MX

Ultimate ispXP™ Flexibility

The ispXPLD™ 5000MX family represents a new class of devices from Lattice Semiconductor called eXpanded Programmable Logic Devices (XPLDs). These devices are built around a new building block, the Multi-Function Block (MFB). These blocks can be configured as SuperWIDE™ (136-input) logic, single- or dual-port memory, FIFO, or CAM depending on the user's application.

This unparalleled PLD flexibility is combined with sysIO™ interfaces for support of leading edge standards such as LVDS, HSTL, and SSTL, along with the more familiar LVCMOS standards. sysCLOCK™ PLLs allow easy clock management. ispXPLD 5000MX devices provide expanded in-system programming referred to as ispXP. As such, ispXPLD devices are non-volatile and infinitely reconfigurable. They can be programmed through an industry standard IEEE 1532 interface or reconfigured through the Lattice sysCONFIG™ interface. Devices are available to support 3.3, 2.5, and 1.8-volt power supply operation.

ispXPLD 5256MX Block Diagram



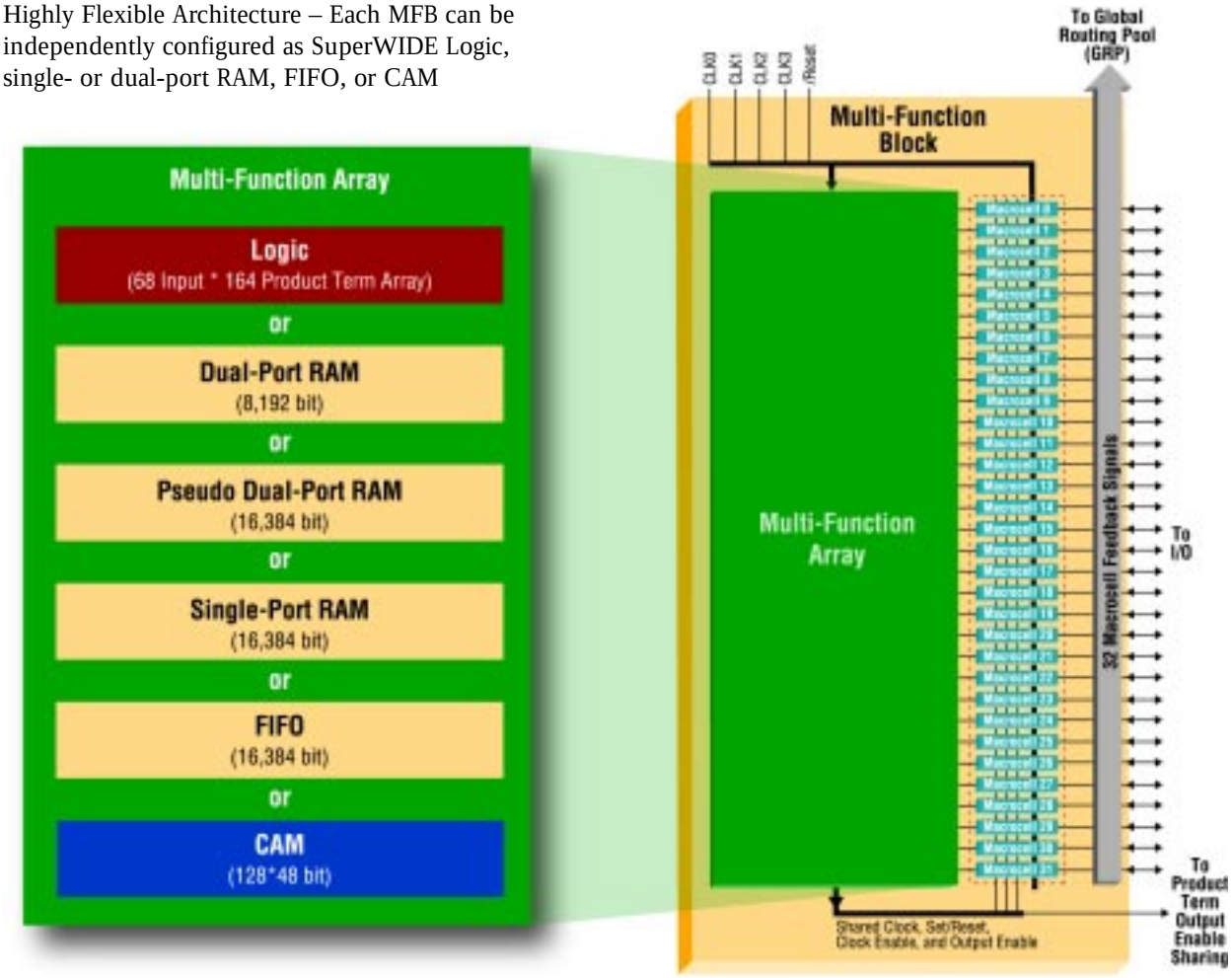
Key Features and Benefits

- **Flexible MFB Architecture**
  - SuperWIDE Logic
  - Arithmetic support
  - Single- or Dual-Port RAM
  - Asynchronous FIFO
  - Ternary CAM
- **sysCLOCK PLLs**
  - Multiply & divide
  - Clock shifting
- **sysIO Interfaces**
  - LVTTL, LVCMOS 1.8, 2.5, 3.3: Programmable drive strength; Flexible bus-maintenance; Hot-socketing
  - SSTL, HSTL
  - GTL+, PCI-X, PCI 3.3, AGP-1X
  - LVDS
  - LVPECL
- **Expanded In-System Programming (ispXP)**
  - Instant-on capability
  - Single chip convenience
  - ISP™ via IEEE 1532 Interface
  - Infinitely reconfigurable via IEEE 1532 or sysCONFIG interface
  - Security scheme
- **High Speed Operation**
  - 4.0ns pin-to-pin delays
  - 300 MHz f_{MAX}
  - Deterministic timing
- **Low Power Consumption**
  - Static power as low as 20mA
  - 1.8-volt core for low dynamic power
- **Easy System Integration**
  - 3.3, 2.5 and 1.8-volt power supply operation
  - IEEE 1149.1 boundary scan testing
  - Lead-free package options

ispXPLD 5000MX Architecture

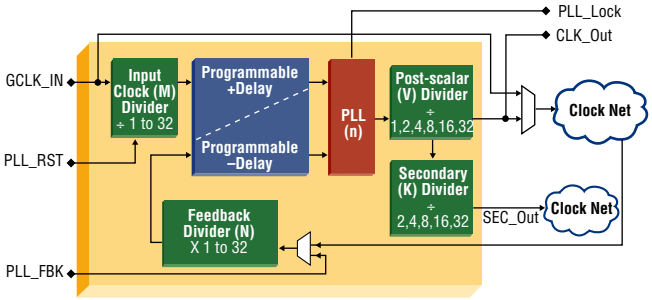
Multi-Function Block MFB

- Highly Flexible Architecture – Each MFB can be independently configured as SuperWIDE Logic, single- or dual-port RAM, FIFO, or CAM



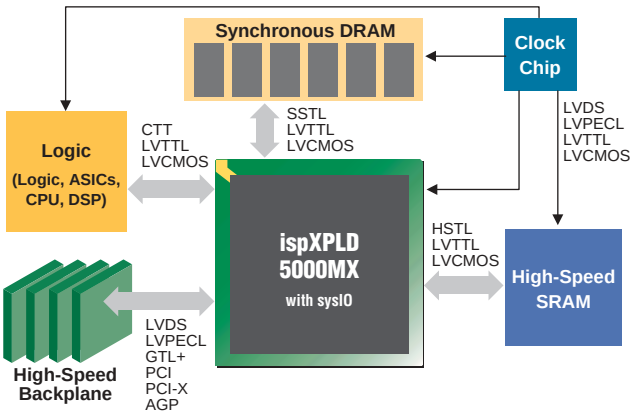
sysCLOCK PLL for Timing Control

- 2 sysCLOCK PLLs per device
- 10 to 320 MHz PLL operation
- ±100ps cycle-to-cycle jitter
- ±150ps period jitter
- ±300ps input jitter



sysIO Interfaces

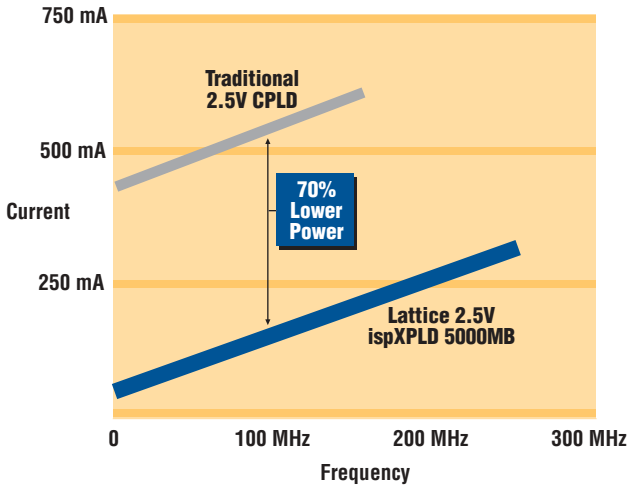
- On-board sysIO Banks allow ispXPLD 5000MX devices to support a wide range of I/O standards
- Each sysIO Bank has its own separate I/O supply voltage and reference voltage



ispXPLD 5000MX Features

Low Power

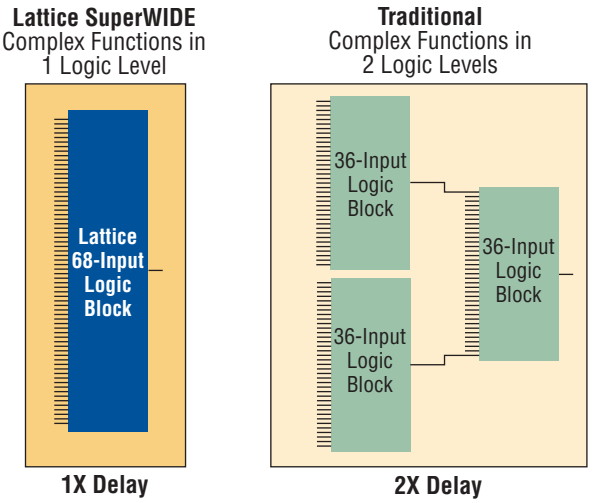
- 70% reduction in power consumption (@ 100MHz)
- Low static power – zero power E^2 cells, full CMOS design
- Low power benefits: improved reliability, smaller power supplies, less cooling required



Note: Power consumption of 512 macrocell device

SuperWIDE Architecture

- 68-input logic block implements complex functions in one logic level
- Two MFBs (Multi-Function Blocks) can be combined to support up to 136 inputs!

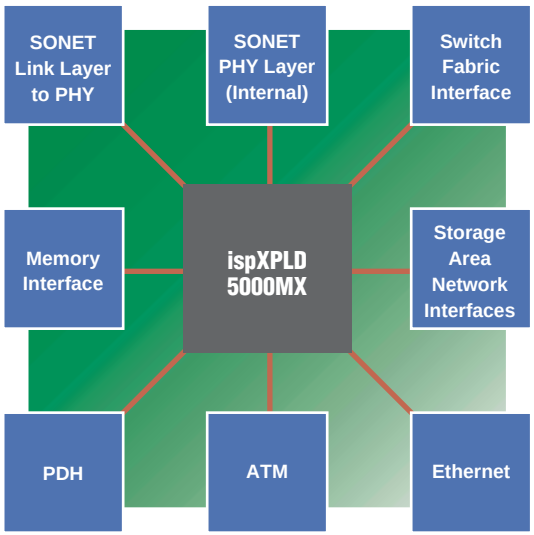


ispXP, sysIO, sysCLOCK, SINGLE- OR DUAL-PORT RAM, FIFO, CAM, AND PROGRAMMABLE LOGIC ALL IN ONE PACKAGE. THE ispXPLD 5000MX OFFERS THE ULTIMATE IN LOGIC DESIGN FLEXIBILITY.

ispXPLD 5000MX Applications

The ispXPLD 5000MX Family is an excellent solution for bus bridging applications. ispXPLD 5000MX features include:

- Instant-on
- High performance – 4.0ns pin-to-pin delay
- sysIO interfaces for high-speed I/Os
- sysCLOCK PLLs for easy timing control
- Memory for buffering



ispXPLD 5000MV, 5000MB and 5000MC Family Attributes*

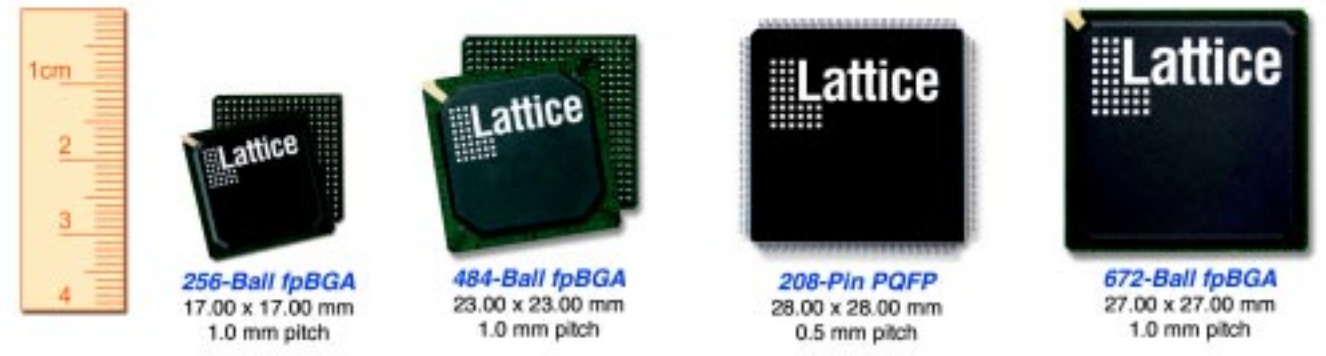
Family Member	System Gates	Macrocells	Memory kbit	CAM kbit	PLLs	t_{PD}	t_S	t_{CO}	F_{MAX}	Vcc
ispXPLD 5256MV	75K	256	128	48	2	4.0ns	2.2ns	2.8ns	300MHz	3.3V
ispXPLD 5512MV	150K	512	256	96	2	4.5ns	2.8ns	3.0ns	270MHz	3.3V
ispXPLD 5768MV	225K	768	384	144	2	5.0ns	2.8ns	3.2ns	250MHz	3.3V
ispXPLD 51024MV	300K	1024	512	192	2	5.2ns	3.0ns	3.7ns	250MHz	3.3V
ispXPLD 5256MB	75K	256	128	48	2	4.0ns	2.2ns	2.8ns	300MHz	2.5V
ispXPLD 5512MB	150K	512	256	96	2	4.5ns	2.8ns	3.0ns	270MHz	2.5V
ispXPLD 5768MB	225K	768	384	144	2	5.0ns	2.8ns	3.2ns	250MHz	2.5V
ispXPLD 51024MB	300K	1024	512	192	2	5.2ns	3.0ns	3.7ns	250MHz	2.5V
ispXPLD 5256MC	75K	256	128	48	2	4.0ns	2.2ns	2.8ns	300MHz	1.8V
ispXPLD 5512MC	150K	512	256	96	2	4.5ns	2.8ns	3.0ns	270MHz	1.8V
ispXPLD 5768MC	225K	768	384	144	2	5.0ns	2.8ns	3.2ns	250MHz	1.8V
ispXPLD 51024MC	300K	1024	512	192	2	5.2ns	3.0ns	3.7ns	250MHz	1.8V

ispXPLD 5000MX Family Package Options and Available I/Os

Family Member	208 PQFP	256 fpBGA*	484 fpBGA*	672 fpBGA*
ispXPLD 5256MX	–	141	–	–
ispXPLD 5512MX	149	193	253	–
ispXPLD 5768MX	–	193	317	–
ispXPLD 51024MX	–	–	317	381

* fpBGA = Fine Pitch BGA (1.0mm ball pitch)

ispXPLD 5000MX Advanced Packaging



Packages are shown actual size. Dimensions refer to package body size.

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