# ispXPGA

**Non-Volatile Infinitely-Reconfigurable Instant-On FPGAs**

## The World's First FPGA to Offer Non-Volatility and Reconfigurability

The ispXPGA™ family of devices allows the creation of high-performance logic designs that are both non-volatile and infinitely reconfigurable. Other FPGA solutions force a compromise, being either reprogrammable, or reconfigurable, or non-volatile. This family offers *all* of these capabilities with a mainstream architecture containing the features required for today's system-level design. We call this concept ispXP™, for eXpanded Programmability.


## ispXPGA Programming / Configuration

- Auto-configure at Power-up in Microseconds
- Reconfigure In-System
- Reprogram During System Operation
- Configure from On-Chip $E^2$ or CPU
- Set Security Bits to Prevent Readback
- No External Configuration Memory
- Totally Secure from Bit-Stream Snooping

The ispXPGA family is available in two options. The standard device supports sysHSI capability for ultra fast serial communications and the "E" series, a high performance, low cost device with no sysHSI functionality.

## Key Features and Benefits

- **Non-Volatile, Infinitely Reconfigurable**
  - Power-up in Microseconds via On-Chip $E^2$ Cells for Instant-on Usage
  - Reconfigure SRAM-based Logic In-System
  - In-System Programmable
  - No External Configuration Memory
- **System-Level Integration**
  - 139K to 1.25M System Gates
  - Up to 496 I/Os
  - Up to 414Kb Embedded Memory
- **High Performance Logic Blocks (PFUs)**
- **Block and Distributed Memory**
- **Variable-Length-Interconnect™ Routing**
- **sysCLOCK™ PLLs for Clock Management**
- **sysIO™ for High Performance Interfacing**
- **Two Options Available**
  - High Performance sysHSI (Standard Part Number)
  - Low-cost, No sysHSI ("E" Series)
- **sysHSI™ for up to 800Mbps Serial Communications**
- **1.8V, 2.5V, and 3.3V Operation**

Instant-on Non-Volatile & Reprogrammable

## ispXPGA Family

| Family Member | System Gates | PFUs | LUT-4 | Logic FFs | Block RAM | Distributed RAM | sysHSI™* Channels | User I/O | Vcc | Packaging | Body Size |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ispXPGA 125/E | 139K | 484 | 1936 | 3.8K | 92K | 30K | 4 | 160<br>176 | 1.8, 2.5, 3.3V | 256 fpBGA<br>516 fpBGA** | 17x17mm<br>31x31mm |
| ispXPGA 200/E | 210K | 676 | 2704 | 5.4K | 111K | 43K | 8 | 160<br>208 | 1.8, 2.5, 3.3V | 256 fpBGA<br>516 fpBGA** | 17x17mm<br>31x31mm |
| ispXPGA 500/E | 476K | 1764 | 7056 | 14.1K | 184K | 112K | 12 | 336<br>336 | 1.8, 2.5, 3.3V | 516 fpBGA**<br>900 fpBGA | 31x31mm<br>31x31mm |
| ispXPGA 1200/E | 1.25M | 3844 | 15376 | 30.8K | 414K | 246K | 20 | 496<br>496 | 1.8, 2.5, 3.3V | 680 fpSBGA**<br>900 fpBGA | 40x40mm<br>31x31mm |

*"E" series does not support sysHSI.
** Thermally enhanced

## *ispLEVER™ Design Software*

Lattice's ispLEVER is a new generation of PLD design tool equipped to provide a complete system for FPSC, FPGA, ispXPLD™, CPLD, ispGDX® and SPLD design. ispLEVER includes a fully integrated, push-button design environment and advanced features for interactive design optimization and debug.

### Features

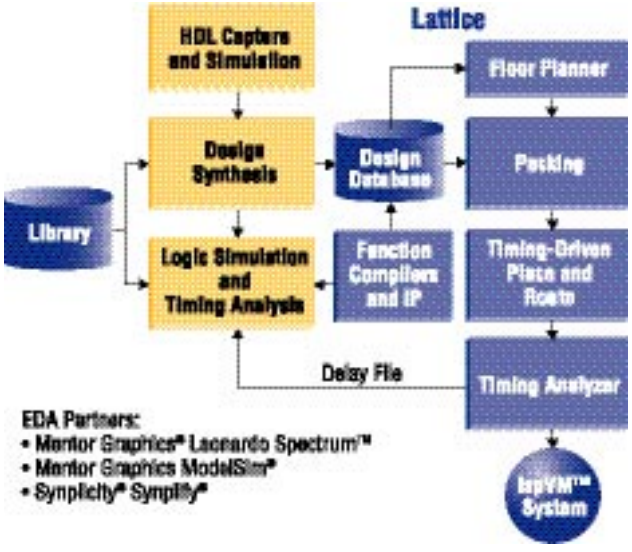
- Fully Integrated Synthesis and RTL and Timing Simulation Tools
- Complete Design Flow for All In-System Programmable (ISP™) Lattice Device Families
- Advanced Timing-Driven Placement and Routing
- IP Manager and Module Generator
- Fast, Efficient Run Times and Competitive Device Performance and Utilization
- Supported by Libraries from Leading CAE Vendors
  - Aldec
  - Cadence
  - Innoveda
  - Mentor Graphics
  - Synopsys
  - Synplicity
- Windows® and UNIX® Solutions

## *ispXPGA Select Performance*

$T_A$ = 25° C; $V_{CC}$ = 1.8V

| Function | | Speed |
|---|---|---|
| 4-Input LUT Delay | | 440ps |
| Synchronous Counter | 8-bit | 334MHz |
| Loadable Up/Dn Carry-Ripple Counter | 64-bit | 156MHz |
| Carry-Ripple Adder | 64-bit | 232MHz |
| Multiplexer | 64:1 | 237MHz |
| De-Multiplexer | 1:64 | 371MHz |
| Shift Reg Up/Dn, Circular Shift | 64-bit | 315MHz |
| Barrel Shifter | 64-bit | 184MHz |
| PLL Frequency | Min<br>Max | 10 MHz<br>320 MHz |
| LVDS with Clock Recovery | Max | 950Mbit |

## *ispLEVER Design Software Flow Chart*




## *Applications Support*

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