# ispMACH 5000VG

## New High Density Architecture for System-Level Integration

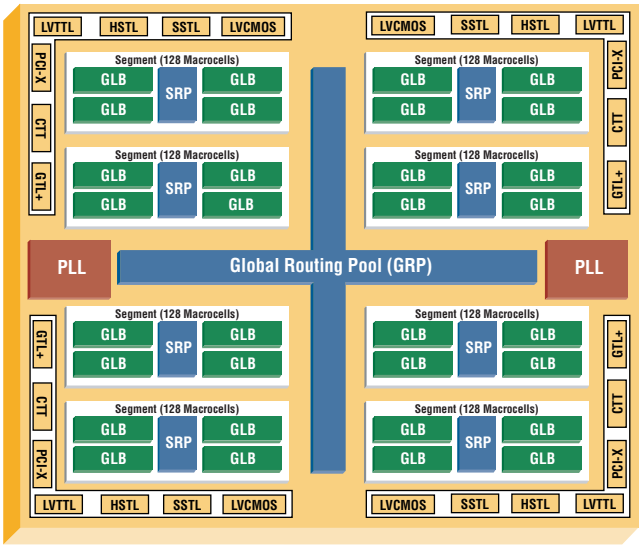
### Superior Density, Performance and Architecture

The ispMACH™ 5000VG Family extends Lattice's successful SuperWIDE™ architecture to higher SuperBIG™ densities. By providing up to 1024 macrocells in a single device, the family increases system level integration by allowing many functions to be combined into a single device.

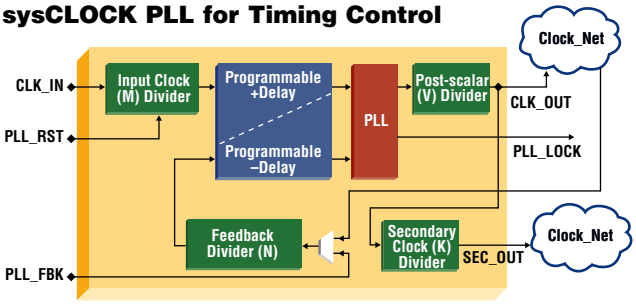
The increased logic capacity of these devices is complemented with sysCLOCK™ PLL and sysIO™ capabilities. sysCLOCK phase locked loops (PLLs) provide design engineers with the capability to multiply, divide, and skew clock signals, an important capability for today's high-performance systems. By supporting advanced I/O standards such as HSTL, SSTL, GTL+, and LVCMOS, sysIO capability allows easy interfacing with high-speed devices supporting these I/O standards.

The SuperWIDE logic blocks of the ispMACH 5000VG Family are optimized for implementing wide functions common in 32-bit and 64-bit systems. Compared to competitive devices with narrower logic, ispMACH 5000VG devices can boost performance by up to 60%!


### ispMACH 51024VG Block Diagram




### sysCLOCK PLL for Timing Control

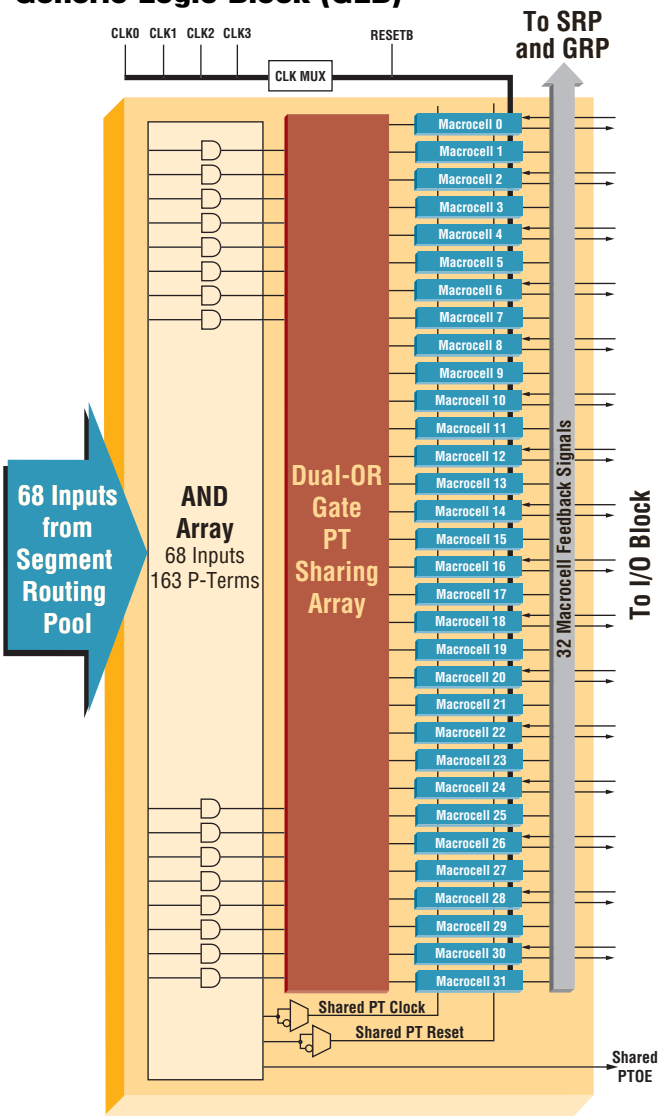



### Key Features and Benefits

- **SuperBIG™ Logic Density**
  - Up to 1024 Macrocells and 384 I/Os for System Level Integration
  - High Performance Two-Tiered Routing
  - 5.0ns $t_{PD}$ Segment Routing; 6.5ns $t_{PD}$ Global Routing
- **SuperWIDE™ Logic Block**
  - 68 Inputs per Logic Block
  - Up to 160 Product Terms per Output
- **sysCLOCK™ PLL**
  - Clock Frequency Synthesis and Skew Management
  - Clock Multiply and Divide Capability
  - Clock Shifting by ±3.5ns in 500ps Steps
  - Differential LVDS and LVPECL Input Support
- **sysIO™ Capability**
  - LVCMOS 1.8, 2.5, 3.3 and LVTTL Support for Standard Board Interfaces
  - SSTL 2/3 Class I and II Support for DRAM Interfaces
  - HSTL Class I and III Support for SRAM Interfaces
  - GTL+, PCI-X for Bus Interfaces
  - 5 Volt Tolerance and Hot-Socketing Capability
- **IEEE 1149.1 Boundary Scan Testable**
- **In-System Programmable via IEEE 1532 ISC Compliant Interface**

# ispMACH 5000VG Architecture

## Generic Logic Block (GLB)

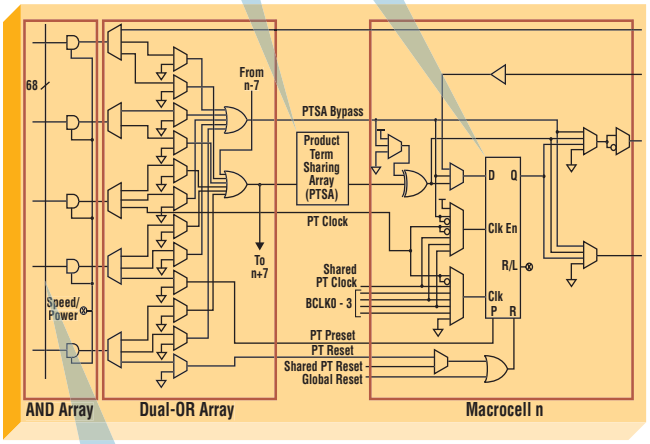



## SuperWIDE™ LOGIC BLOCKS FOR HIGH PERFORMANCE

PTSA expansion capability to support up to **160 Product Terms** per output for increased performance

Flexible register to support a variety of HDL design styles

### Macrocell Perspective

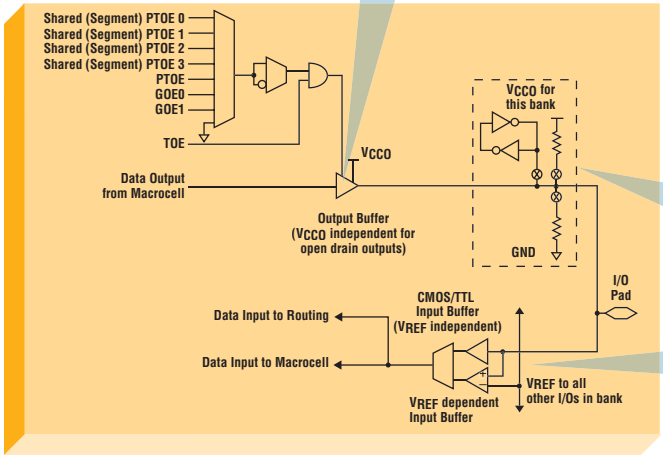



SuperWIDE **68 Inputs** for high performance wide functions

## sysIO™ CAPABILITY FOR SYSTEM FLEXIBILITY

Programmable drive strength and separate I/O power supply enable support for multiple standards

### I/O Block




Flexible bus maintenance circuitry with pull-up, pull-down, and bus-keeper options

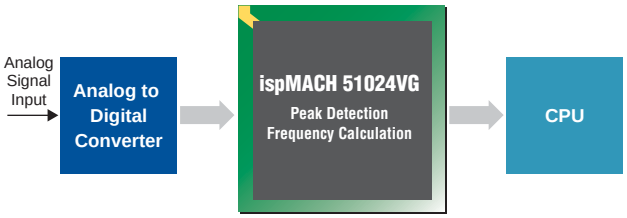
Programmable trip points and comparator for multi-standard support

# ispMACH 5000VG Applications

## High-Speed Digital Signal Processing

The SuperWIDE architecture of the ispMACH 5000VG is perfect for implementing high performance DSP applications. In this application, the ispMACH 51024VG performs:

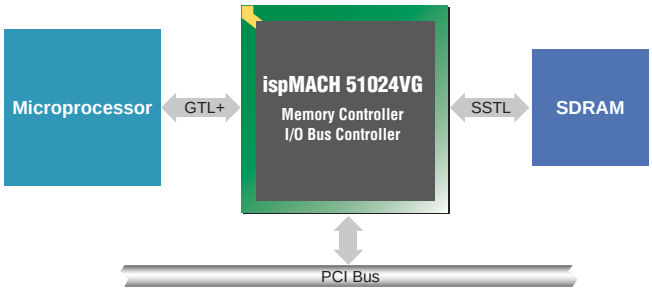
- Peak detection on a 100MHz signal
- Absolute and relative maximum value calculation




## Memory and I/O Bus Controller

The sysIO feature is ideal for interfacing with various memories and microprocessors. In this application, the ispMACH 51024VG performs the following interface functions:

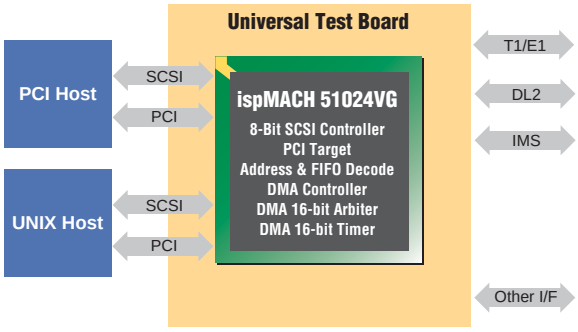
- CPU: GTL+
- SDRAM: SSTL
- Peripheral: PCI bus




## Wireless Base Station Test Board

The ispMACH 51024VG is large enough to integrate many functions to reduce chip count. In this application, the ispMACH 51024VG performs:

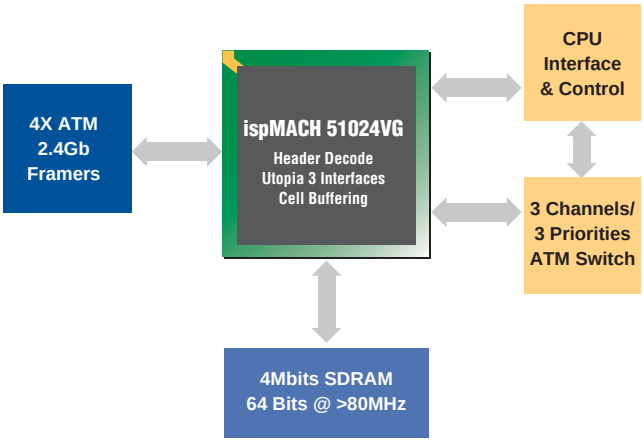
- SCSI Controller
- PCI Interface
- DMA and FIFO control




## ATM Switch

The sysCLOCK PLL allows the ispMACH 51024VG to easily interface with SDRAM. In this networking application, the ispMACH 51024VG performs:

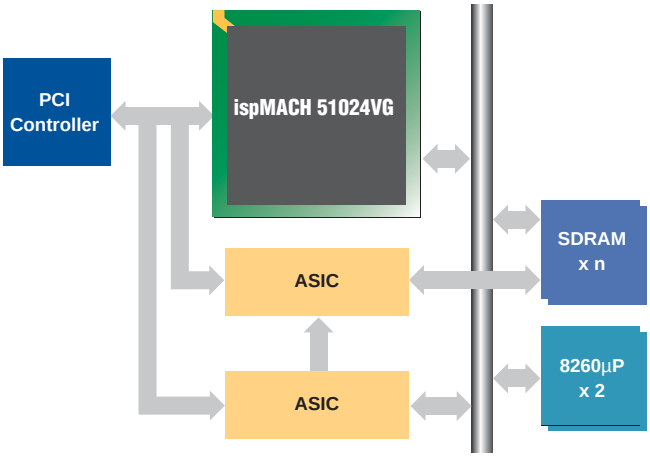
- 32-bit decode function
- High Speed (>80MHz) 64bit SDRAM Interface
- sysIO interface functions




## Central Office Switch / Carrier Card

The flexibility of the sysIO interface allows the ispMACH 51024VG to function in complex environments. In this application, the ispMACH 51024VG performs:

- I/O voltage translation (2.5V and 3.3V)
- SDRAM interface
- sysIO interface to ASICs



## ispMACH 5000VG and ispLSI 5000VE Family Attributes

| Family Member | Macrocells | GLB Inputs | Product Terms per Output | Segment $t_{PD}$ | Global $t_{PD}$ | $t_{SU}$ | $t_{CO}$ | Fmax | Vcc |
|---|---|---|---|---|---|---|---|---|---|
| ispLSI 5128VE | 128 | 68 | 35 | – | 5.0ns | 3.5ns | 3.0ns | 180MHz | 3.3V |
| ispLSI 5256VE | 256 | 68 | 35 | – | 6.0ns | 4.0ns | 3.0ns | 165MHz | 3.3V |
| ispLSI 5384VE | 384 | 68 | 35 | – | 6.0ns | 4.0ns | 3.0ns | 165MHz | 3.3V |
| ispLSI 5512VE | 512 | 68 | 35 | – | 6.5ns | 4.5ns | 3.5ns | 155MHz | 3.3V |
| ispMACH 5768VG* | 768 | 68 | 160 | 5.0ns | 6.5ns | 3.0ns | 4.4ns | 178MHz | 3.3V |
| ispMACH 51024VG** | 1024 | 68 | 160 | 5.0ns | 6.5ns | 3.0ns | 4.4ns | 178MHz | 3.3V |

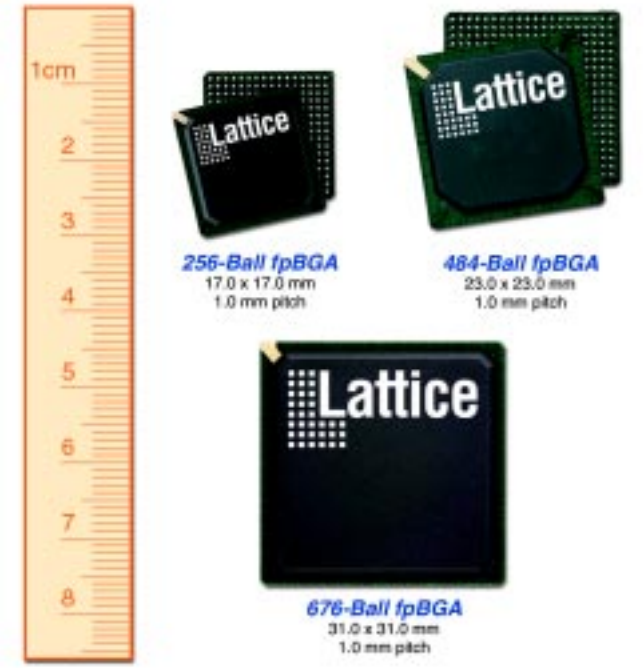
* Advance Information
** Preliminary Information

## ispMACH 5000VG and ispLSI 5000VE Family Package Options and Available I/Os

| Family Member | 128 TQFP | 272 BGA | 388 BGA | 256 fpBGA* | 388 fpBGA* | 484 fpBGA* | 676 fpBGA* |
|---|---|---|---|---|---|---|---|
| ispLSI 5128VE | 96 | – | – | – | – | – | – |
| ispLSI 5256VE | 96 | 144 | – | 144 | – | – | – |
| ispLSI 5384VE | – | 192 | – | 192 | – | – | – |
| ispLSI 5512VE | – | 192 | 256 | 192 | 256 | – | – |
| ispMACH 5768VG | – | – | – | 196 | – | 304 | – |
| ispMACH 51024VG | – | – | – | – | – | 304 | 384 |

* fpBGA = Fine Pitch BGA (1.0mm ball pitch)

## ispMACH 5000VG Advanced Packaging




*Packages are shown actual size. Dimensions refer to package body size.*

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