ispMACH 5000B

PLDs for a 64-Bit World

BFW III: The Third Generation of SuperWIDE™ PLDs with Improved Performance and Architecture

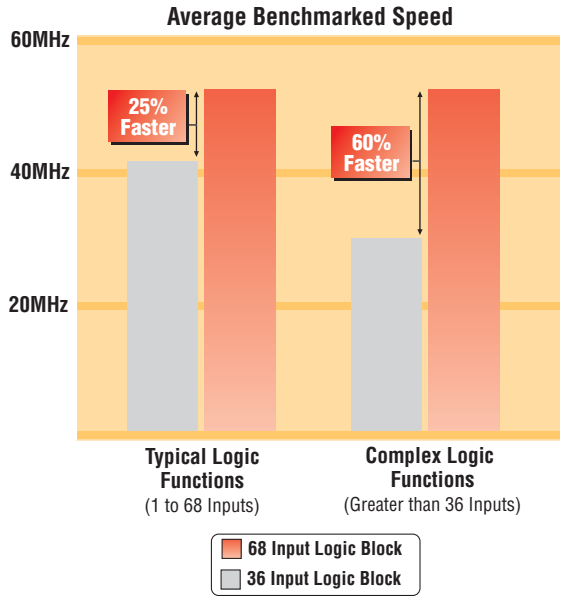
The ispMACH™ 5000B Family is the next generation of Lattice's successful SuperWIDE architecture. Through the use of an advanced technology, the ispMACH 5000B provides significantly improved speed performance, 2.5V support and superior I/O standard support (sysIO™).

The SuperWIDE logic blocks of the ispMACH 5000B Family are optimized for implementing wide functions common in 32-bit and 64-bit systems. Compared to competitive devices with narrow logic, ispMACH 5000B devices can boost performance by up to 60%!

Lattice's sysIO capability provides support for industry standards such as HSTL, SSTL, GTL+, and LVCMOS. The sysIO capability allows easy interfacing with high-speed devices supporting the latest I/O standards.

The ispMACH 5000B Family is available in a wide range of densities (128 to 512 macrocells), I/O counts (92 to 256), and advanced packaging (fpBGA and TQFP). Pin-to-pin performance up to 3.5ns and operating frequencies of 275MHz are supported.

SuperWIDE CPLDs Deliver Superior Performance!



Key Features and Benefits

- **SuperWIDE Logic Block**
  - 68 Inputs / 32 Macrocells per Logic Block
  - Up to 35 Product Terms per Output
- **High Performance**
  - 3.5 ns t_{PD} Pin-to-Pin Delay
  - 275 MHz System Performance
- **sysIO Capability**
  - LVCMOS 1.8, 2.5, 3.3 and LVTTL Support for Standard Board Interfaces
  - SSTL 2/3 Class I and II Support for DRAM Interfaces
  - HSTL Class I and III Support for SRAM Interfaces
  - GTL+ for Bus Interfaces
  - Hot-Socketing Capability
- **Multiple Device Options**
  - 128 to 512 Macrocells
  - 92 to 256 I/Os
  - TQFP, PQFP, and Fine Pitch BGA Package Options
- **Easy System Integration**
  - 2.5V Power Supply
  - IEEE 1149.1 Boundary Scan Testable
  - In-System Programmable via IEEE 1532 ISC Compliant Interface

ispMACH 5000B, 5000VG and ispLSI® 5000VE Family Attributes

Family Member	Macrocells	GLB Inputs	Product Terms per Output	Segment t_{PD}	Global t_{PD}	t_S	t_{CO}	Fmax	Vcc
ispMACH 5128B*	128	68	35	–	3.5ns	2.0ns	2.8ns	275MHz	2.5V
ispMACH 5256B*	256	68	35	–	4.0ns	2.0ns	2.8ns	250MHz	2.5V
ispMACH 5384B*	384	68	35	–	4.5ns	2.5ns	3.3ns	225MHz	2.5V
ispMACH 5512B*	512	68	35	–	5.0ns	2.8ns	3.3ns	200MHz	2.5V
ispLSI 5128VE	128	68	35	–	5.0ns	3.5ns	3.0ns	180MHz	3.3V
ispLSI 5256VE	256	68	35	–	6.0ns	4.0ns	3.0ns	165MHz	3.3V
ispLSI 5384VE	384	68	35	–	6.0ns	4.0ns	3.0ns	165MHz	3.3V
ispLSI 5512VE	512	68	35	–	6.5ns	4.5ns	3.5ns	155MHz	3.3V
ispMACH 5768VG	768	68	160	5.0ns	6.5ns	3.0ns	4.4ns	178MHz	3.3V
ispMACH 51024VG	1024	68	160	5.0ns	6.5ns	3.0ns	4.4ns	178MHz	3.3V

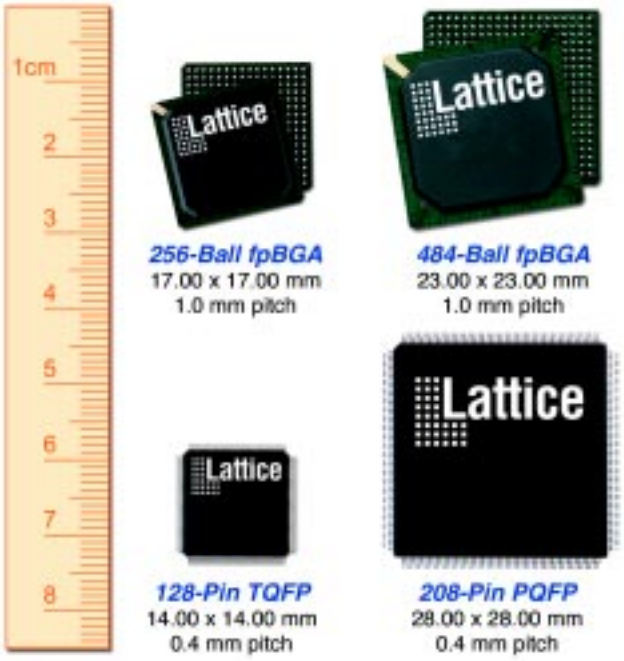
* Preliminary Information

ispMACH 5000B, 5000VG and ispLSI 5000VE Package Options and Available I/Os

Family Member	100 TQFP	128 TQFP	208 PQFP	256 fpBGA*	272 BGA	388 fpBGA*	388 BGA	484 fpBGA*	676 fpBGA*
ispMACH 5128B	–	92	–	–	–	–	–	–	–
ispMACH 5256B	–	92	144	144	–	–	–	–	–
ispMACH 5384B	–	–	156	186	–	–	–	–	–
ispMACH 5512B	–	–	156	196	–	–	–	256	–
ispLSI 5128VE	–	96	–	–	–	–	–	–	–
ispLSI 5256VE	72	96	–	144	144	–	–	–	–
ispLSI 5384VE	–	–	–	192	192	–	–	–	–
ispLSI 5512VE	–	–	–	192	192	256	256	–	–
ispMACH 5768VG	–	–	–	196	–	–	–	304	–
ispMACH 51024VG	–	–	–	–	–	–	–	304	384

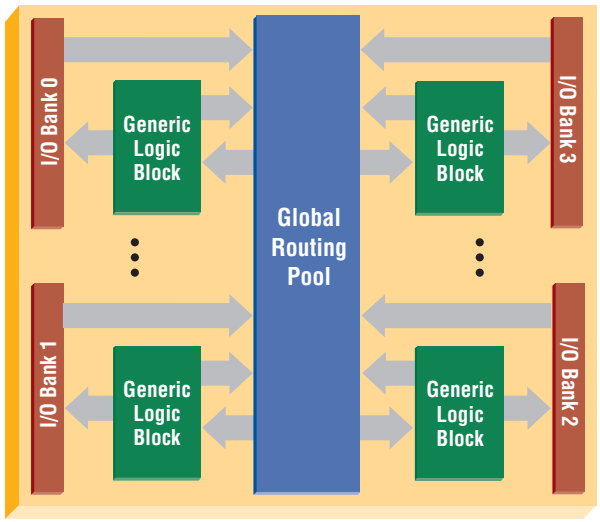
* fpBGA = Fine Pitch BGA (1.0mm ball pitch)

ispMACH 5000B Advanced Packaging



Packages are shown actual size. Dimensions refer to package body size.

ispMACH 5000B Block Diagram



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