ispLSI 5000VE

PLDs for a 64-Bit World.

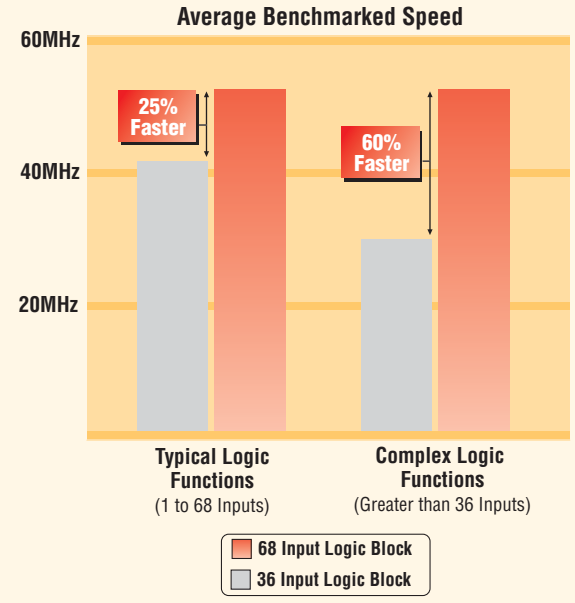
BFW II: The Next Generation of SuperWIDE PLDs is Here!

The ispLSI® 5000VE Family is the second generation of Lattice's highly successful in-system programmable BFW CPLDs. An innovative SuperWIDE architecture supports the widest logic funcions, including 64-bit applications, in a single logic level, boosting complex logic speed by up to 60%. With 32 macrocells and 68 inputs per logic block, the ispLSI 5000VE delivers optimum performance for advanced system designs. The 3.3V ispLSI 5000VE family offers 5ns Tpd, 180MHz Fmax and user selectable 3.3V/2.5V outputs.

The ispLSI 5000VE family is available in a wide range of densities, I/Os and packages. Choose from 128 to 512 macrocells and up to 256 I/Os. Advanced packaging includes space-saving TQFP, BGA and fine-pitch BGA packages.

The new ispLSI 5000VE family is fully supported by Lattice's easy-to-use and powerful ispLEVER™ design software, plus a wide range of popular third-party tools. Designing with ispLSI 5000VE devices is quick and easy using leading synthesis and simulation tools from Exemplar Logic, Model Technology, Synopsys, Synplicity, and Innoveda.

SuperWIDE CPLDs Deliver Superior Performance!



Key Features and Benefits

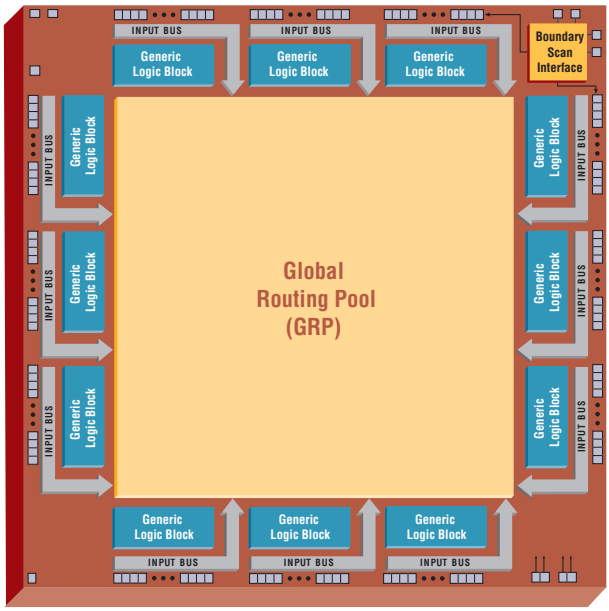
- **The Industry's Widest PLDs!**
  - SuperWIDE Logic Blocks Deliver up to 60% Performance Boost
  - Ideal for I/O Intensive Applications
- **Enhanced Generic Logic Blocks (GLB)**
  - 68 Inputs per GLB
  - 32 Macrocells per GLB
  - Up to 35 Product Terms Per Output
- **3.3V Family with 4 Members Ranging from 128 to 512 Macrocells**
- **5ns Pin-to-Pin Delay and 180MHz System Performance**
- **User Selectable 3.3V/2.5V I/O**
- **TQFP, BGA and Fine-Pitch BGA Package Options**
- **IEEE 1149.1 Boundary Scan Testable**
- **ispJTAG™ In-System Programmable**

ispLSI 5000VE Family

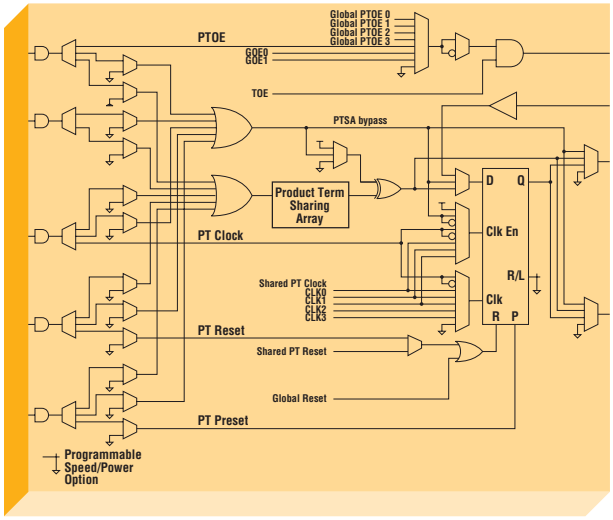
FAMILY MEMBER	MACROCELLS	SPEED: Tpd	SPEED: Fmax	Vccio	I/Os	PIN/PACKAGE
ispLSI 5128VE	128	5.0 ns	180 MHz	3.3V/2.5V	96	128-pin TQFP
ispLSI 5256VE	256	6.0 ns	165 MHz	3.3V/2.5V	72 96 144 144	100-pin TQFP 128-pin TQFP 256-ball fpBGA* 272-ball BGA
ispLSI 5384VE	384	6.0 ns	165 MHz	3.3V/2.5V	192 192	256-ball fpBGA* 272-ball BGA
ispLSI 5512VE	512	6.5 ns	155 MHz	3.3V/2.5V	192 192 256 256	256-ball fpBGA* 272-ball BGA 388-ball fpBGA* 388-ball BGA

* fpBGA = Fine Pitch BGA (1.0mm ball pitch)

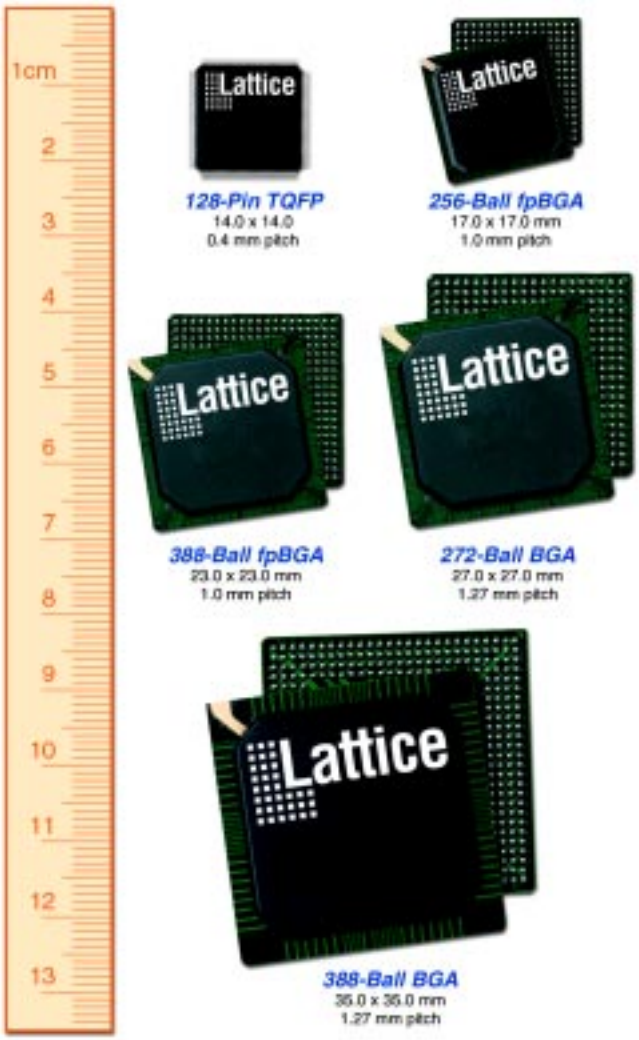
ispLSI 5000VE Block Diagram



ispLSI 5000VE Macrocell



ispLSI 5000VE Advanced Packaging



Packages are shown actual size. Dimensions refer to package body size.

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