ispLSI 2000VE

The World's Fastest PLDs. Period!

BFW II: The Next Level of PLD Performance

The ispLSI® 2000VE Family is the second generation of Lattice's highly successful in-system programmable BFW CPLDs. The ispLSI 2000VE family delivers a blazing 3ns Tpd, 300MHz Fmax and a cool 3.3V power supply. With incredibly fast 2ns Tco and 2ns Tsu performance, ispLSI 2000VE CPLDs are perfect for your most demanding applications.

The ispLSI 2000VE family is available in a wide range of densities, I/Os and packages. Choose from 32 to 192 macrocells and up to 128 I/Os. Advanced packaging includes space-saving TQFP, fine-pitch BGA, PLCC and PQFP packages. And with ispLSI 2000VE devices you can easily migrate your logic designs between different family members – saving time and money.

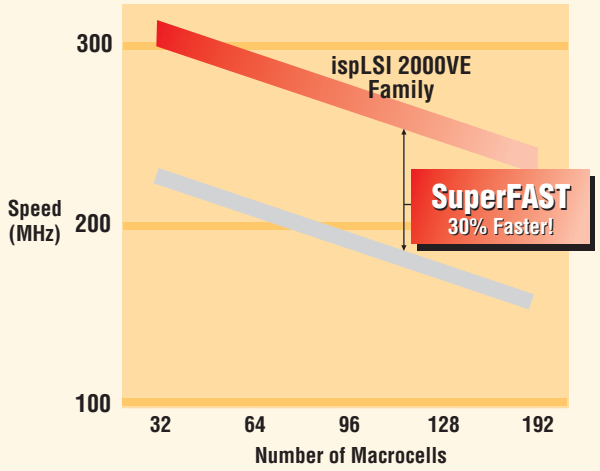
The new ispLSI 2000VE family is fully supported by Lattice's easy-to-use and powerful ispLEVER™ design software, plus a wide range of popular third-party tools. Designing with the ispLSI 2000VE is quick and easy using leading synthesis and simulation tools from Exemplar Logic, Model Technology, Synopsys, Synplicity, and Innoveda.

Key Features and Benefits

- **The Industry's Fastest PLDs at 3.0ns!**
  - 300MHz Fmax
  - 2ns Tco and 2ns Tsu
- **3.3V Family with 5 Members Ranging from 32 to 192 Macrocells**
- **PLCC, PQFP, TQFP and Fine-Pitch BGA Package Options**
- **IEEE 1149.1 Boundary Scan Testable**
- **ispJTAG™ In-System Programmable**
- **JEDEC and Pin Compatible to Original ispLSI 2000V Family**
- **Flexible Architecture**
  - Fine-Grained Logic Blocks: 18 Input/4 Output GLB
  - Enhanced Single-Level Global Routing Pool (GRP)
  - Output Routing Pool for Enhanced Pin Locking
  - Fast and Predictable CPLD Architecture

SuperFAST

Lattice ispLSI 2000VE CPLDs Deliver Exceptional Performance!



ispLSI 2000VE Family

FAMILY MEMBER	MACROCELLS	SPEED: Tpd	SPEED: Fmax	Vcc	I/O's + INPUTS	PIN/PACKAGE
ispLSI 2032VE	32	3.0 ns	300 MHz	3.3V	32 + 2 32 + 2 32 + 2 32 + 2	44-pin PLCC 44-pin TQFP 48-pin TQFP 49-ball caBGA*
ispLSI 2064VE	64	3.5 ns	280 MHz	3.3V	32 + 4 32 + 4 64 + 4 64 + 4	44-pin PLCC 44-pin TQFP 100-pin TQFP 100-ball caBGA*
ispLSI 2096VE	96	4.0 ns	250 MHz	3.3V	96 + 6	128-pin TQFP
ispLSI 2128VE	128	4.0 ns	250 MHz	3.3V	64 + 8 64 + 8 128 + 8 128 + 8 128 + 8	100-pin TQFP 100-ball caBGA* 160-pin PQFP 176-pin TQFP 208-ball fpBGA**
ispLSI 2192VE	192	4.0 ns	225 MHz	3.3V	96 + 9 96 + 12	128-pin TQFP 144-ball fpBGA**

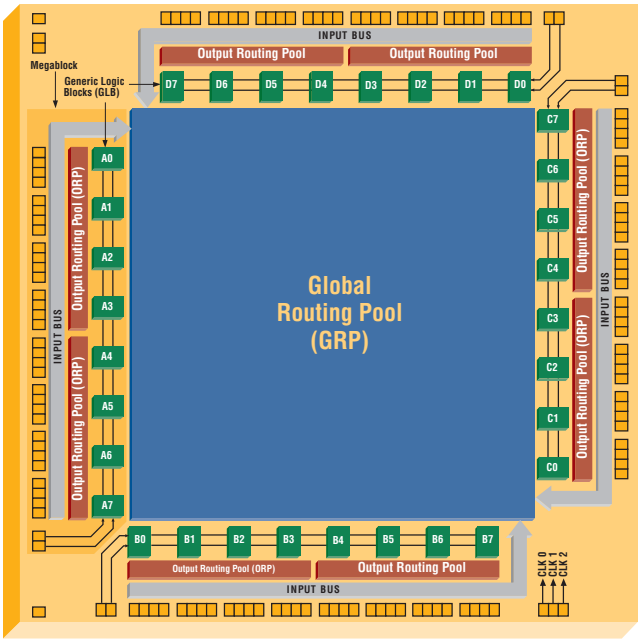
* caBGA = Chip Array BGA (0.8mm ball pitch)

** fpBGA = Fine Pitch BGA (1.0mm ball pitch)

ispLSI 2000VE Advanced Packaging

Packages are shown actual size. All dimensions refer to package body size.

ispLSI 2000VE Block Diagram



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