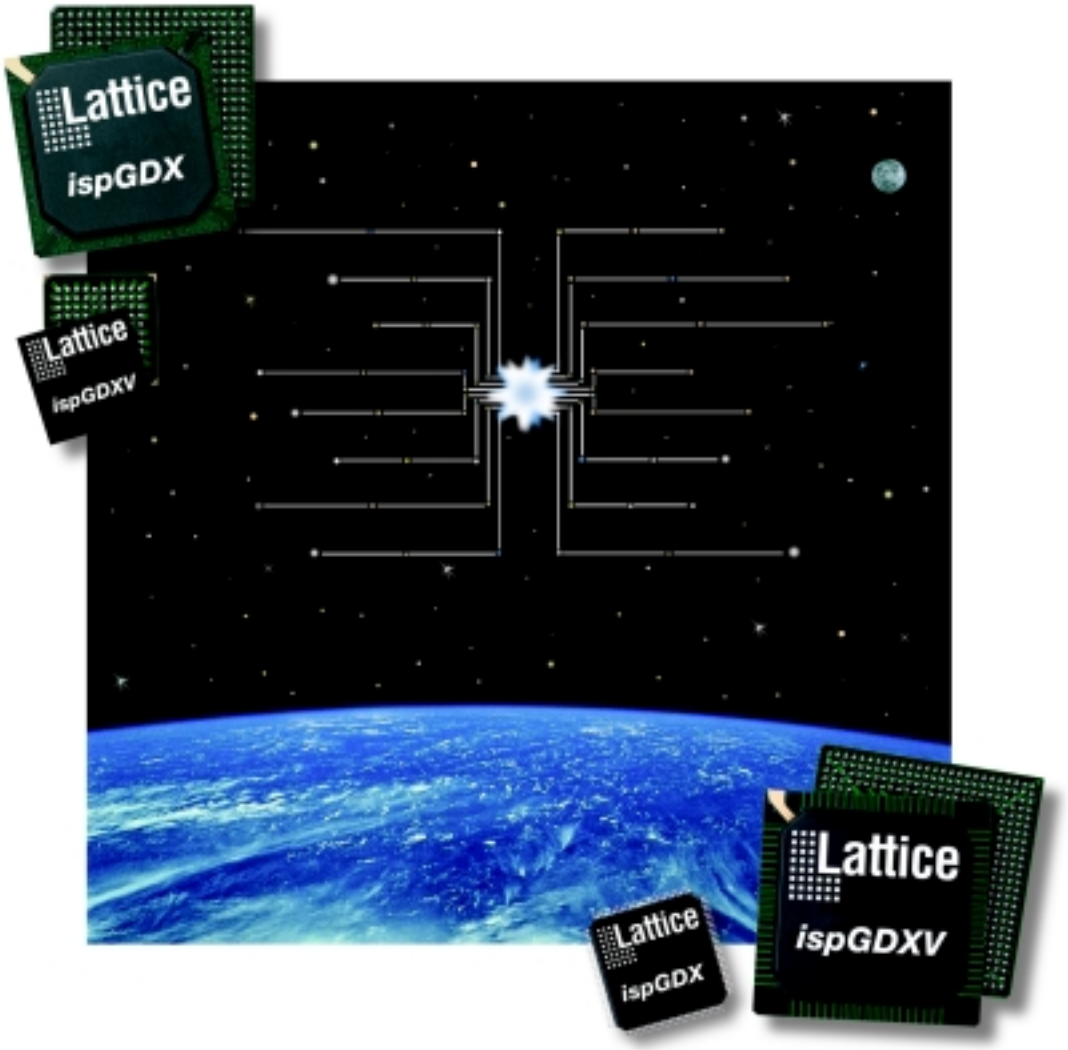


Lattice ispGDX™ Families

Generic Digital Crosspoint Devices

Lattice Semiconductor Corporation

Introducing the Revolutionary ispGDX Families

The ispGDX families are an exciting new series of in-system programmable Generic Digital Crosspoint devices from Lattice Semiconductor. Unlike traditional CPLDs and FPGAs, these families have been designed to provide unprecedented performance and flexibility for system-level signal routing and interface applications. The ispGDX architecture addresses a variety of system-level applications such as multi-port microprocessor interfaces, wide data and address bus interfaces and PCB signal routing for prototyping. It also provides in-system programmable alternatives for integration of eight- and 16-bit CMOS interface functions such as FCT components and supports high output drive for PCI and other bus interface applications. And with the introduction of the ispGDXV™ family, Lattice now supports both 3.3V and 5V system performance.

Specifications

Input-to-Output Delay (Tpd)	5ns
Clock-to-Output Delay (Tgco)	5ns
Setup Time (Tsu)	4ns
MUXsel to Output Delay (Tsel)	6.5ns
Operating Frequency (Fmax)	111MHz

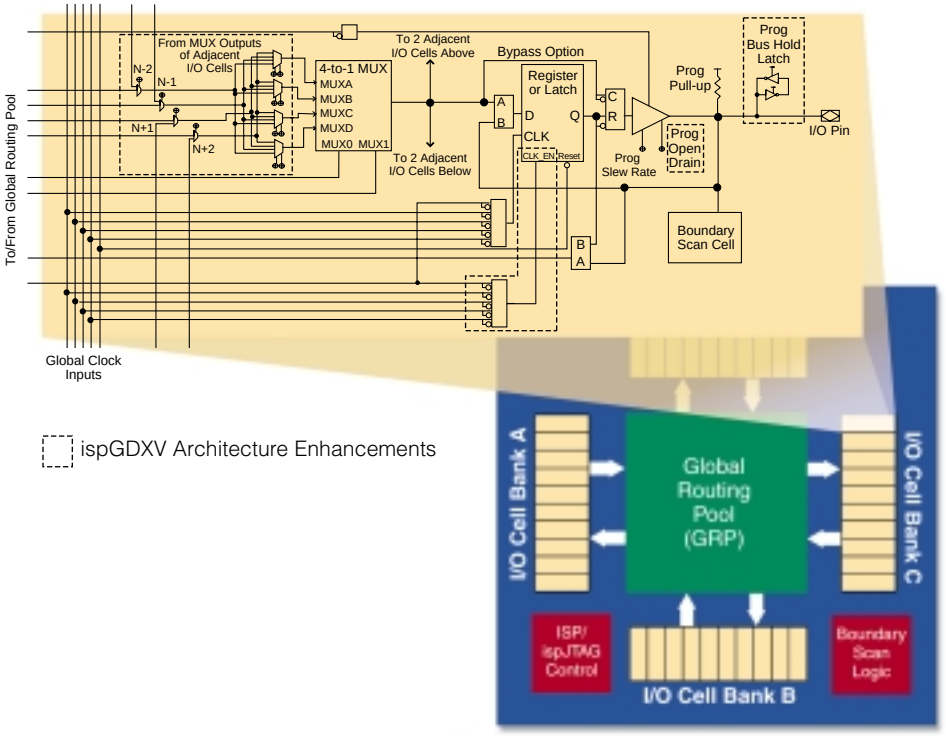
The 5V ispGDX architecture features a series of special-purpose programmable I/O cells interconnected by an E²CMOS® Global Routing Pool (GRP) that defines the basic signal paths. Inputs or outputs can be combinatorial, latched or registered, and each I/O cell has individually programmable I/O tri-state control (OE), output register/latch clock (CLK), programmable polarity and two MUX select inputs (MUXsel) which control a 4:1 multiplexer. This high-speed MUX allows the dynamic selection of up to four signal sources for a given output. Through in-system programming, each I/O pin of the ispGDX device can be driven to fixed HIGH or LOW logic levels to emulate DIP switch and jumper functions to configure PCB options.

The 3.3V ispGDXV family is the next generation in SuperSWITCHing from Lattice Semiconductor. The ispGDXV family is a functional superset of the ispGDX family, adding new features, larger I/O options and a core voltage of 3.3V.

The ispGDXV family offers a new programmable MUX width for MUX chaining and allows up to 16:1 multiplexing. Other new features include a bus hold latch, clock enable and additional slew rate options.

For maximum on-board flexibility, both families are user-selectable as Lattice ISP™ or ispJTAG™ in-system programmable and support IEEE 1149.1 Boundary Scan Test.

ispGDXV Architecture Block Diagram and I/O Cell



Features and Benefits

Feature	Benefit
High Speed	Supports Leading-Edge µP Clock Rates and Interfacing
High I/O	Integrates Dozens of Standard Bus Interface Devices
In-System Programmability	Supports Field Hardware Upgrades, Reduces Manufacturing Costs, Improves Time-to-Market
Any Pin to Any Pin Routing	No Restrictions on Signal Interconnect
High Drive (24 mA) IOL	No Need for External Buffers
High Speed Multiplexer	Supports Real Time Signal Switching
Programmable Wide MUX*	Supports from 4:1 to 16:1* MUX
Programmable I/O Cell (Combinatorial/Register/Latch)	Supports Any Mix of Standard Interface Functions and Efficient Implementation of Custom Functions
Boundary Scan Test	Enhances Board Testability, Lowers PCB Cost
Abundance of I/O Control	Supports Independent Interface Functions in a Single Device
Open-Drain Output Emulation	Supports Wired-OR Bus Structures Without Added Buffers
Output Slew Rate Control	Two Slew Rate Options for Minimizing Output Switching Noise
Fixed HIGH/LOW Outputs	Integrates Traditional Mechanical DIP Switches, While Increasing System Reliability
Bus Hold Latch*	Easy System Bus Interface Design
Clock Enable*	Offers More Logic Control for Clocking

*Available in 3.3V version only.

ispGDX Outperforms Standard Logic Functions

The ispGDX and ispGDXV devices support three similar, yet complementary classes of end-system applications: programmable data path (PDP), programmable random signal interconnect (PRSI) and programmable switch replacement (PSR).

PDP

The PDP class supports integration of system datapath (transceiver, MUX, register and latch) functions and dynamic signal routing via the fast 4:1 or 16:1 multiplexers.

Multiple standard interface components can be replaced with a single programmable ispGDX component! With the ability to program the device as necessary to perform a variety of functions, only a single part is needed in inventory. The flexibility of the unique ispGDX architecture allows more efficient implementation of special-purpose functions (such as 14-bit buses) and less wasted logic. Integrating many functions into a single ispGDX device reduces valuable PCB space, while the addition of in-system programming and Boundary Scan Test reduces time-to-market, improves system testability and decreases overall costs.

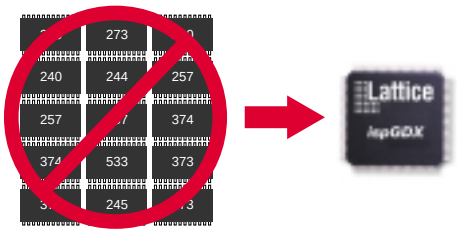
PRSI

The PRSI class includes PCB-level programmable signal routing and is characterized by the need to provide a large number of statically configured 1:1 (or 1:many) pin connections. Used in this fashion, ispGDX devices speed up prototyping by supporting flexible connectivity between major system functional blocks or between systems (for example, between a hardware emulator and test environment).

PSR

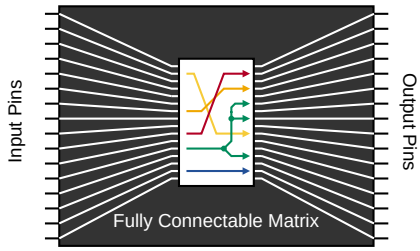
The PSR class provides a solid-state replacement for and integration of mechanical DIP switch and jumper functions. Systems commonly contain at least one DIP switch to configure PCB functions. In addition to bus interface logic, ispGDX device I/O pins can now be dedicated to DIP switch functions, providing a software-configurable replacement for mechanical DIP switches, eliminating the need to manually set DIP switches. With no moving parts, DIP switch functions are more reliable and easier to configure.

Programmable Data Path (PDP)



The ispGDX replaces dozens of discrete interface devices, reducing PCB area and switching noise.

Programmable Random Signal Interconnect (PRSI)

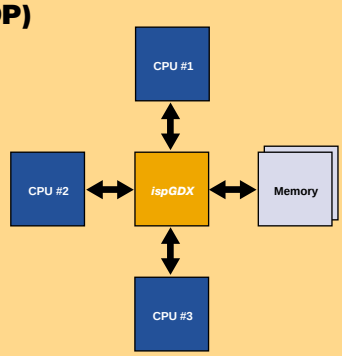


The ispGDX Global Routing Pool (GRP) is an in-system programmable wide signal switching matrix.

Programmable Switch Replacement (PSR)

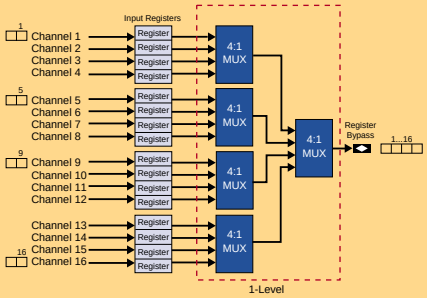
I/O pins can be used for DIP switch emulation.

Multi-Port Memory Interfaces (PDP)



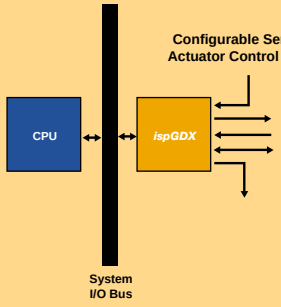
The ispGDX functions as a single chip multi-bus multiplexer.

Telecom Applications (PDP)



Multiplex 16 slow-speed channels into a single high-speed channel.

Industrial Control Applications (PRSI)



The ispGDX provides an in-system programmable signal routing device for industrial control and instrumentation applications.

ispGDX Development System

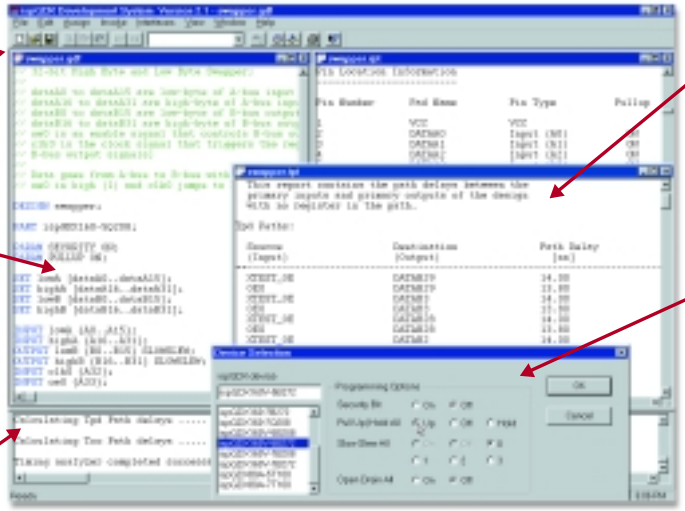
The ispGDX Development System supports ispGDX Family design entry, timing analysis, programming and timing simulation interfaces using a simple language syntax and an easy-to-use Graphical User Interface (GUI) called Design Manager. From design creation to in-system programming, the system is a user-friendly, self-contained design tool. The ispGDX Development System runs under Windows 98®, Windows 95® and Windows NT®. A command line driven version is also available to run on Sun Solaris® and HP-UX® workstations.

Once the ispGDX Design File (GDF) is entered using the compiler's built-in text editor, the compiler automatically checks the design, locates any syntax errors and provides helpful hints for their correction. The compiler process automatically generates a detailed timing report to provide accurate pin-to-pin timing information. Detailed log and report files and on-line help make design debug a snap. System-level simulation files are generated in popular output formats such as EDIF, Verilog, VHDL, Viewlogic and OrCAD.

Familiar, easy-to-use Windows GUI with drop-down menus and function icons.

ispGDX device design syntax is easy and efficient. Quickly define complex functions using powerful key word operators and dot extensions.

The log file window displays compiler operations and design information, while the report file gives detailed data useful in the debug process.

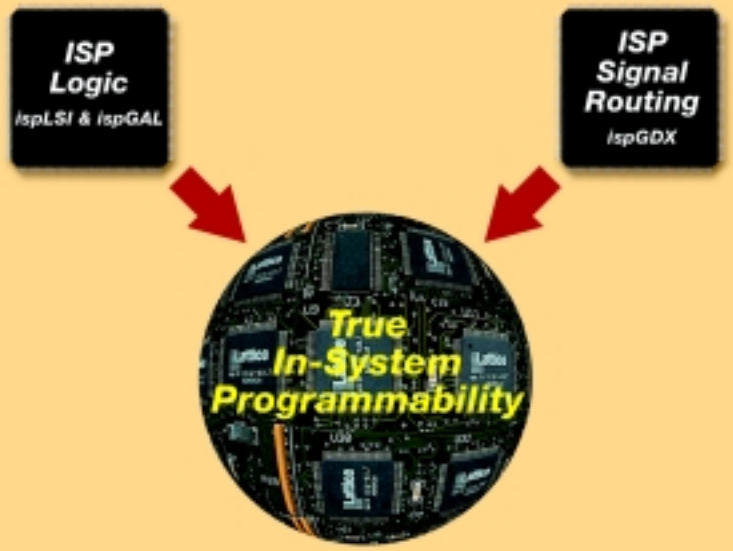


The timing report offers Tpd and Tco path delays, frequency analysis and setup/hold information.

Device selection and parameter control are quick and easy using a simple dialog box.

ispGDX: Next Generation Innovation from Lattice

- Revolutionary New ISP Device Architecture
- Delivers In-System Programmability for Bus Interface and Signal Routing
- ispGDX and ispLSI® Devices Combine for Total System Programmability
- Provides High-Performance, Unconstrained Signal Routing
- Supports 3.3V and 5V System Designs
- Supports Both Static and Dynamic Signal Selection
- Integrates Dozens of Discrete Interface Devices
- Easy-to-Use ispGDX Development System



Family Members and Features

The ispGDX and ispGDXV families include six devices ranging from 80 to 240 programmable I/O pins. These devices support input-to-output signal delays (Tpd) of 5ns, clock-to-output delays (Tgco) of 5ns and operating frequencies (Fmax) of 111MHz. Output buffers have 24mA IOL drive with individually programmable slew rate control to reduce overall ground bounce and switching noise. The devices are offered in space-saving TQFP, PQFP and BGA packages, all featuring IEEE1149.1-compliant Boundary Scan Test. These devices are manufactured using Lattice's high performance, nonvolatile E^2CMOS technology and are 100% tested and specified for 10,000 erase/reprogram cycles.

ispGDX Family Members

	ispGDX or ispGDXV Device			
	80A/V	120A	160A/V	240V
Supply Voltage	5V/3.3V	5V	5V/3.3V	3.3V
I/O Pins	80	120	160	240
Registers	80	120	160	240
I/O-OE Inputs*	20	30	40	60
I/O-Clk Inputs*	20	30	40	60
I/O-MUXsel1 Inputs*	20	30	40	60
I/O-MUXsel2 Inputs*	20	30	40	60
Dedicated Clock Pins	2	4	4	4
Boundary Scan/ISP Interface Pins	4**	4	4	4
Boundary Scan Test	Yes	Yes	Yes	Yes
Package	100 TQFP	176 TQFP 160 PQFP	208 PQFP 272 BGA 208 BGA***	388 BGA

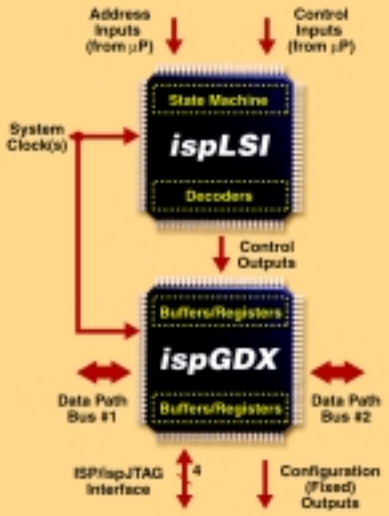
* OE, CLK, MUXsel1 and MUXsel2 can each address 25% of the I/Os.
** MUXed with I/Os.
*** Available in 3.3V versions only.

ispGDX Devices Complement High Density PLDs

...and Support Applications Traditional CPLDs and FPGAs Don't Address

The ispGDX architecture is fundamentally different from traditional High Density PLDs, with no combinatorial logic arrays on the device. The ispGDX architecture has been optimized for signal routing and buffering, providing up to 240 I/Os with 5ns pin-to-pin performance, significantly faster than comparable High Density PLDs. I/O pins can be individually programmed as control inputs or outputs to give maximum application flexibility.

The ispGDX families bring user configurability to the last bastion of "fixed function" standard logic components – signal interface devices. Lattice now offers system designers the benefits of in-system programmability for the signal routing and interface portions of their system designs.



ispGDX devices are the perfect complement to Lattice ispLSI. Use ispLSI devices for fast Control Logic and ispGDX devices for fast Datapath Logic.

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