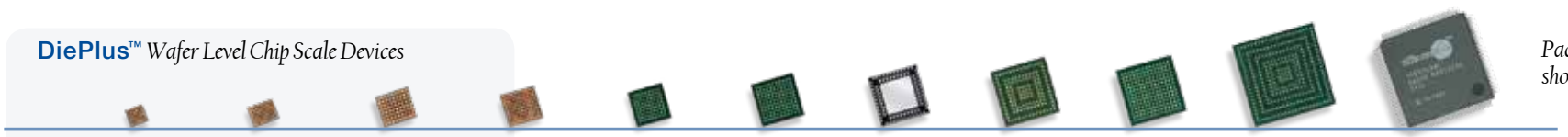
The iCE65 mobileFPGA family

	L-Series Optimized for ultra-low power applications *(1.0 Volt and 1.2 Volt Operation)*						**P-Series** Optimized for display, memory and SERDES applications *(1.2 Volt Operation)*
PART NUMBER	**L01**		**L04**		**L08**		**P04**
Logic Cells	1,280		3,520		7,680		3,520
Embedded RAM Bits	64K		80K		128K		80K
Embedded RAM 4K Blocks	16		20		32		20
Phase-Locked Loop	0		0		0		1
Power/Speed Grade (-L@1.0V, -T@1.2V)	-L	-T	-L	-T	-L	-T	-T
Core Operating Current, 0 KHz	12 µA	19 µA	26 µA	43 µA	54 µA	90 µA	43 µA
Core Operating Current, 32 KHz	15 µA	23 µA	31 µA	50 µA	62 µA	100 µA	60 µA
Core Operating Current, 32 MHz	3 mA	4 mA	7 mA	8 mA	14 mA	17 mA	9 mA
Configuration Bits	245K		533K		1,057K		533K
PACKAGE	**PROGRAMMABLE I/O: MAX I/O (LVDS CHANNELS)**						
81-ball BGA	63 (0)						
84-pin QFN	67 (0)						
100-pin VQFP	72 (0)		72 (9)				
121-pin BGA	92 (0)						95 (13)
132-ball BGA	93 (0)		95 (11)		95 (12)		
196-ball BGA			150 (18)		150 (18)		148 (18)
284-ball BGA			176 (20)		222 (25)		174 (20)
DiePlus™ (Known Good Die)	**PROGRAMMABLE I/O: MAX I/O (LVDS CHANNELS)**						
Wafer Level Chip Scale Package: WLCSP	CS36 25 (0)		CS63 48 (4)		CC72 55 (8)	CS110 92 (12)	
Bare Die	95 (0)		176 (20)		222 (25)		174 (20)

Version 1.1

DiePlus™ *Wafer Level Chip Scale Devices*



CS36	CS63	CC72	CS110	CB81	CB121	QN84	CB132	CB196	CB284	VQ100
.4 mm pitch 2.5 X 2.5 mm	.4 mm pitch 3 X 4 mm	.5 mm pitch 4 X 5 mm	.4 mm pitch 4 X 5 mm	.5 mm pitch 5 X 5 mm	.5 mm pitch 6 X 6 mm	.5 mm pitch 7 X 7 mm	.5 mm pitch 8 X 8 mm	.5 mm pitch 8 X 8 mm	.5 mm pitch 12 X 12 mm	.5 mm pitch 14 X 14 mm

Packages are shown actual size.