Enclosed are IBIS buffer models for I/O Buffers that can be programmed at various pin sites in ORCA type devices. These models make it possible to generate the unique IBIS model for any chip design that can be created in these devices. A unique IBIS model must be created for each customized ORCA design because each design contains a unique combination of I/O Buffer types at different pin locations.

In the future, software will be released to automatically generate IBIS models for each design created in ORCA Foundry. Still further plans call for ORCA Foundry to be modified to automatically create IBIS models on the fly. In the meantime, it is necessary to create your own chip level IBIS model using the procedure that follows:

First, it is important to understand the chip level IBIS format. Several examples can be found at the IBIS home page: http://www.eia.org/eig/ibis/ibis.htm. If the "Articles" link is selected, two of the Articles that give examples of chip level IBIS models are: "Practical Issues with IBIS Models" and "I/O-buffer modeling spec simplifies simulation for high-speed systems". Both of these articles give good examples for chip level IBIS models, and provide meaningful discussion on IBIS model formats, purposes, and applications.

At a top level, the IBIS model for the chip consists of a Header, a pinlist for the chip, and then an IBIS description of each I/O Buffer type used in the pinlist. The chip name should be descriptive, all lower case, 8 characters or less, and contain no special characters. The resulting IBIS file must end in the ".ibs" extension. A header format example follows, (the vertical bar "|", delineates a comment...) and should be modified for each unique design:

```
|******************************************************************
***
|
[IBIS Ver]      2.1
[File Name]     <Chip_name_goes_here>.ibs
[File Rev]      <numeric.numeric>
[Date]          <Month Day, Year>
[Source]        Original from Lucent Technologies, an example IBIS file.
[Notes]         This includes IBIS Version 2.1 features to illustrate a
                top level IBIS design.
[Disclaimer]    This information is for modeling purposes only, and
                is not guaranteed.
[Copyright]     None
|
|******************************************************************
***
|
[Component]     <Chip_name_goes_here>
[Manufacturer]  Lucent Technologies
[Package]
| variable       typ                 min                 max
R_pkg            0.1600              0.1600              0.1600
L_pkg           12.0000nH           10.0000nH           14.0000nH
C_pkg            0.5000pF            0.5000pF            0.5000pF
|
|******************************************************************
***
```

The Source, Notes, Disclaimer, and Copyright fields may be filled in with any text that best serves the ORCA user and their corporation. The Resistance, Inductance and Capacitance values for the package (R_pkg, L_pkg, and C_pkg respectively) given in the example are typical

values. The exact values for a given package type are available in the "Package Information" chapter of the ORCA data book.

The header information is then followed by a pinlist that indicates the Pin number, the signal name (pin name) that has been selected for that pin number, and finally by the type of ORCA buffer that has been placed at that pin. Three additional fields are provided for the Resistance, Inductance and Capacitance of each pin. These are best left blank for now. An example pinlist follows:

```
|
|*********************************************************************
*
|          Example Pinlist
|*********************************************************************
*
|
[Pin]  signal_name          model_name           R_pin     L_pin
C_pin
1      VSS                  GND
2      VDD                  POWER
3      CLK                  IBMPU
4      PIF_DATA_0           IBM
5      PIF_DATA_1           IBM
6      PIF_DATA_2           IBM
7      PIF_DATA_3           IBM
8      PIF_DATA_4           IBM
9      PIF_DATA_5           IBM
10     PIF_DATA_6           IBM
11     PIF_DATA_7           IBM
12     VDD                  POWER
13     PIF_FULL_N_OUT       OB6
14     PIF_EN_N_OUT         OB6
15     PIF_SOC_OUT          BMZ12FPU
16     PIF_DATA_8           IBM
17     PIF_DATA_9           IBM
18     PIF_DATA_10          IBM
19     PIF_DATA_11          IBM
20     PIF_DATA_12          IBM
21     VSS                  GND
22     PIF_DATA_13          IBM
23     PIF_DATA_14          IBM
24     PIF_DATA_15          IBM
25     PIF_FULL_N_1         IBMPU
26     VDD                  POWER
27     PIF_EN_N_1           IBMPU
28     PIF_SOC_1            IBMPD
29     PHY_DATA_0           IBT
30     PHY_DATA_1           IBT
31     VSS                  GND
32     PHY_DATA_2           IBT
33     PHY_DATA_3           IBT
34     PHY_DATA_4           IBT
35     PHY_DATA_5           IBT
36     PHY_DATA_6           IBT
37     PHY_DATA_7           IBT
38     PHY_FULL_N_OUT       OB6
39     PHY_EN_N_OUT         OB6
40     VDD                  POWER
41     PHY_SOC_OUT          BTZ12FPU
42     PHY_DATA_8           IBT
43     PHY_DATA_9           IBT
```

```
44      PHY_DATA_10          IBT
45      PHY_DATA_11          IBT
46      PHY_DATA_12          IBT
47      PHY_DATA_13          IBT
48      PHY_DATA_14          IBT
49      PHY_DATA_15          IBT
50      PHY_FULL_N_1         IBTPU
51      VSS                  GND
53      VSS                  GND
54      VSS                  GND
55      PHY_EN_N_1           IBTPU
56      PHY_SOC_1            IBTPD
|
|*************************************************************************
*
|          The Example Pinlist would continue past this point
|*************************************************************************
*
|
```

Note that the Model name given for VDD and VSS are reserved names, specifically POWER and GND (respectively). All other Model names are the names given for the ORCA buffers used in this design. In this case, the example design uses the IBMPU, IBM, OB6, BMZ12FPU, IBMPD, IBT, BTZ12FPU, IBTPU, and IBTPD buffer types. These, then, are the buffer model files that must be included in the lines following the pinlist in the design.

The files containing these buffer models are labeled according to the buffer models they define. Only the buffer models that are used must be included in the chip level IBIS model. Others may be present and unused, but will be taking up a lot of unnecessary disk space if all of the ORCA IBIS buffer models are included.

The best way to generate a pinlist for a given ORCA design is to use the ..PAD file that is generated during PAR (Place And Route). The third, "LOCATED" field, should be replaced with the type of the ORCA buffer used at that pin as shown above. Power and Ground pins may be added as found in the data book (and given as gaps, missing in the pin sequence). Dedicated pins, and pins not used in the design may be simply omitted from the list (Note that pin #52, the dedicated CCLK pin, is missing from the above list).