ispMACH™ 5000VG ISP™ CPLD Architecture Key Fact Sheet

Summary: Engineers continually strive to improve system performance, time-to-market, and integration. The ispMACH 5000VG family provides them with a new programmable solution to meet these challenges. This third generation SuperWIDE™ architecture increases system level integration through the provision of sysIO™ advanced I/O support, sysCLOCK™ PLLs, and SuperBIG™ logic capacities of up to 1024 macrocells. This system level integration capability is coupled with the traditional CPLD characteristics of high performance, ease-of-design, and instant availability of logic at power-up.

Features	Benefits
System Level Integration	
• **sysIO Capability** - LVCMOS (1.8, 2.5, 3.3), LVTTL - SSTL, HSTL, CTT - PCI, GTL+, AGP - LVDS, LVPECL (Clock inputs) - Programmable Drive Strength • **sysCLOCK Phase Locked Loops (PLLs)** - Two on-chip sysCLOCK PLLs - Multiply/Divide from 1-32 - Frequency range 5-180 MHz - Shift clock +/- 3.5ns in 500ps steps • **SuperBIG Architecture** - Initial devices up to 1024 macrocells - Up to 384 I/O	• **Get Signals On and Off Chip At High Speed** - Chip-to-chip interfaces - Chip-to-memory interfaces - Chip-to-backplane drivers - Clock distribution - Elimination of series termination resistors • **Improves High Speed System Performance** - Manage multiple clock domains - Synthesize new clocks - Supports wide range of applications - Improve set-up and clock-to-out times • **Allows High Logic Capacity With CPLD Characteristics** - Reduced system part count - Supports I/O requirements of complex functions
High Speed Performance	
• **High Performance Silicon** - 5ns pin-to-pin delay - 178MHz operating frequency (f_{MAX}) • **SuperWIDE Logic Blocks** - 68 inputs to logic blocks - Up to 160 product terms per output	• **Raw Speed Performance** - Implement high-speed combinatorial functions - Implement high-speed registered functions • **Increased System Speed Performance** - Up to 60% performance increase over traditional CPLDs - Up to 25% performance increase over traditional CPLDs
CPLD Ease-Of-Use	
• **Predictable Deterministic Timing** • **"Instant" Logic Availability At Power-Up** • **IEEE 1532 In-System Programming (ISP)** • **IEEE 1149.1 Boundary Scan Test** • **Flexible Logic** • **ispLEVER™ Design Tool Support**	• **Simple Design Verification** • **Simplifies Design, Supports System Boot-up** • **Fast Debug, In-Field Changes, & Reduced Costs** • **Improve System Test** • **Matches A Variety Of HDL Coding Styles** • **Single Design Tool For All Lattice Logic Products**