Management Considerations for In-System Programmable PLDs

ISP: The Lattice Revolution

Lattice ISP™ PLDs, first introduced in 1992, have revolutionized the world of programmable logic by dramatically reducing time-to-market and production costs and enabling systems to be upgraded in the field. With Lattice ISP PLDs, there is no need for stand-alone device programmers. No need for programmed device inventories. No need for complex manufacturing flows. No need for expensive field updates.

Design Benefits of ISP:

- Faster Time-to-Market
- Simplified System Prototyping
- Improved Device and Board Level Testability

Manufacturing Benefits of ISP:

- Reduced Manufacturing Costs
- Substantial Inventory Reductions
- Lower Procurement Costs
- Painless Code Changes on the Manufacturing Floor
- Reduced Re-Work Costs
- Improved System Quality and Reliability

Field Service/Support Benefits of ISP:

- Easy Field Reconfiguration or Customization
- Cost Effective Remote Upgrade and Repair

Lattice ISP PLDs enable designers to define and develop systems based on reconfigurable hardware. Lattice ISP PLDs make hardware as flexible and easy to modify as software so system prototyping and debugging is fast and easy. Lattice ISP PLDs also streamline the system manufacturing flow by reducing the number of unique components needed and by integrating all device programming steps into final production board test. This reduces the complexity and cost of each system while manufacturing flexibility is increased.

With Lattice ISP PLDs, benefits are realized even after systems have been shipped: field hardware upgrades become as easy and inexpensive as sending a disk to the end customer or downloading a new hardware configuration via modem.

While Lattice is the leading supplier of in-system programmable PLDs with well over 90% market share, virtually every vendor of CPLD products has now followed the Lattice lead and is introducing their first generation of in-system programmable products.

The benefits of Lattice ISP PLDs are very tangible and system designers are not only taking advantage of them, but are demanding this capability in every PLD they use. It therefore comes as no surprise that all major CPLD vendors now claim to offer an in-system programmable solution comparable to that of Lattice.

The issue is that these other CPLD vendors offer immature and incomplete solutions. Limited silicon offerings, primitive manufacturing software support and a general lack of experience in in-system programmable PLD technology result in risk-prone, unproven solutions at best. Just as not all suppliers of design tools are the same, not all in-system programmable solutions are the same.

The following analysis will compare the Lattice ISP solution to that of other in-system programmable CPLD solutions beginning to be offered by Altera and Xilinx. The executive summary shown below and the supporting back-up analysis contained in the balance of this paper compare these solutions in several critical areas:

	Lattice	Altera	Xilinx
Device Support	31	8	5
Pin-Locking	Leader	3rd	2nd
JTAG Programmable Devices	14	8	4
Program/Erase Time	< 20 Sec.	> 60 Sec.	> 60 Sec.
Turbo Programming	YES	NO	NO
ATE Support	ALL	NO	HP Only
Field Upgrade Capability	YES	NO	NO
Proven Mfg. Experience (Units)	> 15MM	<< 1MM	<< 1MM

Figure 1. In-System Programmable Device Suppliers

	LATTICE	ALTERA	XILINX
Number of 5 Volt In-System Programmable Families	8: ispLSI® 1000, 1000E, 2000, 3000, 6000, ispGDS™, ispGDX™, ispGAL®	2: MAX 7000S, 9000	1: XC9500
Number of True 3.3 Volt In-System Programmable Device Families	1: ispLSI 2000V	None	None
Number of In-System Programmable Devices Shipped in TQFP/SSOP Packages	16	3	3
Density Range (Logic Gates)	650 - 25,000	600 - 12,000	800 - 12,800
1st Introduction	1992	1995	1996

Lattice ISP Product Breadth/Support

Lattice has shipped over 15 Million ISP PLDs since the 1992 introduction of the ispLSI 1000 Family and currently serves over 90% of the in-system programmable PLD market.

No other in-system programmable vendor offers a breadth of product close to that of Lattice's (See Figure 1). Lattice provides both 5 Volt and 3.3 Volt ISP PLD products ranging from 20-pin, ISP signal routing switches (ispGDS™) and 28-pin, 650 gate 22V10 architectures (ispGAL22V10) to 304-pin, 20,000 gate CPLDs (ispLSI 3448), all the way up to 25,000 gate CPLDs containing dedicated Memory and Register/Counter Function Blocks (ispLSI 6192). Lattice offers over 31 ISP devices, all available today.

All of these high-performance Lattice ISP products can be incorporated easily onto system circuit boards, performing a wide variety of system-level functions with the ability to be programmed and reprogrammed via a single 4- or 5-wire ISP interface.

Design Tools

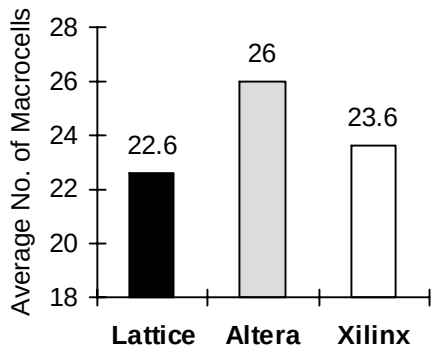
In order to keep up with continually changing market conditions and shorter product life cycles, engineers must improve their productivity wherever possible. One of the emerging methodologies is the use of Hardware Description Languages (HDL) such as VHDL and Verilog-HDL for high-level design. When combined with Lattice's efficient HDL synthesis and logic fitter tools, system designers can define logic targeted for in-system programmable high-density PLDs quickly and easily.

Lattice software provides demonstrably better device utilization and speed when used in an HDL design environment as compared to competitive approaches. In order to benchmark this point, an HDL synthesis benchmark evaluation was performed using the PREP benchmark circuits. The benchmark results clearly show Lattice as the optimum solution. For a complete copy of this analysis, see Benchmarking HDL Programmable Logic Solutions (Lattice Document #I0079).

These benchmarks compared the results obtained using Lattice's ispLSI 2128-100LT with Altera's MAX7128SQC160-10 and Xilinx's XC95144-10PQ160, all 10ns Tpd devices. The benchmark study evaluated the nine PREP benchmark functions which include Data Path, Timer/Counter, Small State Machine, Large State Machine, Arithmetic, Accumulator, Binary Counter, Pre-Scaled Counter, and Memory Map. Each design was synthesized with various CAE vendor tools.

Utilization for each device was compared by looking at the average number of macrocells required to implement each benchmark circuit. The results show that Lattice produces the most efficient logic utilization of any vendor (See Figure 2). The Altera and Xilinx solutions produced results which use 30.6% and 9.3% more macrocells respectively than Lattice to implement the same logic functions. That means that Lattice users obtain higher density and greater value for every device dollar.

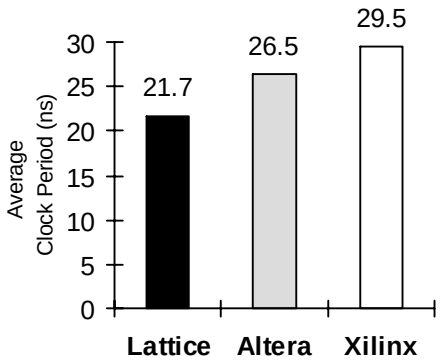
Figure 2. Average Number of Macrocells Required to Implement Each PREP Benchmark



After utilization was compared, speed for the three devices was evaluated using the same nine benchmark circuits. The performance results below illustrate the average clock period achieved across all synthesis tools for each of the benchmark functions.

Figure 3 shows that Lattice again produces superior results. In fact, the average PREP benchmark in the Lattice ispLSI device performed 20% faster than the Altera device and 34.5% faster than the Xilinx device. Even though the Lattice, Altera and Xilinx devices evaluated have comparable data sheet performance specifications of 10ns Tpd and Fmax of 100MHz, the combination of Lattice's CPLD architecture and HDL Synthesis-Optimized design flow produced, on average, 20% higher performance than Altera and nearly 35% higher system performance than that of Xilinx.

Figure 3. Average Clock Period of Single Instance of Each PREP Benchmark



Pin-Locking

The ability to modify the logic device after it has been soldered to the circuit board is certainly a key capability for any in-system programmable PLD. Device architectures which possess the resources to accommodate changes in logic or additions of incremental logic without changing the original pin assignments are valuable to the system designer.

To explore this issue further, the pin-locking performance of equivalent sized in-system programmable PLDs from Lattice and Xilinx were evaluated using three "real world" PLD designs. The Xilinx device was chosen because of this vendor's claims that their devices have 100% pin-locking capability. In reality this claim is false: the Xilinx XC9500 family's pin-locking capability is neither close to 100%, as is being promoted in the marketplace, nor as good as Lattice's current generation ispLSI families of ISP CPLDs.

This pin-locking evaluation was performed with XACT-ABEL software and compares the Xilinx XC95108 to the closest comparable gate-density and pin count Lattice ispLSI device, the ispLSI 1032E.

The designs consisted of a multiplexer circuit with registered outputs and output enables, a sequential logic circuit with buffered registers and a microprocessor peripheral circuit with a timer and memory management unit. These designs were chosen due to their high I/O utilization which generally creates problems with any device's ability to route signals to a fixed pin out. All the designs fit into both devices with unlocked pins. (See Figure 4 for further explanation of the I/O pins).

Figure 4: Designs Evaluated

Design	Pins			
	Input	Output	Bi-directional	Total
#1	36	1	30	67
#2	29	13	13	55
#3	34	24	0	58

Each design was assigned 10 arbitrary pin configurations. (See Lattice ispLSI vs. Xilinx XC9500 Pin-Locking Evaluation TT#2024 for further explanation).

Comparing the results of the 30 different design and configuration combinations for each device clearly shows that Lattice ispLSI has the advantage. Only 6 of 30 routes were successful with the Xilinx XC95108, while 28 of 30 were routed with the Lattice ispLSI 1032E. Figure 5 summarizes the results and shows the number of configurations for each design which were successful.

Figure 5: Summary of Results

Design	Xilinx 95108	Lattice 1032E
#1	2	8
#2	2	10
#3	2	10
Total Successes	6	28
% of Total Tests	20%	93%

Analyzing designs 1, 2 and 3 shows that they have similarities in their logic. All unplaced signals for the Xilinx architecture are part of output or bi-directional

buses after the input pins have been locked. The only conclusion one can draw from the above design implementations is that the input and pin feedback of the Xilinx 9500 devices does NOT support 100% pin-locking.

On the input and bi-directional pin feedbacks, the switch matrix does not provide a 100% signal interconnect, therefore locking the input pins in a sequential order restricts the software so that the pin feedback of the bi-directional pins is difficult to place. The locked input pins also caused output pin placement problems. On these commonly used user functions, the Xilinx architecture consistently shows its limitations in routing resources and pin-locking capabilities.

Conversely, the output routing pool (ORP) and product term sharing array (PTSA) in Lattice's ispLSI architecture greatly increases the device's pin-locking capability: The ispLSI architecture from Lattice offers superior pin-locking performance over other suppliers.

Device Performance

Another issue to consider is raw device performance. With most vendors claiming to offer comparable performance options, it should be noted that they are not all equal. For instance take Xilinx and Lattice who both market a high-performance, 44-pin in-system programmable PLD. Xilinx offers their 5.0ns (Tpd), 36 macrocell XC9536-5 and Lattice offers the 5.0ns (Tpd), 32 macrocell ispLSI 2032-180.

Figure 6: 16-Bit Bus Data Path

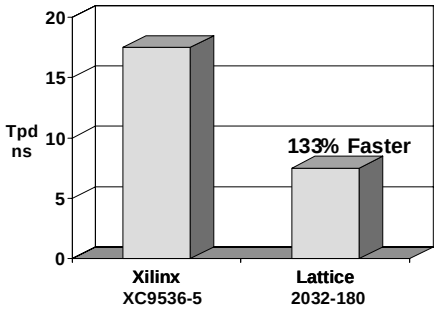


Figure 7: 8-Bit Parity Generator

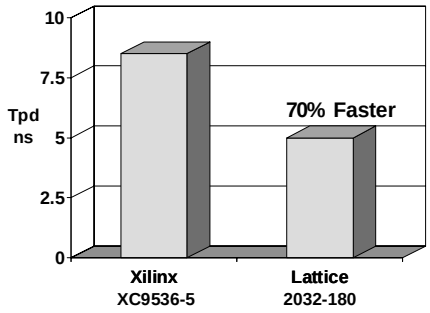
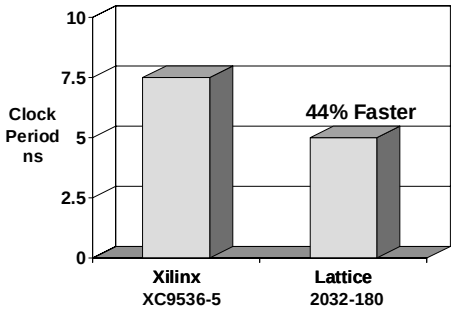


Figure 8: Clock Divider (Divide By 2)



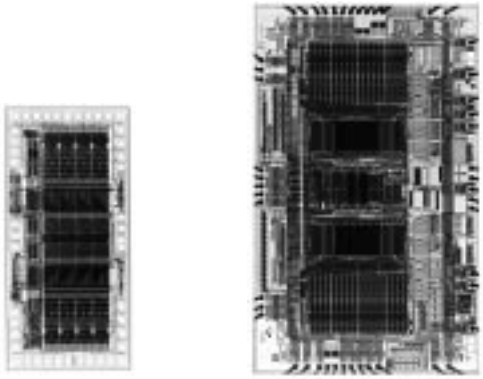
From a data sheet perspective, one would expect these devices to operate at roughly the same performance levels, however, actual implementation of 3 common benchmark functions (16-bit Bus Data Path, 8-bit Parity Generator and a Divide-by-2 Clock Divider) shows Lattice to be anywhere from 44% to 133% faster than Xilinx. The results of these three performance benchmarks are shown in figures 6, 7 and 8 above.

As can be seen not all devices which claim to have equivalent system performance in fact do. Architectural differences between vendors such as routing capabilities and feedback speeds contribute to the differences in true device performance. Lattice ispLSI CPLDs deliver true high-performance while the other vendors haven't proven this.

Technology

Device die size, which ultimately drives device cost, must always be taken into account when evaluating an in-system programmable PLD. Currently there are two technologies used in implementing in-system programmable PLDs: Electrically Erasable (E^2) PROM and Flash. E^2CMOS® ISP PLDs were pioneered by Lattice and have been in production for over 5 years, while Flash in-system programmable PLDs are a recent entrant into this market.

Figure 9: E^2CMOS vs Flash PLD Die Size



Lattice
ispLSI 2032

Xilinx
XC9536

Figure 10: JTAG Programmable Products

	LATTICE	ALTERA	XILINX
JTAG Programmable Families	4: ispLSI 2000V, 3000, 6000, ispGDX	2: MAX 7000S, 9000	1: XC9500
JTAG Programmable Devices in Production	14	8	4
JTAG Testable Families	3: ispLSI 3000, 6000, ispGDX	2: MAX 7000S, 9000	1: XC9500
# of JTAG Testable Devices in Production	11	8	4

Flash-based in-system programmable PLDs contain numerous short comings when compared to E^2CMOS solutions. Flash PLDs require higher programming currents (Up to 10^5x higher) and larger programming transistors and voltage pumps which require larger programming circuitry to operate. This larger programming circuitry and other factors ultimately result in die sizes up to 2x that of the equivalent E^2CMOS device (See Figure 9). Additionally, Flash is an extremely complex (double-polysilicon) process technology which presents numerous problems when used for in-system programming including potential reliability issues such as long term data retention and programming endurance.

In addition, Flash is still very "immature" with less that 1 year of production experience for in-system programmable PLDs. Only Lattice can provide a proven reliable solution with over 5 years of ISP production experience, over 15 million ISP devices shipped, and over 500 million E^2CMOS PLDs shipped.

JTAG Programming Interface

Designs which implement JTAG test (package/board continuity) as part of their manufacturing flow, should look to Lattice for the broadest families of JTAG testable and programmable devices in the industry. Lattice has three families of CPLDs which support JTAG programming (ispLSI 2000V, 3000 and 6000) along with the ispGDX family of Generic Digital Crosspoint devices. The ispLSI 3000, 6000 and ispGDX families are actually configurable to support either the standard Lattice ISP protocol or the ispJTAG™ interface. Lattice has also developed programming software (ispDOWNLOAD™) which enables all Lattice ISP products to co-exist in the same chain independent of which programming protocol is used.

In fact, the truth is that there is no JTAG programming standard established in the industry today. All JTAG programming implementations are vendor specific and completely unique. Vendor specific programming cycles for each vendor's devices will be required. The effort to establish a JTAG programming standard, while underway, may take a number of years to develop. In the mean time, Lattice offers the most complete in-system programmable solution in the industry whether utilizing Lattice's ISP or ispJTAG protocol.

Refer to Figure 10 which shows the product breadth of the three major PLD vendors in the JTAG programmable market.

Manufacturing Considerations

Programming methodologies vary from vendor to vendor but only Lattice supplies a complete in-system programming solution. Lattice devices support more programming options than any other vendor, from programming a few devices on a PC or workstation to programming production volumes on ATE equipment.

Lattice supports programming with all major ATE manufacturers (HP, Teradyne, GenRad and others) and has had hundreds of customers implement this time saving programming and test methodology. As the only vendor offering a comprehensive ATE vector creation utility (ispATE™), Lattice can support any ATE programming and test needs.

Figure 11: ATE Competitive Listing

	Lattice	Altera	Xilinx
ATE Support	All ATE Vendors	NO	HP Only
Parallel (Turbo) Programming	YES	NO	NO
MicroP Programming	YES	NO	NO
PC/WS Programming	YES	YES	YES

Figure 12: Programming Times

Program Time	LATTICE	ALTERA	XILINX
Erase/Program Time	< 20 seconds (All Devices)	> 60 seconds (All Devices)	> 60 seconds (All Devices)

Vendors such as Altera and Xilinx do not offer comparable ATE support (See Figure 11 for a Competitive Listing). For example Lattice is the only vendor to offer microprocessor programming. By programming via the microprocessor, expensive ATE test time can be saved and future field upgrades can be handled seamlessly with little or no effort. These advantages again save additional time and money as compared to other solutions.

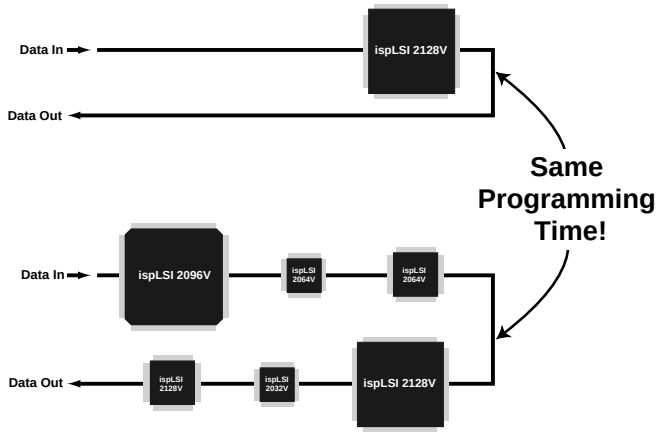
A limiting factor when programming a Xilinx device is the fact that it requires twice as many programming vectors as the equivalent gate-density Lattice ispLSI device. Doubling the number of programming vectors drastically increases the amount of ATE time required, thus costing more time and money.

Lattice provides all of the tools required to fully implement a design and program from any PC, Workstation or ATE.

Lattice is the only vendor which can support erase/programming times of less than 20 seconds. Altera and Xilinx require at least 3 times as long to erase/program their devices. Refer to Figure 12 for a complete listing of competitive programming times. At any gate-density level Lattice ispLSI devices will program faster that the competition. This time savings reduces overall manufacturing costs.

In addition to the ispATE and ispDOWNLOAD tools available, Lattice also allows up to 100 devices to be programmed in a single chain in parallel such that multiple devices can now be programmed in the same time that it takes to program a single device. Parallel programming (Turbo ispDOWNLOAD) is yet another way that Lattice ispLSI products save time and money.

Figure 13: Lattice Parallel Programming



Looking to the future, all new ISP CPLD product designs from Lattice are committed to offer even faster programming times, thus making the economics of programming ISP devices on expensive ATE equipment even more attractive.

Field Upgrades

Today, field upgrades are primarily performed with a microprocessor based download. For example, new hardware configurations can be transmitted via modem (Telecom network applications) to existing systems in the field. ispCODE™ is a free uncompiled C-Based version of Lattice's ispDOWNLOAD routines. ispCODE can be easily integrated into the system's on board processor's microcode to control the in-system programming of Lattice ISP devices.

With Lattice ISP devices, field upgrades simply require the receipt of new device programs. These new programs can be delivered to the end system easily and inexpensively by methods ranging from the mailing of a floppy disk to transferring the data via modem. Changes can update system features such as memory configurations, communication protocols and microprocessor clock rates without removing the printed circuit board from the system. No other vendor allows for such real-time upgradability.

Pricing

Lattice is the most competitive in-system programmable PLD vendor from a long-term, component cost perspective. 12 years of E^2CMOS experience and advanced fabrication technologies allow Lattice to be the leader in cost-effective PLDs today and into the future. Lattice's commitment to its ISP products is readily demonstrated by its "ISP is FREE" program which offers its in-system programmable devices at the same price as traditionally programmed PLDs. To further evaluate the cost savings which can be associated with Lattice ISP refer to the ISP Cost-of-Ownership Analysis (Document #I0056).

Lattice ISP

Only Lattice offers the Total ISP solution with a track record other PLD suppliers can't match.

- Pioneer of ISP Devices
- > 15MU Shipped
- 31 Silicon Solutions Available Today
- Space-Saving TQFP Packaging
- 5V and 3.3V ISP Solutions
- Hundreds of Man-Years Experience Making ISP a Practical Reality
- Superior ispVHDL Software Support
- Flexible Pin-Locking
- The Best System-Level Performance
- JTAG Test and Programming
- ATE Support for All Major Vendors
- Faster Program/Erase Times
- Support for Field Upgrades

Conclusion

The future of CPLDs is inextricably linked to in-system programmability. With analysts predicting that 50% of the total CPLD market will be using in-system programmable devices by the year 2000. As the market grows Lattice will remain committed to providing world class ISP product support. **There is only one vendor who can provide a Total ISP solution - Lattice Semiconductor Corporation.**

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Order #: I0080