Introduction to ispMACH 5000 Family

October 2002

Introduction

The ispMACH™ 5000 product families represent the next generation of Lattice's SuperWIDE™ CPLD architecture. Through their wide 68-input blocks, these devices give significantly improved speed performance for typical designs over architectures with a lower number of inputs.

The ispMACH 5000VG takes the unique benefits of the SuperWIDE architecture and extends it to higher densities referred to as SuperBIG™, by using the combination of an innovative product term architecture and a two- tiered hierarchical routing architecture. Additionally, sysCLOCK™ and sysIO™ capabilities have been added to maximize system-level performance and integration.

The ispMACH 5000B enhances the SuperWIDE product lines, which include ispLSI® 5000VA, 5000VE, and ispMACH 5000VG, with improved performance, sysIO capability and 2.5V support. The ispMACH 5000B family provides logic designers with a single architecture to meet a broad range of system requirements.

ispMACH 5000VG Family

- **High Density**
  - 768 to 1,024 macrocells
  - 196 to 384 I/Os

- **sysCLOCK PLL – Timing Control**
  - Multiply and divide factors between 1 and 32
  - Clock shifting capability ± 3.5ns in 500ps steps
  - Multiple output frequencies
  - External feedback capability for board-level clock deskew
  - LVDS/LVPECL clock input capability

- **High Speed Logic Implementation**
  - SuperWIDE 68-input logic block
  - Up to 160 product terms per output
  - Hierarchical routing structure provides fast interconnect

- **sysIO Capability**
  - LVCMOS 1.8, 2.5 and 3.3
  - LVTTL
  - SSTL 2 (I & II)
  - SSTL 3 (I & II)
  - CTT 3.3, CTT 2.5
  - HSTL (I & III)
  - PCI-X, PCI 3.3
  - GTL+
  - AGP-1X
  - 5V tolerance
  - Programmable drive strength

- **Ease of Design**
  - Product term sharing
  - Extensive clocking and OE capability

■ **Easy System Integration**
- 3.3V power supply
- Hot socketing
- Input pull-up, pull-down or bus-keeper
- Open drain capability
- Slew rate control
- Macrocell-based power management
- IEEE 1149.1 Boundary Scan testable
- In-System Programmable via IEEE 1532 ISC compliant interface

ispMACH 5000B Devices

■ **High Density**
- 128 to 512 macrocells
- 92 to 256 I/Os

■ **High Speed Logic Implementation**
- SuperWIDE 68-input logic block
- Up to 35 product terms per output
- Single-level Global Routing Pool (GRP)

■ **SysIO Capability**
- LVCMOS 1.8, 2.5 and 3.3
- LVTTL
- SSTL 2 (I&II)
- SSTL 3 (I&II)
- CTT 3.3, CTT 2.5
- HSTL (I&III)
- PCI 3.3
- GTL+
- AGP-1X
- LVDS (Clock input)
- LVPECL (Clock input)
- Programmable drive strength

■ **Ease of Design**
- Product term sharing
- Extensive clocking and OE capability

■ **Easy System Integration**
- 2.5V power supply
- Hot socketing
- Input pull-up, pull-down or bus-keeper
- Open drain capability
- Slew rate control
- Macrocell-based power management
- IEEE 1149.1 Boundary Scan testable
- IEEE 1532 compliant In-System Programmable (ISP™)

ispMACH 5000VG Overview

The ispMACH 5000VG devices consist of multiple SuperWIDE 68-input, 32-macrocell Generic Logic Blocks (GLBs) interconnected by a tiered routing system. Groups of four GLBs, referred to as segments, are interconnected via a Segment Routing Pool (SRP). Segments are interconnected via the Global Routing Pool (GRP.) Together the GLBs and the routing pools allow designers to create large designs in a single device without compromising performance.

Each GLB has 68 inputs coming from the SRP and contains 163 product terms. These product terms form groups of five product term clusters, which feed the PT sharing array or the macrocell directly. The ispMACH 5000VG allows up to 160 product terms to be connected to a single macrocell via the product term expanders and PT Sharing Array.

The macrocell is designed to provide flexible clocking and control functionality with the capability to select between global, product term and block-level resources. The outputs of the macrocells are fed back into the switch matrices and, if required, the sysIO cell.

All I/Os in the ispMACH 5000VG family are sysIOs, which are split into four banks. Each bank has a separate I/O power supply and reference voltage. The sysIO cells allow operation with a wide range of today's emerging interface standards. Within a bank, inputs can be set to a variety of standards, providing the reference voltage requirements of the chosen standards are compatible. Within a bank, the outputs can be set to differing standards, providing the I/O power supply voltage and the reference voltage requirements of the chosen standard are compatible. Support for this wide range of standards allows designers to achieve significantly higher board-level performance compared to the more traditional LVCMOS standards.

The ispMACH 5000VG devices also contain sysCLOCK Phase Locked Loops (PLLs) that provide designers with increased clocking flexibility. The PLLs can be used to synthesize new clocks for use on-chip or elsewhere within the system. They can also be used to deskew clocks, again both at the chip and system levels. A variable delay line capability further improves this and allows designers to retard or advance the clock in order to tune set-up and clock-to-out times for optimal results. Table 1 details the key attributes and packages for the ispMACH 5000VG devices.

ispMACH 5000B Family Overview

The ispMACH 5000B devices also consist of multiple SuperWIDE 68-input, 32-macrocell GLBs; however, they are interconnected by a single-level routing system (GRP). Together, the GLBs and the GRP allow designers to create large designs in a single device without compromising performance. The GLB has 68 inputs coming from the GRP and contains 163 product terms. These product terms form groups of five product term clusters, which feed the product term sharing array and the macrocell directly. The ispMACH 5000B allows up to 35 product terms to be connected to a single macrocell via the Product Term Sharing Array.

The macrocell is designed to provide flexible clocking and control functionality with the capability to select between global, product terms, and block-level resources. The outputs of the macrocells are fed back into the switch matrices and, if required, the sysIO cell.

The ispMACH 5000B devices are divided into four sysIO banks, where each bank is capable of supporting 14 different I/O standards. Support for this wide range of standards allow designers to achieve significantly higher board-level performance compared to the more traditional LVCMOS standards. Each sysIO bank has its own I/O supply voltage, reference voltage, and termination voltage, resources allowing each bank complete independence from the others. Each I/O within a bank is individually configurable consistent with the supply voltage and reference voltage settings. In addition, each I/O has individually configurable drive strength, weak pull-up, weak pull-down or a bus-friendly latch.

Tables 1 and 2 detail the key attributes and packages for the ispMACH 5000VG and ispMACH 5000B devices.

Table 1. ispMACH 5000VG (3.3V) Family Selection Guide

	ispMACH 5768VG	ispMACH 51024VG
Macrocells	768	1,024
User I/O Options	196/304	304/384
t_{PD} (ns)	5.0	5.0
t_S (ns) – Set-up with 0 Hold (ns)	3.0	3.0
t_{CO} (ns)	4.4	4.4
f_{MAX} (MHz)	178	178
Supply Voltage (V)	3.3	3.3
Package	256 fpBGA 484 fpBGA	484 fpBGA 676 fpBGA

Table 2. ispMACH 5000B (2.5V) Family Selection Guide

	ispMACH 5128B	ispMACH 5256B	ispMACH 5384B	ispMACH 5512B
Macrocells	128	256	384	512
User I/O Options	92	92/144	156/186	156/196/256
t_{PD} (ns)	3.0	4.0	4.0	4.5
t_S (ns) – Set-up with 0 Hold (ns)	1.7	2.1	2.1	2.5
t_{CO} (ns)	2.2	2.7	2.7	2.8
f_{MAX} (MHz)	275	250	250	200
Supply Voltage (V)	2.5	2.5	2.5	2.5
Package	128 TQFP	128 TQFP 208 PQFP 256 fpBGA	208 PQFP 256 fpBGA	208 PQFP 256 fpBGA[1] 484 fpBGA[1]

1. Pin compatible with ispMACH 5000VG.

Figure 1. ispMACH 5000VG Family Packages