# ispLSI® 8000 and 8000V Family Architectural Description

**October 2001**

## Introduction

The ispLSI 8000 and 8000V Family of Register-Intensive, SuperBIG™ In-System Programmable Logic Devices is based on Big Fast Megablocks of 120 registered macrocells and a Global Routing Plane (GRP) structure interconnecting the Big Fast Megablocks. Each Big Fast Megablock contains 120 registered macrocells arranged in six groups of 20, a group of 20 being referred to as a Generic Logic Block, or GLB. Within the Big Fast Megablock, a Big Fast Megablock Routing Pool (BRP) interconnects the six GLBs to each other and to 24 Big Fast Megablock I/O cells with optional I/O registers. The Global Routing Plane which interconnects the Big Fast Megablocks has an additional 144 global I/Os with optional I/O registers.

Outputs from the GLBs in a Big Fast Megablock can drive both the Big Fast Megablock Routing Pool within the Big Fast Megablock and the Global Routing Plane between the Big Fast Megablocks. Switching resources are provided to allow signals in the Global Routing Plane to drive any or all the Big Fast Megablocks in the device. This mechanism allows fast, efficient connections, both within the Big Fast Megablocks and between them.

***Figure 1. ispLSI 8840 and 8840V Functional Block Diagram***

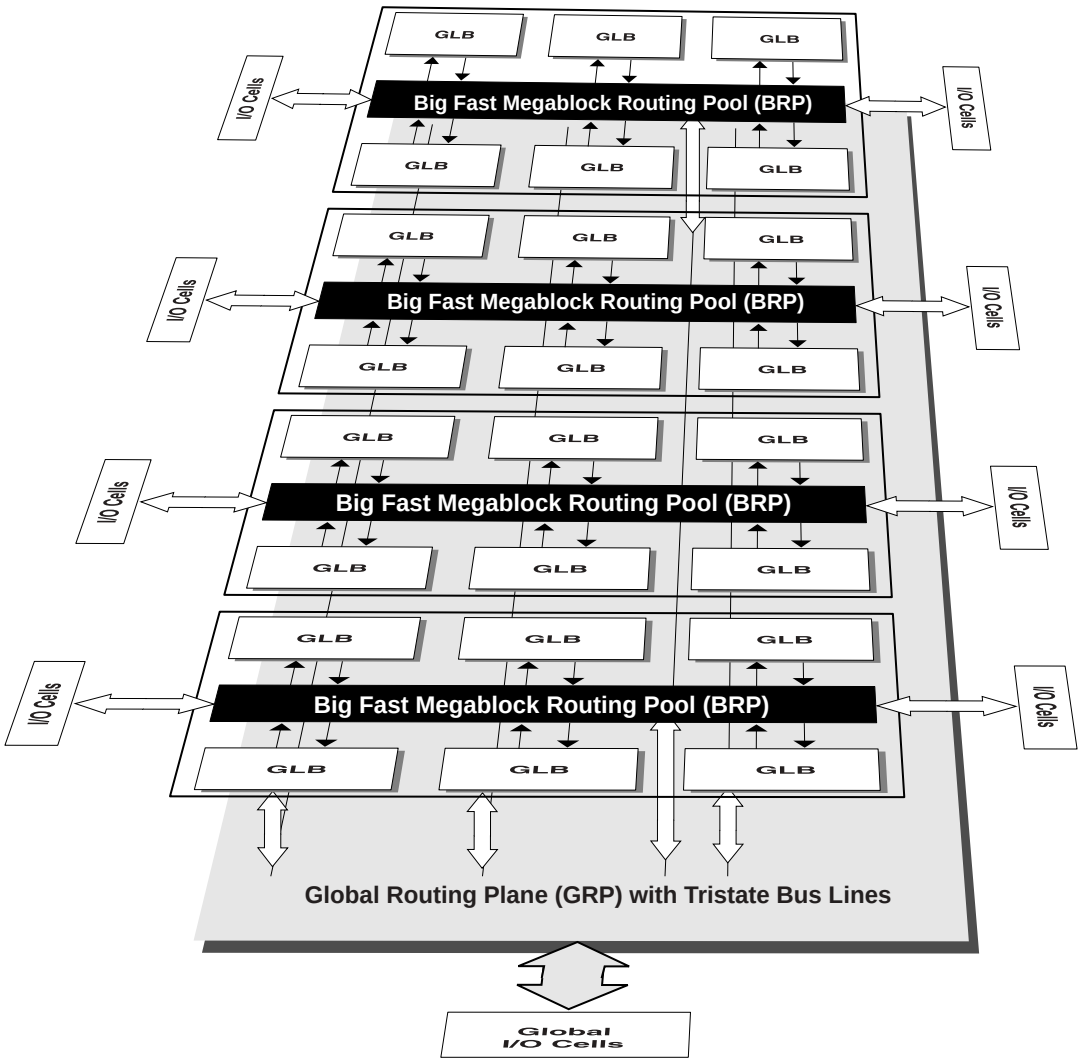
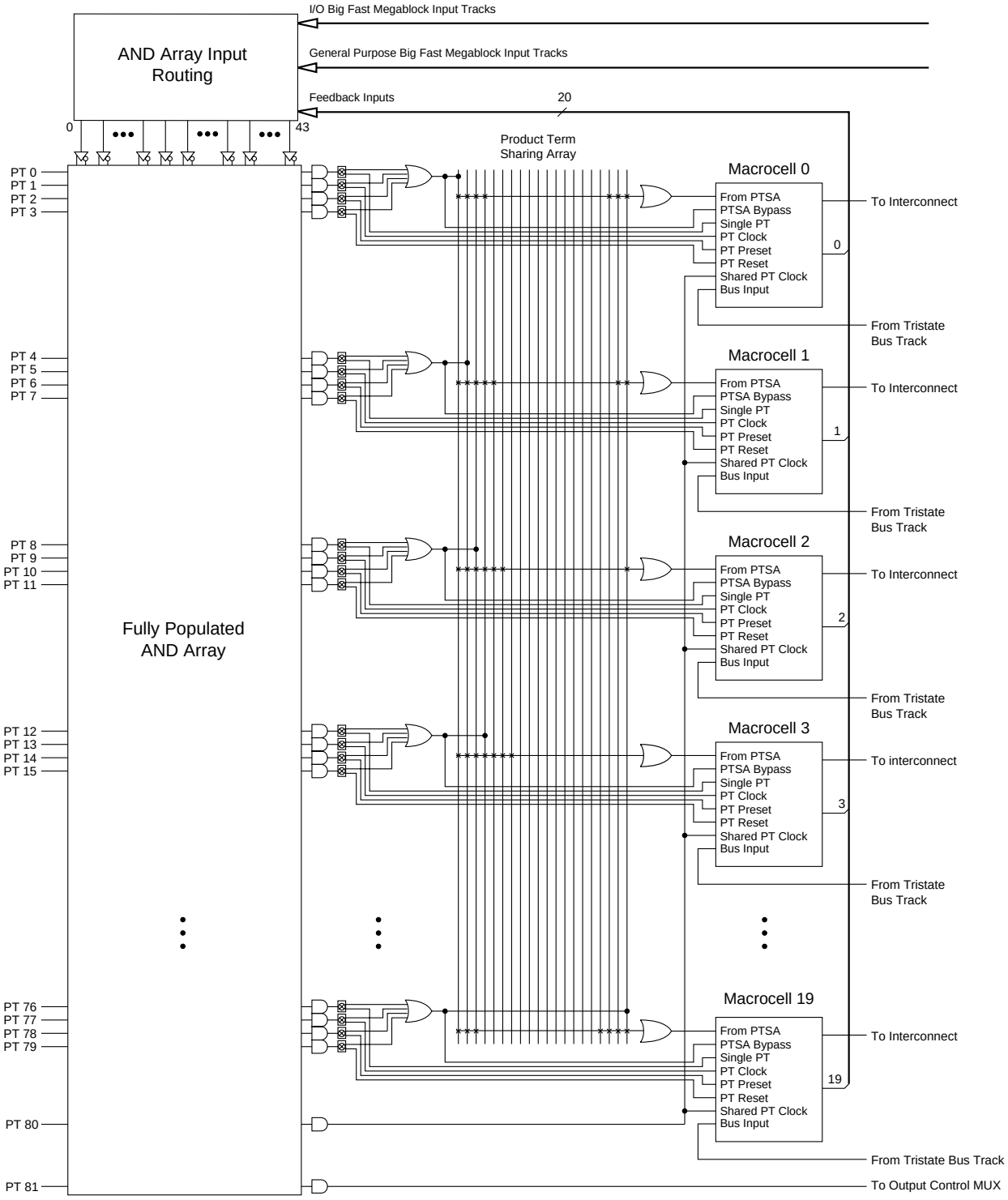


***Figure 2. ispLSI 8000 and 8000V GLB***




Note: Macrocells 9 and 10 do not support Tristate Bus Feedback.

⊠ Function Selector ($E^2$ Cell Controlled)

## Generic Logic Block

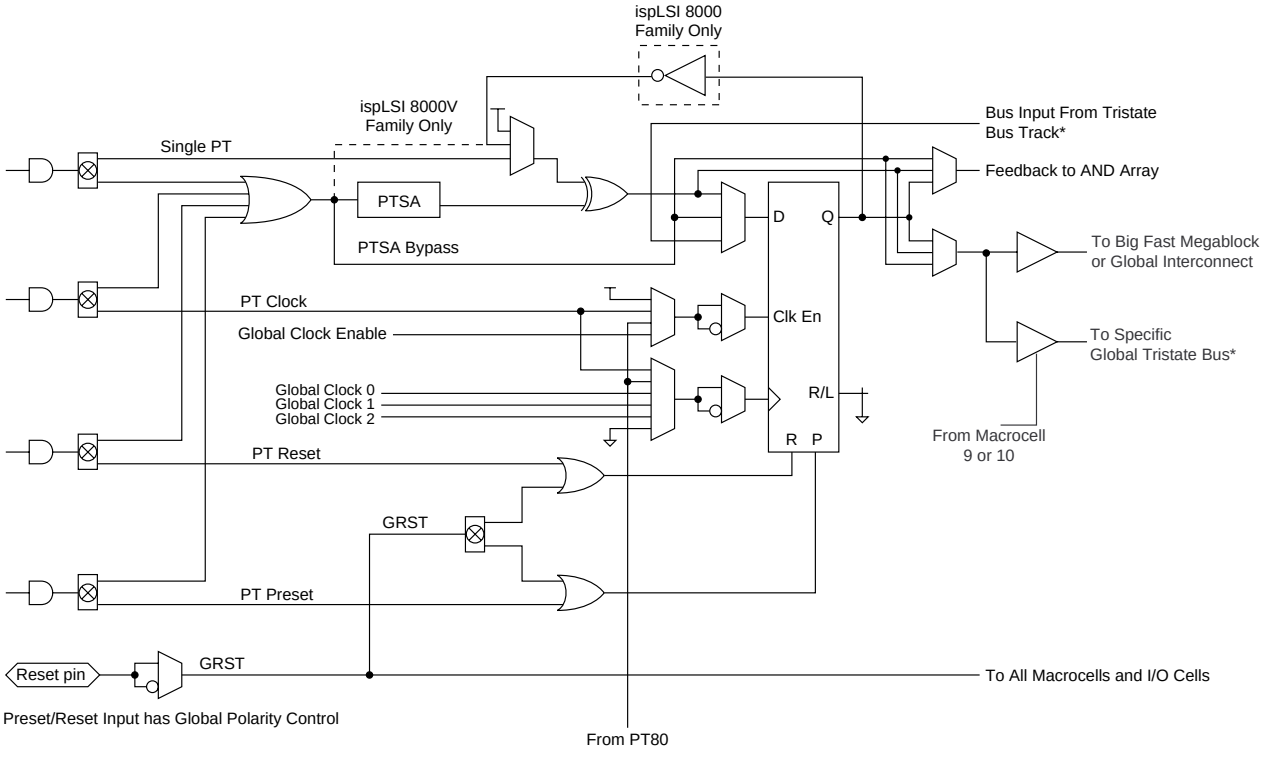
Each GLB contains 20 macrocells and a fully populated, programmable AND-array with 80 general purpose logic product terms. The GLB has 44 inputs which are available in both true and complement form for every product term can be driven from both BRP and GRP. Up to 20 of these inputs can be driven from the local feedback of the GLB for logic functions that require fast feedback. The 80 general purpose product terms can be grouped in 20 sets of four and sent into a Product Term Sharing Array (PTSA) which allows sharing up to a maximum of 28 product terms for a single macrocell function. Alternatively, the PTSA can be bypassed for functions of four product terms or less.

## Macrocell

The 20 registered macrocells in the GLB are driven by the 20 outputs from the PTSA or the PTSA bypass. Each macrocell contains a programmable XOR gate, a programmable register/latch/toggle flip-flop and the necessary clocks and control logic to allow combinatorial or registered operation. The macrocells each have two outputs, one output can be fed back inside the GLB to the AND-array, while the other output drives both the Big Fast Megablock Routing Pool and the Global Routing Plane. This dual or concurrent output capability from the macrocell allows efficient use of the hardware resources. One output can be a registered function for example, while the other output can be an unrelated combinatorial function feeding more complex logic functions elsewhere in the chip.

Macrocell registers can be clocked from one of several global, local or product term clocks available on the device. A global, local and product term clock enable is also provided, eliminating the need to gate the clock to the macrocell registers. Reset and preset for the macrocell register is provided from both global and product term signals. The polarity of all of these control signals is selectable on an individual macrocell basis. The macrocell register can be programmed to operate as a D-type register, a D-type latch or a T-type flip-flop.

***Figure 3. ispLSI 8000 and 8000V Macrocell***




*Not available for Macrocells 9 and 10.

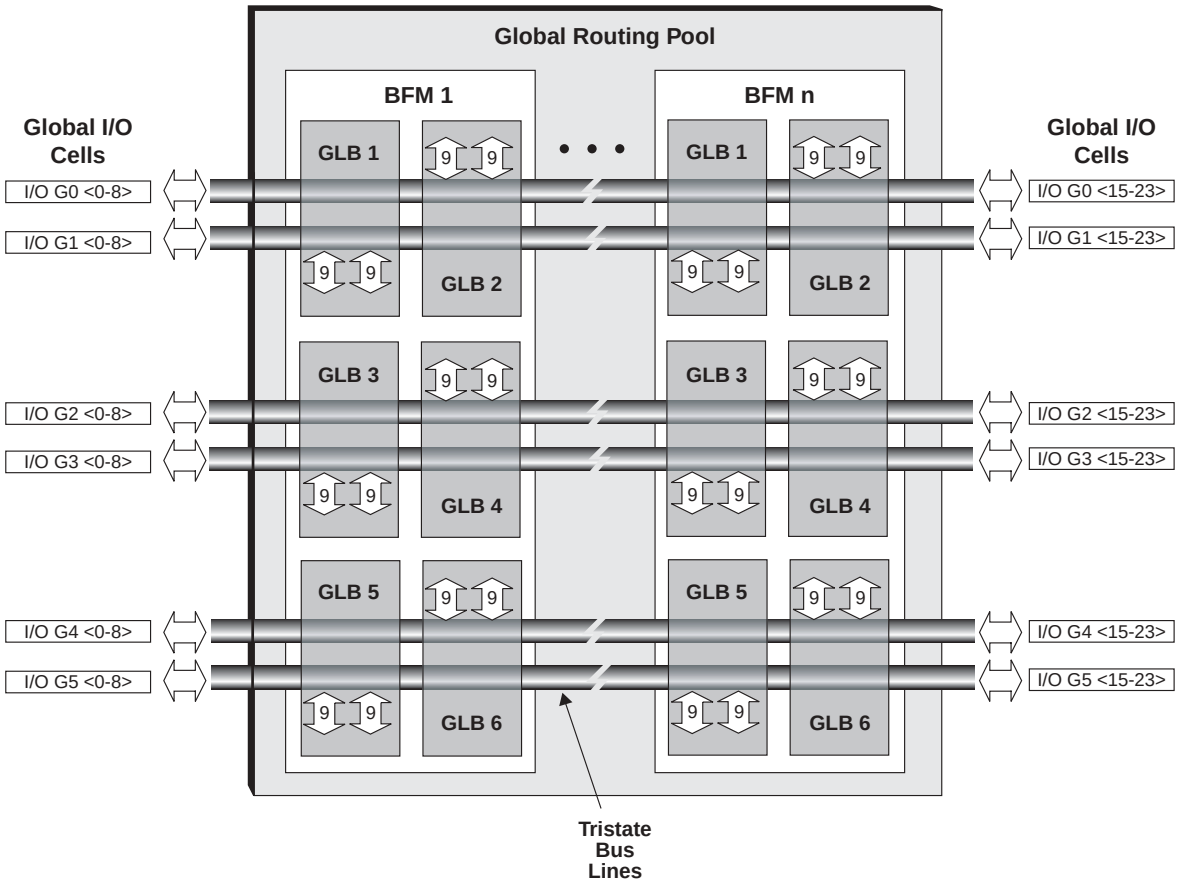
⊗ : Function Selector ($E^2$ Cell Controlled)

## Embedded Tristate Bus

The Global Routing Plane (GRP) includes a 108-line embedded internal tristate bus that enables multiple GLBs to drive the same tracks. This bus can be partitioned into various bus widths such as twelve 9-line buses, six 18-line buses or three 36-line buses. The GLBs can dynamically share a subset of the Global Routing Plane tracks. This feature eliminates the need to convert tristate buses to wide multiplexers on the programmable device. Up to 18 macrocells per GLB can participate in driving the embedded tristate bus. The remaining two macrocells per GLB are used to generate the internal tristate driver control signals on each data byte (with parity). The embedded tristate bus can also be configured as an extension of an external tristate bus using the bidirectional capability of the I/O cells connected to the Global Routing Plane. The Global Routing Plane I/Os 0-8 and 15-23 from each group (I/OGx as defined in the I/O Pin Location Table) can connect to the internal tristate bus as well as the unidirectional/non-tristate global routing channels. I/Os 9-14 connect only to the global routing channel.

The embedded tristate bus has internal bus hold and arbitration features in order to make the function more “user friendly”. The bus hold feature keeps the internal bus at the previously driven logic state when the bus is not driven to eliminate bus float. The bus arbitration is performed on a “first come, first served” priority. In other words, once a logic block drives the bus, other logic blocks cannot drive the bus until the first releases the bus. This arbitration feature prevents internal bus contention when there is an overlap between two bus enable signals. Typically, it takes about 3ns to resolve one bus signal coming off the bus to another bus signal driving the bus. The arbitration feature combined with the predictability of CPLD, makes the embedded tristate bus the most practical for the real world bus implementations.

***Figure 4. Embedded Tristate Bus***

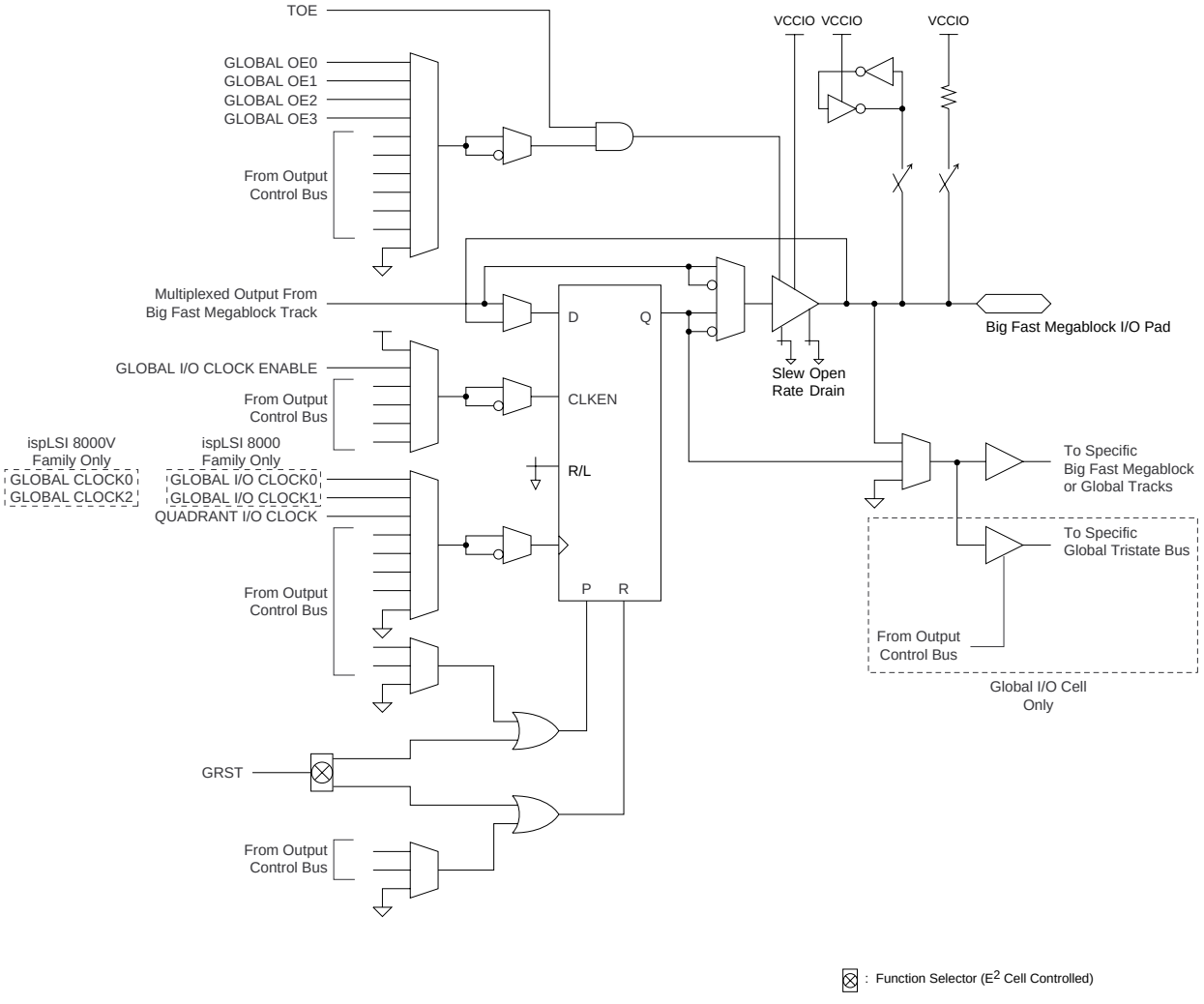


## I/O Cell and I/O Controls

Control signals for the I/O cell registers are generated using an extra product term within each GLB, or using dedicated input pins. Each GLB has two extra product terms beyond the 80 general purpose available for the macrocell logic. The first additional product term is used as an optional shared product term clock for all the macrocells within the GLB. The second additional product term is then routed to an I/O Control Bus using a separate routing structure from the Big Fast Megablock Routing Pool and Global Routing Plane. Use of a separate control bus routing structure allows the I/O registers to have many high-speed control signals with no impact on the interconnection of the GLBs and Big Fast Megablocks. The I/O Control Bus is split into four quadrants, each servicing the I/O cell control requirements for one edge of the device. Signals in the control bus can be independently selected by any or all I/O cells to act as clock, clock enable, output enable, reset or preset.

Each Big Fast Megablock has 24 I/O cells. The Global Routing Pool has 144 I/O cells. Each I/O cell can be configured as a combinatorial input, combinatorial output, registered input, registered output or bidirectional I/O. I/O cell registers can be clocked from one of several global, local or product term clocks which are selected from the I/O control bus. A global and product term clock enable is also provided, eliminating the need for the user to gate the clock to the I/O cell registers. Reset and preset for the I/O cell register is provided from both global and product term signals. The polarity of all of these control signals is selectable on an individual I/O cell basis. The I/O cell register can be programmed to operate as a D-type register or a D-type latch.

***Figure 5. I/O Cell***



## Clock Distribution

The ispLSI 8000 and 8000V family has several clock inputs from which the GLB and the I/O cell register clocks can be driven. There are three Global Clocks (CLK0-2), two Global I/O Clocks (GIOCLK0-1 for ispLSI 8000 Family only), and four Quadrant Clocks (QIOCLK0-3). In addition to the clock inputs, there is one GLB clock enable (CLKEN) and one I/O clock enable (IOCLKEN). The clock polarity can be selected at the individual register. The GLB global clocks can be used as master clocks which have the lowest internal clock skew. Global Clock0 and Global Clock2 in the ispLSI 8000V Family are also capable of driving the I/O register clocks. Similarly, the quadrant clocks are divided to drive each quadrant's I/Os (defined in the individual data sheets) with minimum clock skew.

## Boundary Scan

In-System Programming (ISP™) of the device is performed via IEEE1149.1 compliant JTAG state machine or Lattice ISP state machine for the ispLSI 8000 family. The BSCAN/$\overline{\text{ispEN}}$ pin selects between the two protocols. The four-wire interface on the ispLSI 8000 Family includes Test Data In (TDI)/Serial Data In (SDI), Test Clock (TCK)/Serial Clock (SCLK), Test Mode Select (TMS)/Mode Control (MODE), and Test Data Out (TDO)/Serial Data Out (SDO). ISP program enable and disable is controlled by the private programming instruction set for the ispJTAG™ interface and by the BSCAN/$\overline{\text{ispEN}}$ pin for the ISP interface.

The EPEN signal, when high, enables the Test Access Port (TAP) for programming and test for the ispLSI 8000V Family. The ispLSI 8000V Family provides the dedicated four-wire interface via TDI, TDO, TMS and TCK.

In addition to ISP programming, the JTAG state machine also provides standard boundary scan test capability. Standard boundary scan instructions supported are Sample/Preload, Extest, Bypass and High-Z instructions. The boundary scan test registers associated with each of the I/O pins control the state of the I/O pin when the device is not in normal functional mode. This feature allows users to define the state of the I/O pins during test and ISP programming modes.

***Figure 6. Boundary Scan Register for I/O Pins***

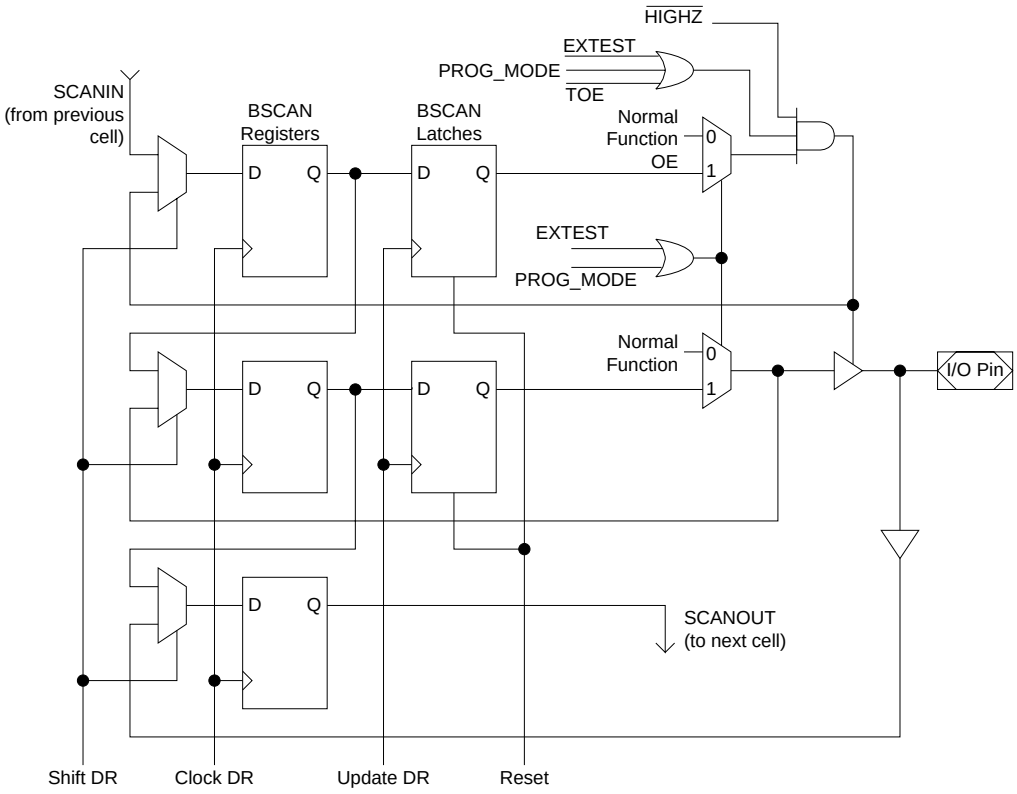
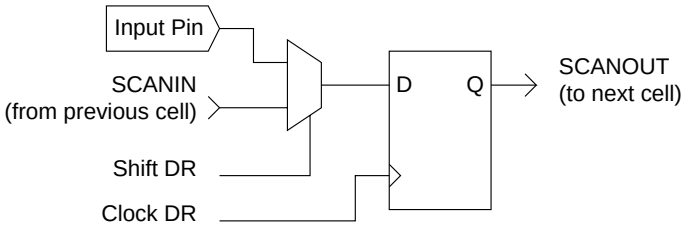


***Figure 7. Boundary Scan Register for Dedicated Input Pins***




## Timing Model

The task of determining the timing through the ispLSI 8000 and 8000V family, just as any CPLD, is relatively simple. The device timing model provided in Figure 8 shows the specific delay paths. Once the implementation of a given function is determined either conceptually or from the Fitter/Place and Route software report file, the delay path of the function can easily determined from the timing model. The software timing analyzer reports the timing delays based on the same timing model for a particular design. Note that the internal timing parameters are given for reference only, and are not tested. The external timing parameters are tested and guaranteed for every device.

***Figure 8. ispLSI 8000 and 8000V Simplified Timing Model***