Introduction to ispLSI® 2000E, 2000VE and 2000VL Families

Introduction

Lattice Semiconductor's ispLSI Families are high density and high performance E^2CMOS® programmable logic devices. They provide design engineers with a superior system solution for integrating high speed logic on a single chip.

With densities from 1,000-8,000 gates, the ispLSI 2000E, 2000VE and 2000VL Families are I/O-intensive, programmable logic devices that combine the high performance and ease of use of PLDs with the density and flexibility of FPGAs.

These CPLD families are ideal for designs needing high performance in conjunction with high I/O requirements.

The ispLSI 2000E, 2000VE and 2000VL Families incorporate Lattice Semiconductor's innovative In-System Programmable (ISP™) technology. ISP technology allows for real-time programming, less expensive manufacturing and end-user feature reconfiguration.

E^2CMOS technology features reprogrammability, the ability to program the device again and again to easily incorporate any design modifications. This same capability allows full parametric testability during manufacturing, which specifies 100 percent programming and functional yield.

ispLSI 2000E Family

- Industry's Fastest 5V CPLD
- 225 MHz System Performance
- 3.5 ns Pin-to-Pin Delay
- 5V Programmable Logic Core
- ispJTAG™ In-System Programmable via IEEE 1149.1 (JTAG) Test Access Port
- User-Selectable 3.3V or 5V I/O
- Programmable Open-Drain Outputs
- PCI Compatible Outputs

ispLSI 2000VE Family

- Industry's Fastest 3.3V CPLD
- 300 MHz System Performance
- 3.0 ns Pin-to-Pin Delay
- ispJTAG In-System Programmable via IEEE 1149.1 (JTAG) Test Access Port
- Boundary Scan Test (IEEE 1149.1)
- Programmable Open-Drain Outputs
- 3.3V/5V Compatible I/O

ispLSI 2000VL Family

- Industry's Fastest 2.5V Family
- 180MHz System Performance
- 5.0ns Pin-to-Pin Delay
- ispJTAG In-System Programmable via IEEE 1149.1 (JTAG) Test Access Port
- Boundary Scan Test (IEEE 1149.1)
- Programmable Open-Drain Outputs
- 3.3V Compatible I/O

ispLSI Development Tools

- ispLEVER™ Systems for PC and Lattice UNIX-Based Design Tools
- Tightly Integrated with Leading CAE Vendors' Tools
- Productivity Enhancing Static Timing Analyzer, Physical Viewer and Explore Tools
- VHDL, Verilog-HDL, ABEL, State Machine and Schematic Entry
- Timing and Functional Simulators
- Comprehensive ISP Programming Tools
- Windows® XP, Windows 2000, Windows 98, Windows NT®, Solaris and Hewlett-Packard UNIX Platforms

Overview

The ispLSI 2000E, 2000VE and 2000VL Families of high density devices address high performance system logic needs, implementing logic functions ranging from registers, to counters, to multiplexers, to complex state machines.

With PLD densities ranging from 1,000 to 8,000 gates, the ispLSI 2000E, 2000VE and 2000VL Families provide a wide range of programmable logic solutions to meet tomorrow's design requirements today.

Each device contains multiple Generic Logic Blocks (GLBs) designed to maximize system flexibility and performance. A balanced ratio of registers and I/O cells provides the optimum combination of internal logic and external connections. A global interconnect scheme ties everything together, enabling utilization of up to 80% of available logic. Tables 1 and 2 describe the Family attributes.

Introduction to ispLSI 2000E, 2000VE and 2000VL Families

The 2000VE and 2000VL Families offer multiple I/O options for the ispLSI 2128VE,2128VL and ispLSI 2064VE and 2064VL devices. The ispLSI 2128VE, and 2128VL are available in both 128- and 64-I/O versions and the ispLSI 2064VE and 2064VL are available in both 64- and 32-I/O versions.

Table 1. ispLSI 2000E (5V) Family Attributes

	2000E Family			
	2032E	**2064E**	**2096E**	**2128E**
Density (PLD Gates)	1,000	2,000	4,000	6,000
Speed: fmax (MHz)	225	200	180	180
Speed: tpd (ns)	3.5	4.5	5.0	5.0
Macrocells	32	64	96	128
Registers	32	64	96	128
Inputs + I/O	35	70	104	138
Pin/Package	44 PLCC 44 TQFP 48 TQFP*	100 TQFP*	128 TQFP* 128 PQFP*	176 TQFP*

*Supports 3.3V I/O and PCI-Compliant Drive

Table 1-0003A/2K

Table 2. ispLSI 2000VE (3.3V) Family Attributes

	2000VE Family				
	2032VE	**2064VE**	**2096VE**	**2128VE**	**2192VE**
Density (PLD Gates)	1,000	2,000	4,000	6,000	8,000
Speed: fmax (MHz)	300	280	250	250	225
Speed: tpd (ns)	3.0	3.5	4.0	4.0	4.0
Macrocells	32	64	96	128	192
Registers	32	64	96	128	192
Inputs + I/O	35	38/70	104	138/74	107/110
Pin/Package	44 PLCC* 44 TQFP 48 TQFP 49 caBGA	44 PLCC* 44 TQFP 100 TQFP 100 caBGA	128 TQFP	100 TQFP 100 caBGA 160 PQFP 176 TQFP 208 fpBGA	128 TQFP 144 fpBGA

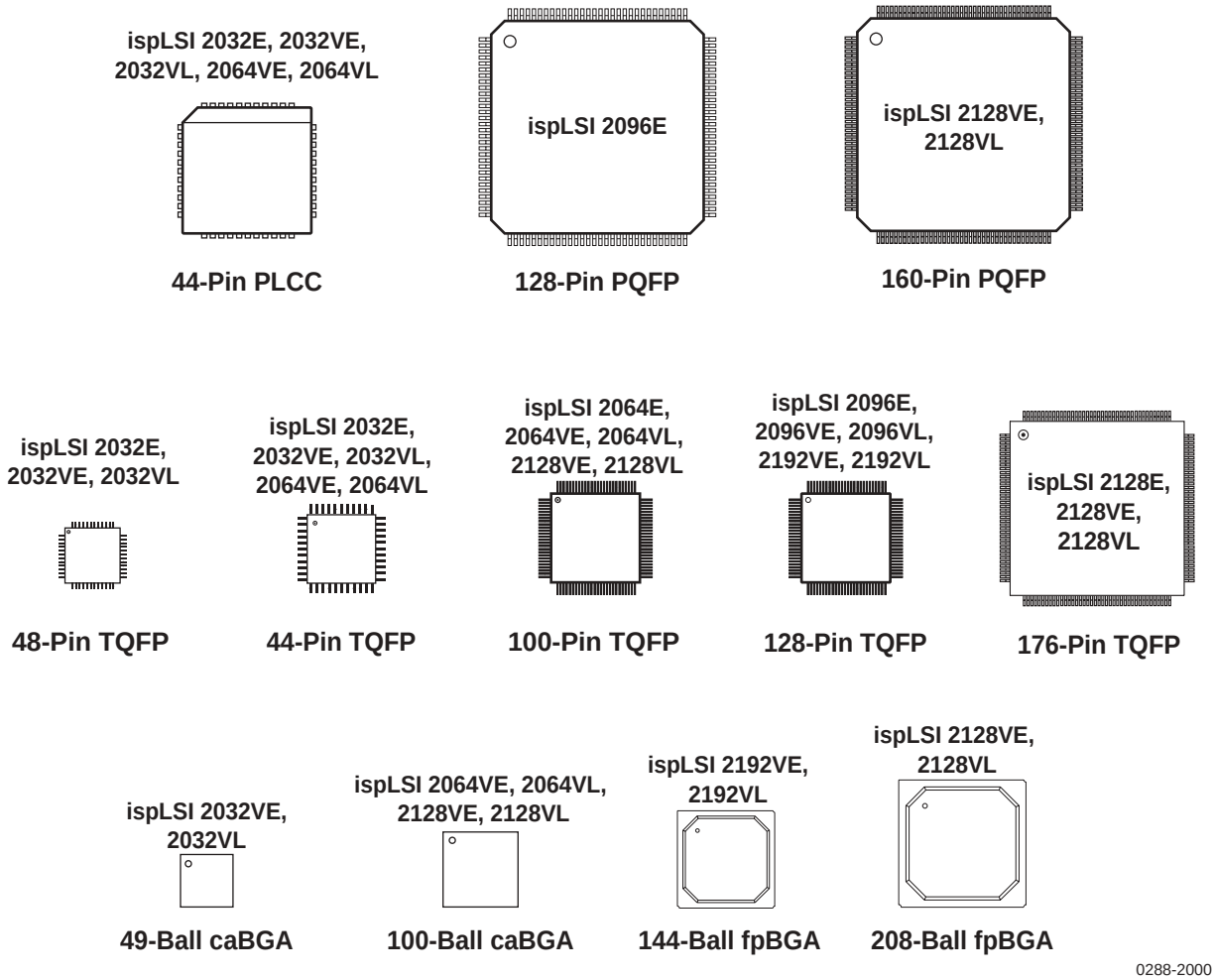
* Not available for fastest speed grade.

Table 3. ispLSI 2000VL (2.5V) Family Attributes

	2000VL Family				
	2032VL	**2064VL**	**2096VL**	**2128VL**	**2192VL**
Density (PLD Gates)	1,000	2,000	4,000	6,000	8,000
Speed: fmax (MHz)	180	165	165	150	150
Speed: tpd (ns)	5.0	5.5	5.5	6.0	6.0
Macrocells	32	64	96	128	192
Registers	32	64	96	128	192
Inputs + I/O	35	38/70	104	138/74	107/110
Pin/Package	44 PLCC 44 TQFP 48 TQFP 49 caBGA	44 PLCC 44 TQFP 100 TQFP 100 caBGA	128 TQFP	100 TQFP 100 caBGA 160 PQFP 176 TQFP 208 fpBGA	128 TQFP 144 fpBGA

Table 1-0003C/2K

Figure 1. ispLSI 2000E, 2000VE and 2000VL Family Packages



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