Introduction to ispLSI® 8000 and 8000V Families

Introduction

Lattice Semiconductor Corporation's SuperBIG™ ispLSI 8000 and 8000V families extend densities to 1080 macrocells while offering logic gating and high register counts. These families support high density designs where integration of complete logic subsystems into a single device is necessary.

The ispLSI 8000 and 8000V families, like all of Lattice's high density PLDs, are in-system programmable. In-System Programmability (ISP™) allows real-time programming, less expensive manufacturing and end-user feature reconfiguration.

E^2CMOS® technology features reprogrammability, the ability to program the device again and again, to easily incorporate any design modifications. This same capability allows full parametric testability during manufacturing, which guarantees 100 percent programming and functional yield.

ispLSI 8000 Family

- ❑ 5V Power Supply
- ❑ 110 MHz System Performance
- ❑ 8.5 ns Pin-to-Pin Delay
- ❑ Deterministic Performance
- ❑ 1152 Total Registers
- ❑ High Density (45,000 PLD Gates)
- ❑ 5V or 3.3V I/O
- ❑ State-of-the-Art BGA Packaging
- ❑ Flexible Easy-to-Use Architecture
- ❑ Internal Tristate Bus Support
- ❑ Open-Drain and Bus Hold I/O Options
- ❑ Extra-Wide GLB with 44 Inputs/20 Macrocells
- ❑ In-System Programmable
- ❑ Boundary Scan Test (IEEE 1149.1)
- ❑ PCI Compatible Inputs and Outputs

ispLSI 8000V Family

- ❑ 3.3V Power Supply
- ❑ 125 MHz System Performance
- ❑ 8.5 ns Pin-to-Pin Delay
- ❑ Deterministic Performance
- ❑ Up to 1440 Total Registers – the Industry's Largest CPLD!
- ❑ High Density (32,000 - 60,000 PLD Gates)
- ❑ 3.3V I/O and 2.5V Outputs
- ❑ State-of-the-Art BGA Packaging
- ❑ Flexible Easy-to-Use Architecture
- ❑ Internal Tristate Bus Support
- ❑ Open-Drain and Bus Hold I/O Options
- ❑ Extra-Wide GLB with 44 Inputs/20 Macrocells
- ❑ In-System Programmable
- ❑ Boundary Scan Test (IEEE 1149.1)

ispLSI Technology

- ❑ UltraMOS E^2CMOS — the PLD Technology of Choice
- ❑ Electrically Erasable/Programmable/ Reprogrammable
- ❑ 100% Tested During Manufacture
- ❑ 100% Programming Yield
- ❑ Fast Programming

ispLSI Development Tools

- ❑ ispLEVER™ Systems for PC and Lattice UNIX-Based Design Tools
- ❑ Tightly Integrated with Leading CAE Vendors' Tools
- ❑ Productivity Enhancing Static Timing Analyzer, Physical Viewer and Explore Tools
- ❑ VHDL, Verilog-HDL, ABEL, State Machine and Schematic Entry
- ❑ Timing and Functional Simulators
- ❑ Comprehensive ISP Programming Tools
- ❑ Windows® XP, Windows 2000, Windows 98, Windows NT®, Solaris and Hewlett-Packard UNIX Platforms

Introduction to ispLSI 8000 and 8000V Families

ispLSI 8000 and 8000V Families Overview

The ispLSI 8000 and 8000V families of 5V and 3.3V Register-Intensive, SuperBIG High Density In-System Programmable logic devices support high performance system logic designs. The devices implement system-level logic functions including high performance peripheral controllers, arithmetic co-processors and bus masters.

With densities up to 60,000 PLD gates, the ispLSI 8000 and 8000V families provide a flexible and innovative programmable logic solution for today's most complex design requirements.

Each ispLSI 8000 and 8000V family member's architecture is based on a Big Fast Megablock containing 120 registered macrocells and a Global Routing Plane (GRP) structure which interconnects the Big Fast Megablocks. Wide 20-macrocell Generic Logic Blocks (GLBs) and wide input gating (44 inputs) create a flexible and high performance solution. A global interconnect scheme ties everything together, enabling high utilization of available logic.

Table 1. ispLSI 8000 Family

	8840
Density (PLD Gates)	45,000
Speed: f_{max} (MHz)	110
Speed: t_{pd} (ns)	8.5
Macrocells	840
Registers	1152
Inputs + I/O*	312
Pin/Package	432-Ball BGA

*Supports 5V/3.3V I/O

8K Family

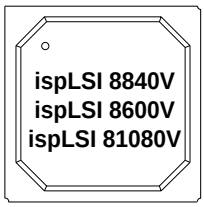
Table 2. ispLSI 8000V Family

	8600V	**8840V**	**81080V**
Density (PLD Gates)	32,000	45,000	60,000
Speed: f_{max} (MHz)	125	125	125
Speed: t_{pd} (ns)	8.5	8.5	8.5
Macrocells	600	840	1080
Registers	864	1152	1440
Inputs + I/O*	192-264	312	360
Pin/Package	272-Ball BGA 492-Ball BGA	272-Ball BGA 492-Ball BGA	272-Ball BGA 492-Ball BGA

*Supports 3.3V/2.5V I/O.

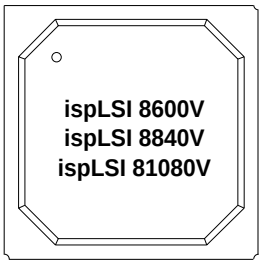
8KV Family

Figure 1. ispLSI 8000 and 8000V Family Packages



272-Ball BGA

432-Ball BGA



492-Ball BGA