Introduction to ispGDXV,® ispGDX® and ispGDS® Families

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Introduction

Lattice Semiconductor Corporation, the pioneer of non-volatile E^2CMOS® in-system programmable (ISP™) logic, has now expanded the application of ISP PLDs to include programmable switching, interconnect and jumper functions with the ispGDX and the ispGDS devices. In-system programmability allows for real-time programming, less expensive manufacturing and end-user feature reconfiguration.

The ispGDXV and ispGDX families provide designers with programmable alternatives for integration of eight- and 16-bit interface functions, as well as high performance and flexibility in system-level signal routing and interface applications.

This ispGDS (Generic Digital Switch) Family is an innovative programmable switch matrix architecture that allows quick implementation of changes to PCB connections without changing mechanical switches or other system hardware.

The ispGDXV, ispGDX and ispGDS devices provide higher quality and reliability than other interface and switch solutions due to the nature of E^2CMOS technology. E^2CMOS technology features reprogrammability, the ability to program the device again and again to easily incorporate design modifications. This same capability allows full parametric testability during manufacturing which guarantees 100 percent programming and functional yield.

Lattice's ispLEVER™ Development System software supports ispGDXV and ispGDX design using VHDL or Verilog. From creation to in-system programming, ispLEVER is an easy-to-use, self-contained design tool.

The ispGDS Compiler is a simple DOS command line compiler which accepts an ASCII text file of the ispGDS design description and produces a JEDEC file for programming and a .doc file containing design compilation details. The ispGDS Compiler syntax is easy, yet powerful, allowing the use of labels and operators.

ispGDXV Family

- Flexible Architecture
- 3.3V Core Voltage
- Programmable 3.3V or 2.5V Output Levels
- 250MHz System Performance
- 3.0ns Pin-to-Pin Delay
- 80 to 240 Programmable I/O Pins
- Programmable Wide MUX Supports up to 16:1 MUX
- Boundary Scan Test (IEEE 1149.1 Standard)
- PCI Compatible Output Drive

ispGDX Family

- Flexible Architecture, 5V Core Voltage
- 111MHz System Performance
- 5ns Pin-to-Pin Delay
- 80 to 160 Programmable I/O Pins
- Boundary Scan Test (IEEE 1149.1 Standard)
- PCI Compatible 24mA Output Drive
- Lattice ISP or ispJTAG™ Programming Interface

ispGDS Family

- High-Speed Switch Matrix
- 7.5ns Propagation Delay
- 14, 18 or 22 I/Os
- In-System Programmable

ISP Product Technology

- UltraMOS E^2CMOS — the PLD Technology of Choice
- Electrically Erasable/Programmable/Reprogrammable
- 100% Tested During Manufacture
- 100% Programming Yield
- Fast Programming

ispGDX Development in the ispLEVER Design System

- VHDL and Verilog Synthesis Support
- Industry Standard JEDEC File for Programming
- Min/Max and Detailed Timing Reports
- Interfaces to Popular Timing Simulators
- Detailed Log and Report Files for Easy Design Debug
- On-line Help
- Windows 2000, Windows 98, Windows XP and Windows NT Compatible Graphical User Interface
- Solaris and HP-UX Versions Available

ispGDS Assembler

- Accepts ASCII Text Design Description
- Includes Preprocessor For Adding Labels and Inversion
- Industry Standard JEDEC File for Programming

ispGDXV and ispGDX Family Overview

The Generic Digital Crosspoint families (ispGDX and ispGDXV) from Lattice Semiconductor consists of seven members, ranging from 80 to 240 programmable I/Os. This innovative in-system programmable architecture has been optimized for digital signal interface and routing applications and features a series of special-purpose programmable I/O cells interconnected by an E^2CMOS Global Routing Pool (GRP).

Any input can be routed to any output and each I/O cell has individual programmable I/O tri-state control (OE), output latch clock (CLK), programmable polarity, open-drain output emulation and two MUX select (MUXsel) inputs which control a fast 4:1 MUX allowing dynamic selection of up to four signal sources for a given output. Inputs or outputs can be combinatorial, latched, registered or driven to a static HIGH or LOW state.

The 3.3V ispGDXV Family is a functional superset of the ispGDX family, adding new features and greater I/O options. The I/Os are capable of 3.3V and 2.5V input/output levels.

High performance (3.0ns) in this family is combined with low power in space-saving BGA, TQFP and PQFP packages.

ispGDS Family Overview

The ispGDS (Generic Digital Switch) Family combines the in-system programmability, high performance and low power of Lattice Semiconductor's GAL programmable logic technology with a switch matrix architecture, resulting in an innovative programmable signal router. The ispGDS is a configurable switch matrix which provides the ability to quickly implement and change PCB connections without changing mechanical switches or other system hardware. ISP allows the connections to be reprogrammed without removal from the printed circuit board via a simple

5V, 4-wire serial interface. This capability allows the system designer to define hardware which can be reconfigured in-system to meet a variety of applications. The ispGDS also conserves board real estate, providing up to 22 I/Os in about a quarter square inch of board space.

With today's demand for user-friendly systems, there is an increasing need for hardware which is easily reconfigured under software control without manual intervention. The ispGDS family is an ideal solution for end-system feature reconfiguration and signal routing applications. The fast 7.5ns propagation delay through the devices supports high-performance signal routing applications. Easier system upgrades, user feature selection and system manufacturing are the results.

There are two members of the ispGDS Family: the ispGDS22 and ispGDS14. Each of the devices operate identically with the only difference being the number of I/O cells available.

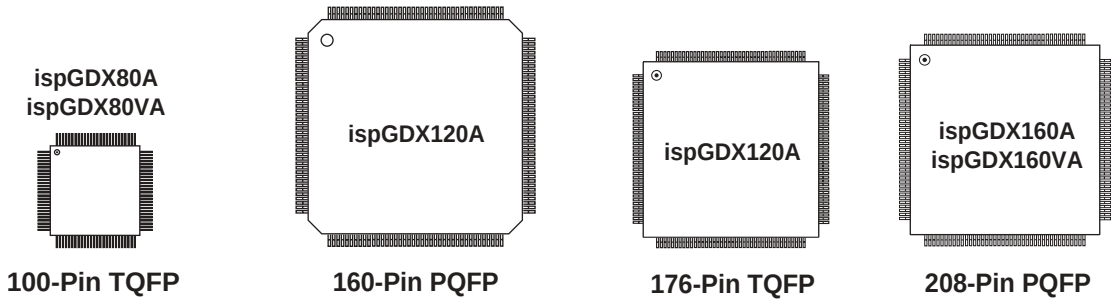
Table 1. ispGDX/V Family Attributes

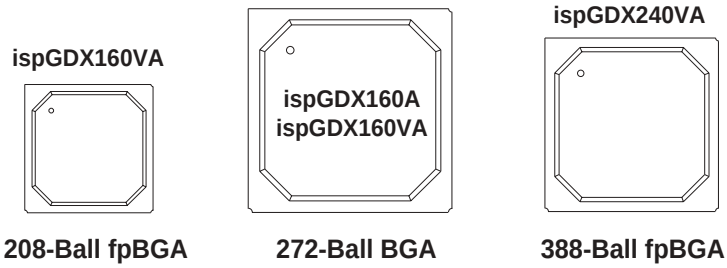
	ispGDX80A/VA	ispGDX120A	ispGDX160A/VA	ispGDX240VA
Voltage	5V/3.3V	5V	5V/3.3V	3.3V
I/O Pins	80	120	160	240
Speed: **f**max (MHz)*	143/250	143	143/250	167
Speed: **t**pd (ns)	5/3.0	5	5/3.5	5/4.5
Dedicated Clock Pins	2	4	4	4
Pin/Packages	100-Pin TQFP	160-Pin PQFP 176-Pin TQFP	208-Pin PQFP 208-Ball fpBGA 272-Ball BGA	388-Pin fpBGA

*$f_{max} = 1/(t_{wh} + t_{wl})$

GDX Attributes

Figure 1. ispGDXV and ispGDX Family Packages





GDX Packages

Figure 2. ispGDS Family Packages