Using ispLSI® 5000VE Devices in a Hot Swap Environment

January 2002 Application Note AN8069

Introduction

The term “hot swap” refers to the common practice of either inserting or removing devices or boards to or from a system without a proper power-up sequence or stable signals during power up. Hot swapping is beneficial to both designers and customers. It allows the removal of potentially defective devices or boards from a system, or upgrade capacity without the inconvenience and expense of taking the entire system down. Lattice’s SuperWIDE™ ispLSI 5000VE devices can be used to interface with communication standard and proprietary buses where hot swap capability is desired. The I/O leakage current stays at less than 10μA (without the internal pull-up) when the input voltage is swept from 0V to 5.6V. This is a desirable characteristic for hot swap environments. This application note describes the I/O behavior of ispLSI 5000VE devices in hot swap applications.

I/O Characteristics

The input and I/O voltage/current characteristics of the ispLSI 5000VE devices illustrate how the devices behave in a hot swap environment. It is critical that there are no abnormal current surges on the pins during the hot swapping process. It is also necessary to know when the device outputs turn on and off during a power-up or power-down cycle so that proper load/behavior on the bus or board can be expected.

Figures 1-8 show voltage vs. current for an I/O pin configured as input or tri-stated output for ispLSI 5000VE devices. Since the ispLSI 5000VE device family has two kinds of power supply pins (V_{CC} and V_{CCIO}), there are six combinations of power supply sequencing to be considered. In addition, the development software allows the I/O pin to be internally referenced to V_{CCIO} or to V_{CC}. When the I/O is referenced to V_{CC} from the development software, the I/Os will operate at 3.3V standards and the V_{CCIO} has no affect on the I/O pin. Otherwise, the V_{CCIO} pin supplies the reference voltage for the I/O pin. The I/O pin characteristic shown in Figures 1-6 are taken with the I/O pin referenced to V_{CCIO}. Figures 7 and 8 show the conditions where an I/O pin is referenced to V_{CC} through the development software. The input voltage is swept from -1.0V to +6.0V.

Figure Number	V_{CC} (V)	V_{CCIO} (V)
1	3.3	3.3
2	3.3	2.5
3	3.3	0
4	0	3.3
5	0	2.5
6	0	0
7	3.3	V_{CC}
8	0	V_{CC}

Figure 9 shows the V_{CC} level at which the output pin becomes active. In this case, the output signal is a combinatorial path. The V_{CC} level at which the ispLSI 5000VE output becomes active is approximately 1.5V. Figure 10 shows the V_{CC} level at which the output pin becomes inactive. The V_{CC} level at which the ispLSI 5000VE stops to switch is approximately 1.3V. The absolute maximum V_{CC} specification of 5.4V for the ispLSI 5000VE devices must be satisfied at all times.

It is recommended to tie the JTAG pins high if a board is to be used in a hot swap environment. This is to prevent the JTAG state machine from entering a state other than the Test-Logic-Reset state. The TMS, TDI and TCK pins can be tied high with a resister in the range from 4.7K to 10kΩ.

Summary

As shown in the graphs, there is no current surge in the positive voltage range as long as the input voltage condition is within the specification. The current starts to increase as the voltage is swept in the negative direction as a result of the input clamp (ESD) protection circuitry. The ispLSI 5000VE I/Os do not show current discontinuity during power up and power down. These characteristics prove that the device will not go into undesirable states in a hot swap environment when all the external sources meet the specification.

Technical Support Assistance

Hotline: 1-800-LATTICE (Domestic)
1-408-826-6002 (International)
e-mail: techsupport@latticesemi.com

Figure 1. Input Characteristic with V_{CC} = 3.3V, V_{CCIO} = 3.3V

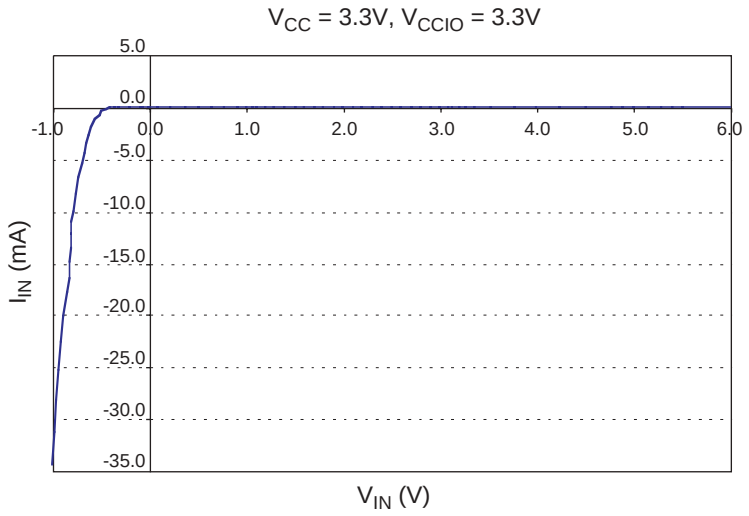

Figure 2. Input Characteristic with V_{CC} = 3.3V, V_{CCIO} = 2.5V

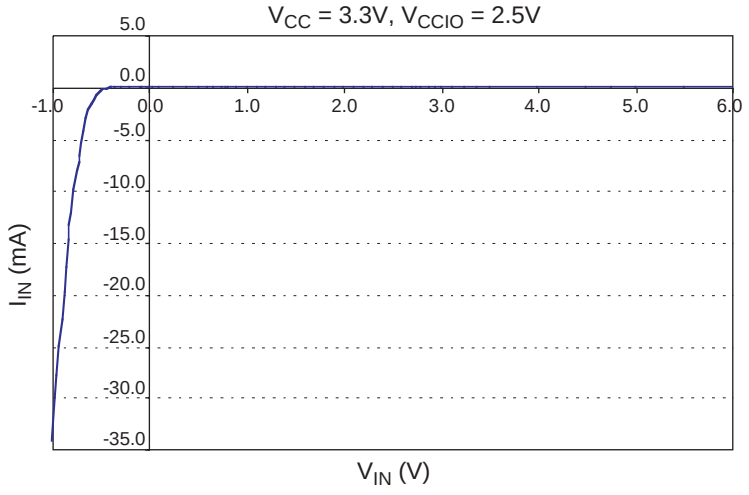

Figure 3. Input Characteristic with V_{CC} = 3.3V, V_{CCIO} = 0V

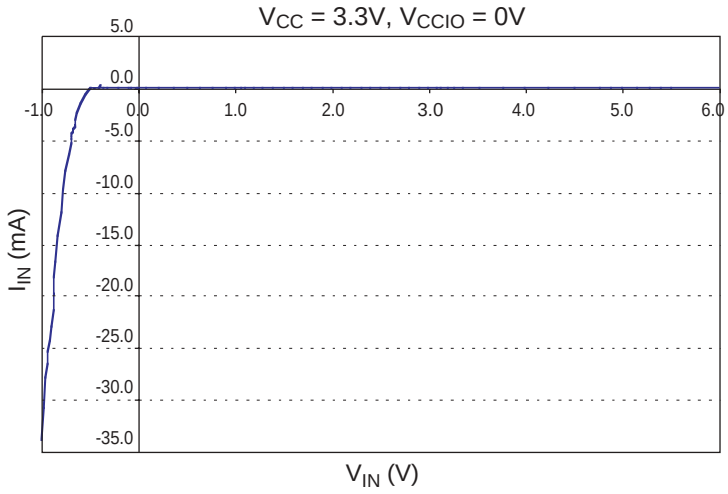

Figure 4. Input Characteristic with V_{CC} = 0V, V_{CCIO} = 3.3V

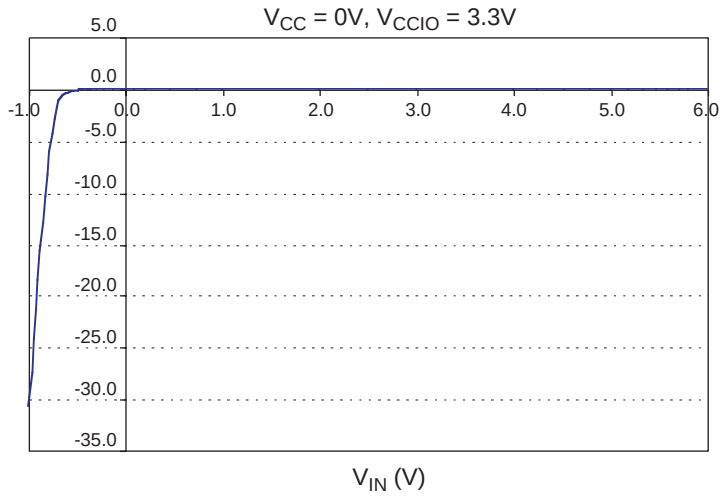

Figure 5. Input Characteristic with V_{CC} = 0V, V_{CCIO} = 2.5V

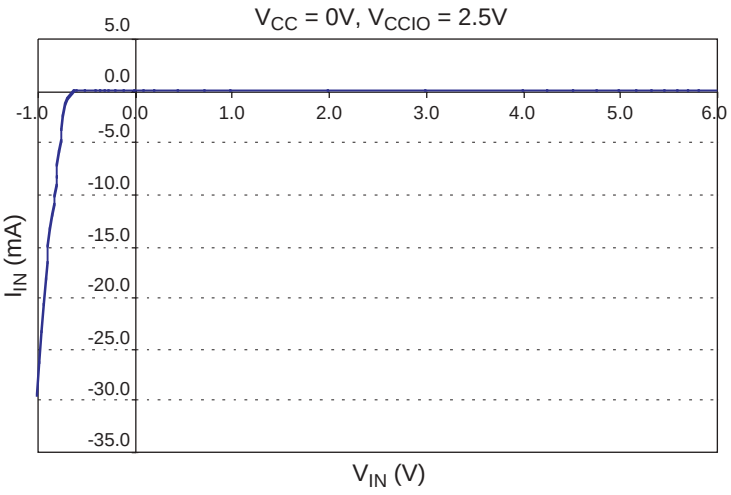

Figure 6. Input Characteristic with V_{CC} = 0V, V_{CCIO} = 3.3V

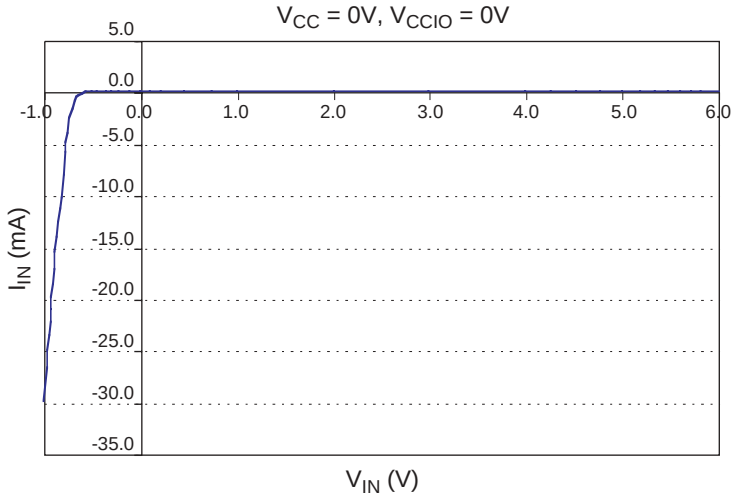

Figure 7. Input Characteristic with V_{CC} = V_{CCIO} = 3.3V

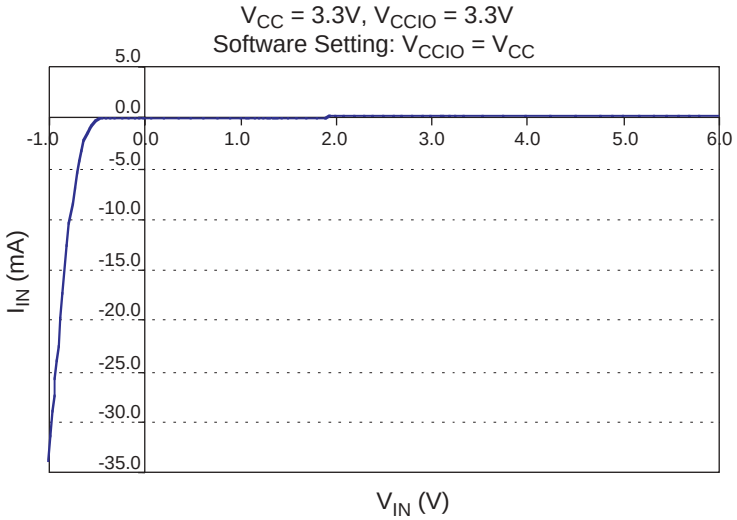

Figure 8. Input Characteristic with V_{CC} = V_{CCIO} = 0V

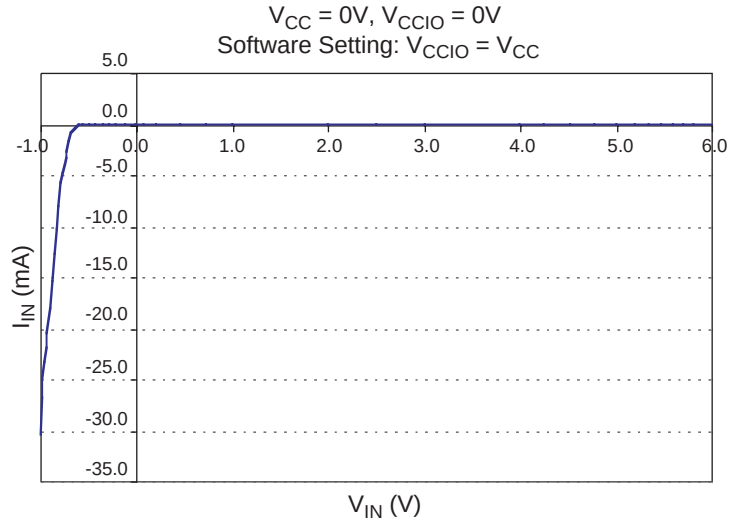

Figure 9. Output Power-up Characteristics

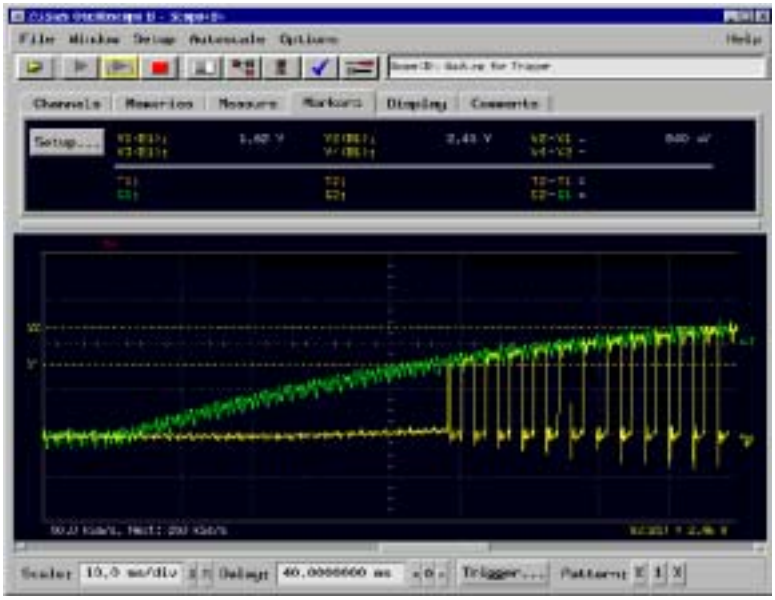

Figure 10. Output Power-down Characteristics