Using ispGDX160VA with the Motorola MPC860 to Provide a Generic Communications Processor Solution

Introduction

The Motorola MPC860 microprocessor has a Power PC core and a quad integrated communications controller. This application note overviews a design example showing how two Lattice 3.3V in system programmable cross point switch GDX160VA devices can be used in conjunction with the MPC860 to provide a generic and flexible Comms I/F module. One GDX160VA is used to interface to the Communications Processor Module and the other with the Memory Controller.

Communications Processor Module

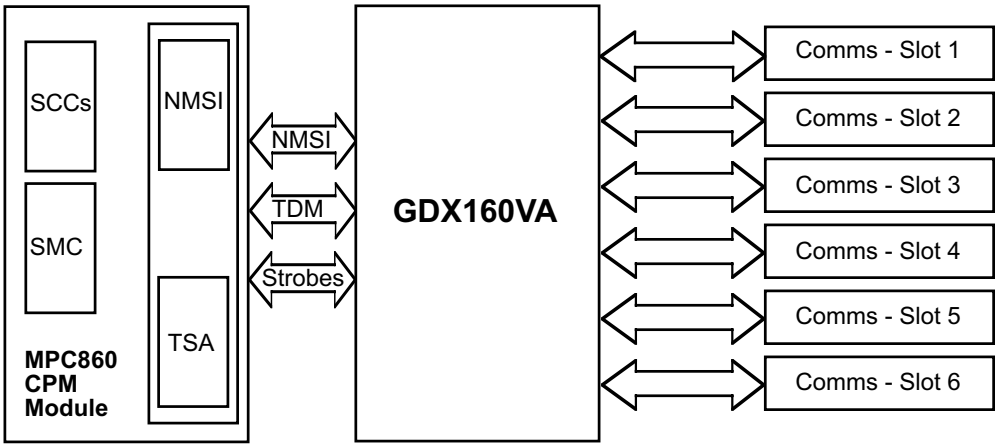
The Communications Processor Module (CPM) allows the MPC860 to implement high performance communication links. It supports multiple communication channels, with each supporting multiple protocols. The CPM contains Baud Rate generators, four full-duplex Serial Communication Controllers(SCCs), two full-duplex Serial Management Channels (SMCs) and a Time Slot Assigner (TSA). Protocols supported include Ethernet, UART, BISYNC and HDLC. The TSA supports Basic Rate ISDN, Primary Rate ISDN and RS232. In all the CPM has around sixty programmable, multi function I/O pins through which these functions communicate externally.

To keep the design generic and flexible the communication ports are housed on plug in daughter cards which provide the physical/mechanical interface. There are separate daughter cards for Ethernet, Basic Rate ISDN, Primary Rate ISDN, RS232 and so on. The daughter card configuration on the motherboard will determine the Comms functionality of the product.

Fig.1. shows the CPM/GDX160VA block diagram. The connection between the CPM and GDX160VA is via the Serial Interface (SI) on the MPC860. The SI consists of two sets of pins, the Non-Multiplexed Serial Interface (NMSI) and the Time Division Multiplexed (TDM) pins. There are two TDMs (A and B) which share a common set of pins and are controlled by the Time Slot Assigner. The GDX160VA connects to all of the NMSI and TDM pins as well as the four strobe output pins. It accommodates up to six separate Comms channel daughter card sockets. The GDX160VA is used to allow the routing of any of the SI pins of the MPC860 to any of the lines of the six symmetrical Comms channels. Each of the Comms channel sockets can support any protocol and be populated with any daughter card, the GDX160VA allowing any mix of cards. For example the BRI ISDN daughter card can be plugged into any or all of the six Comms sockets or you could have two PRI ISDN, one Ethernet and three RS232 cards and so on.

The GDX160VA maps the appropriate CPM resources according to the Comms function currently being supported. So, for example, SMC1 muxed (via TDM pins) or SMC1 non-muxed (via NMSI) can be routed to any of the Comms sockets. It provides fast bi-directional buffering, transceiver and dynamic muxing functions with low sig-

Figure 1. MC/GDX160VA Block Diagram



nal skew and good switching characteristics. In all the GDX160VA replaces approximately a dozen octal TTL devices which would otherwise be required to perform these functions. Also the flexibility of re-configurability for different Comms applications and JTAG test provides added value to the GDX solution. The fully populated, non-blocking General Routing Pool (GRP) of the GDXV makes it ideally suited for this type of point to point mapping.Memory Controller

The MPC860 Memory Controller (MC) controls up to eight memory blocks shared between a General Purpose Chip select Machine (GPCM) and two User Programmable Machines (UPMA and UPMB). Each memory block can be assigned to any of the three machines. The MC provides dynamic bus sizing, eight Chip Select lines, Write Enable and Output enable strobes, arbitration logic and a DRAM controller.

The GPCM supports fixed timing patterns for lower performance, non-burst mode memory like boot EPROM and also memory mapped peripherals such as FPGA/CPLD and user I/F blocks. The UPMs support higher performance memory blocks such as DRAM and burst mode SRAM and finer granularity timing patterns. Each UPM provides four byte select and six general purpose lines, address muxing, periodic timers and generation of programmable control signals for RAS/CAS strobes. They can be used to provide customised strobes allowing the implementation of memory systems with specific timing requirements.

Fig.2. shows the MC/GDX160VA block diagram. The GDX160VA interfaces to the MC pins and the 32 bit address bus pins of the MPC860 and generates eight separate control busses for support of RAM, Flash, Dual Port RAM, Memory Mapped CPLD/FPGA and user specific interfaces. The address bus is buffered for distribution to the rest of the board. In addition, two of the address bits are decoded in the GDX160VA to provide four bank select signals. This is possible as the GDXV I/O cell Mux is like a two input look up table allowing the emulation of any two input TTL function. The two address inputs connect to the two Mux select lines and the four Mux inputs (A-D) are set internally to values which give the correct output for the chosen function. The two bit decoder consumes four I/O cells and is achieved in 4ns.

To keep the design as generic and flexible as possible all of the control busses are kept symmetrical. Some of the memory and peripheral blocks may be housed on daughter cards which could be plugged into any of the eight control busses allowing multiple/different memory and peripheral configurations. The non-blocking fully populated GRP allows any pin of the MC interface on the MPC860 to bi-directionally connect to any of the signals of each of the control busses. Therefore the GPCM, UPMA or UMPB can be used at will without having to take into account PCB layout considerations for these machines at an early stage of development. This may improve time to market. Also if, for example, it was necessary to change the timing patterns for strobes on a particular memory bus that is currently connected to the GPCM then this can be achieved by reprogramming the GDX160VA via ispJTAG and mapping to one of the UPMs instead.

The fast 4ns Tpd, non-blocking GRP, low skew, superior switching characteristics with high current drive make the GDXV ideal for the Memory Controller interface function. Also the 5V compatible I/O allows direct interfacing to 5V core devices. In all about fifteen octal TTL devices have been integrated into a single GDX160VA part.

Conclusion

The two GDX160VA devices used to interface to the CPM and MC in this design example represent a saving of up to thirty chips over the equivalent discrete octal TTL solution. This represents a significant saving in component count, PCB area/complexity, and cost. In addition, the added boundary scan test feature enhances the overall testability of the product. The GDX160VA devices provide fast and flexible buffering, routing and dynamic muxing of the MPC860 resources with a minimal 4ns latency. Their in system programmability via the JTAG port allows a generic processor motherboard to be configured at the testing stage to support multiple Comms configurations and flexible memory block/peripheral interfacing dependant on the end customer application.

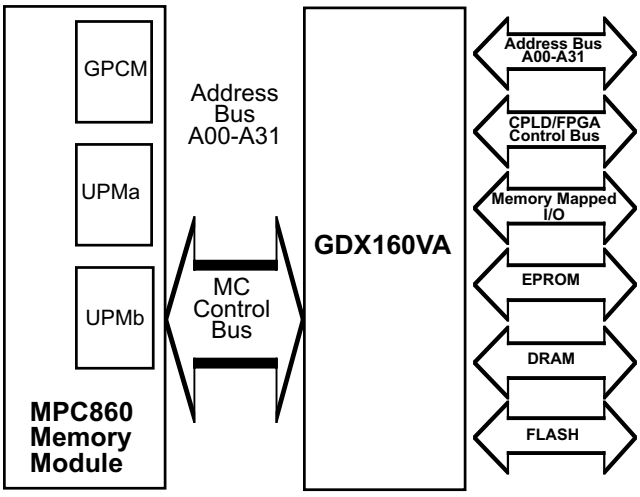


Figure 2. CPM/GDX160VA Block Diagram