Power Management and Calculation for Certus-NX Devices

Technical Note

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AF%	Activity Factor Percentage
ADC	Analog Digital Converter
AP	Application Processor
DPM	Defects Per Million
EBR	Embedded Block RAM
FDSOI	Fully Depleted Silicon on Insulator
FPGA	Field Programmable Gate Array
GPIO	General Purpose Input/Output
HDL	Hardware Description Language
HP	High Performance
IO	Input Output
LFM	Linear Feet per Minute
LMMI	Lattice Memory Mapped Interface
LP	Low Power
LRAM	Large RAM
LUT	Look-Up Table
LVDS	Low Voltage Differential Signaling
OSC	Oscillator
PLL	Phase Locked Loop
T_J, T_A, T_B, T_C,	Junction, Ambient, Board and Case Temperatures
TWR	Trace Report
UDB	Unified Design Database
USR	User Interface
VCD	Value Change Dump
VCO	Voltage Controlled Oscillator

1. Introduction

Certus™-NX low-power general purpose FPGAs from Lattice Semiconductor help stretch battery life and simplify thermal management in end applications by lowering power consumption. Certus-NX device features the ability to dynamically shut down used blocks in user mode. In addition, there is the ability to switch the device from High Performance (HP) to Low Power (LP) mode by changing the technology back bias via a performance grade selection.

This technical note serves as a usage guide for managing and determining the power consumption of Certus-NX devices. The document details the conceptual and functional description along with a guide to utilize the power saving functions. Analyzing power consumption in your design using the Lattice Radiant® software Power Calculator tool is also described.

2. User Standby Mode during Normal State

User Standby Mode for Certus-NX devices is useful in reducing power consumption when the device is in operation state, which is Normal State. User Standby Mode is a dynamically controlled option where some blocks can be placed in a User Standby Mode when the block is not required by the application. The reduction in power in achieved by placing these blocks in a low leakage state.

Take care when enabling the User Standby Mode for the blocks. This renders the blocks non-functional. Only the block capable of being placed in User Standby Mode should be placed in the state, if it is not used in the application.

Table 2.1 provides a list of blocks that have User Standby Mode and the signal required to place in a Standby Mode.

Table 2.1. Blocks Supporting User Standby Mode

Block	User Standby Control Signal
PLL	Through PLL powerdown (pllpd_en_n_i) signal. Low signal powers down block.
IO (1.8 V bottom banks)	Through LVDS output buffer disable and INR disable via bank control (STDBYINR and STDBYDIF signals). High signal powers down feature.
LRAM	Through the dps_i signal. High signal powers down block.
ADC	Through the adc_en_i signal. Low signal powers down block.

2.1. Usage of User Standby Mode

Each block with User Standby Mode option has a signal that can be accessed via FPGA fabric through soft logic. Application should include a soft controller for accessing User Standby Mode features. This soft controller can place the unused blocks in User Standby Mode, and hence provide the power savings.

Figure 2.1 is a sample block diagram of the User Standby Mode use case. The diagram shows a soft user logic that is similar to a state machine. The user logic can place each block in User Standby Mode either together or selectively.

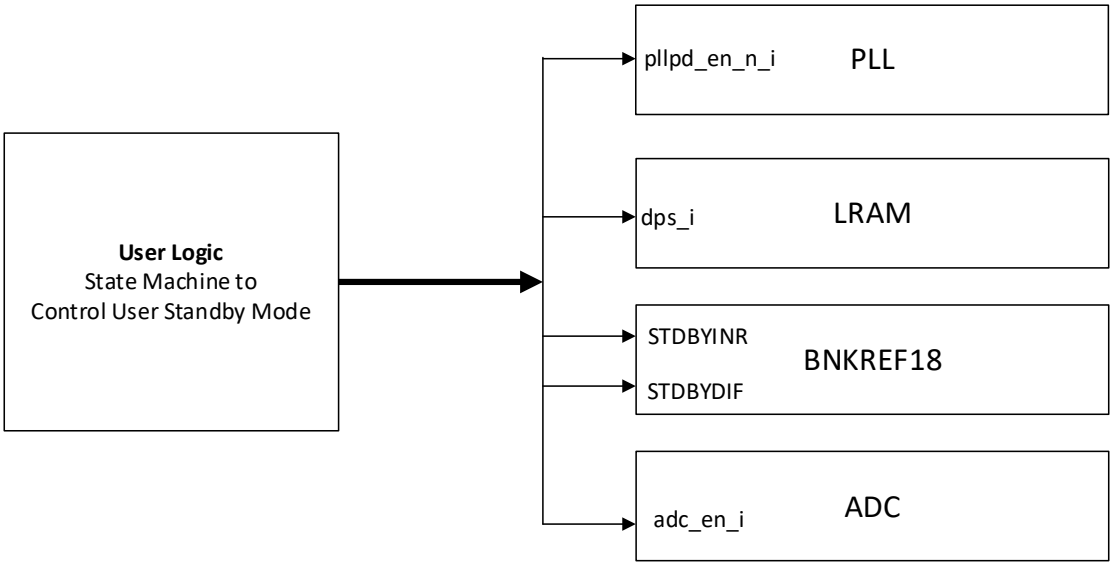

Figure 2.1. User Standby Mode Use Case Example Block Diagram

The following sections discuss how each of the blocks can be placed in User Standby Mode, the signals that can be used, and recommendations.

2.1.1. User Standby Mode for PLL

The Certus-NX device PLL contains a User Standby Mode that allows the PLL to be placed into a standby state to save power when not needed in the design. User Standby Mode is very similar to holding the PLL in reset since the Voltage Controlled Oscillator (VCO) is turned OFF and needs to regain lock when exiting standby. In both cases, reset and standby mode, the PLL retains its programming.

When generating the PLL using Lattice Radiant IP Catalog Designer, the standby option can be enabled by checking **Power Mode Settings: Enable Powerdown Mode** under **Optional Ports** tab in the PLL configuration user interface. This adds the PLL Powerdown Port pllpd_en_n_i which is an active low signal. This port can then be connected to the soft controller for dynamic control during periods when PLL is not required.

2.1.2. User Standby Mode for LRAM

The LRAM has the ability to shut down a portion of the internal logic off upon assertion of the dps_i signal. This initiates the always-on portion of the LRAM to gate inputs and shuts down the internal memory.

2.1.3. User Standby Mode for ADC

The ADC uses the adc_en_i to enable or disable the block. It disables the clocking within the block, thus reducing power when the block is not being used.

2.1.4. User Standby Mode for Inputs and Outputs

Referenced, differential, and LVDS I/O standards consume more power than other I/O standards and are not always required to be active. Bank Controller allows you to turn the I/O off dynamically on the bottom banks only. The STDBYINR signal is used to turn OFF referenced and differential inputs. The STDBYDIFF signal is used to turn OFF the LVDS output driver.

In order to use these feature, the application must instantiate the primitives that control these bank controllers. Primitives and corresponding simulation behavior are discussed in the section below. The control signals to enable and disable this feature has to be controlled by user logic.

2.1.4.1. Bank Controller for Input Reference and Differential

In the Certus-NX device, the Dynamic Bank Controller is used to power down banks that have Referenced and Differential inputs. The control is dynamic, and if needed can release these inputs including bidirectional I/O.

The BNKREF18 primitive is discussed in the next session.

BNKREF18 Primitive

BNKREF18 Dynamic Bank Controller is represented with the primitive as shown in Figure 2.2. Each instantiation controls a single bank. If control is required for two banks, two BNKREF18 primitives have to be instantiated.

The Inputs Reference and Differential Enable, or the STDBYINR signal is an active high signal that can place these inputs in User Standby Mode. This disables the referenced and differential receivers and any bank controller reference circuits that consume dynamic power, resulting in reduction in power consumption by these circuits.

The LVDS Output Enable, or the LVDSENI signal is an active high signal that can place these outputs in User Standby Mode. This disables the LVDS output receiver circuits that consume dynamic power, resulting in reduction in power consumption by these circuits.

For further details on the implementation of this primitive, refer to Lattice Radiant Software online help.

Figure 2.2. Primitive for Bank Controller

3. Power Performance Grade

The Certus-NX family parts have the ability to switch power performance grades due to a feature of the 28 nm Fully Depleted Silicon on Insulator (FDSOI) technology. The power-speed tradeoff on the technology can be modified by adjusting the back bias voltage. This is implemented by choosing one of the two power performance grades available at each speed and voltage setting. The HP grade stands for high performance, and consumes the most power. The LP grade stands for low performance, and consumes the least power at the cost of speed.

This performance grade can be selected when the device is selected in the Lattice Radiant software, or adjusted after the fact. However, this is not a dynamic setting that can be modified after the device is configured.

4. Power Consumption and Calculation

Lattice Radiant software includes a Power Calculator tool that can determine the power consumption of the Certus-NX devices. Power Calculator is the fastest power simulation tool available in the industry. It offers two modes: Estimation Mode for what-if analysis, and Calculation Mode for the more accurate application-specific power consumption by importing UDB design files. The engine performs each calculation quickly and accurately.

When running the Power Calculator tool in Estimation Mode, you can provide estimates of the utilization of various components and the tool provides an estimate of the power consumption. This is a good start, especially for what-if analyses and device selection.

Calculation Mode, on the other hand, is a more accurate approach, where you can import the actual device utilization by importing the post place and route netlist design file, or the UDB file. Additionally, Power Calculator supports features like Trace Report or TWR import, to get the clock frequencies for various clocks. Trace Report only includes frequencies of the clocks nets that are constrained in the Preference file. You are still required to provide frequencies of the clocks that are not included in Preference file and hence the Trace Report.

The default Activity Factor (AF%) for dynamic power calculation is set to 10% in the Power Calculator. You can change the default AF for the entire project or for each clock net individually. Activity Factor is discussed in detail in the Activity Factor Calculation section.

4.1. Power Calculator

To start Power Calculator from the Lattice Radiant software Tools menu or toolbar:

1. Open a project or create a new one.
2. Choose **Tools > Power Calculator**.

Power Calculator main window opens in estimation mode or calculation mode, depending on the design stage, and displays the Power Summary page as shown in Figure 4.1.

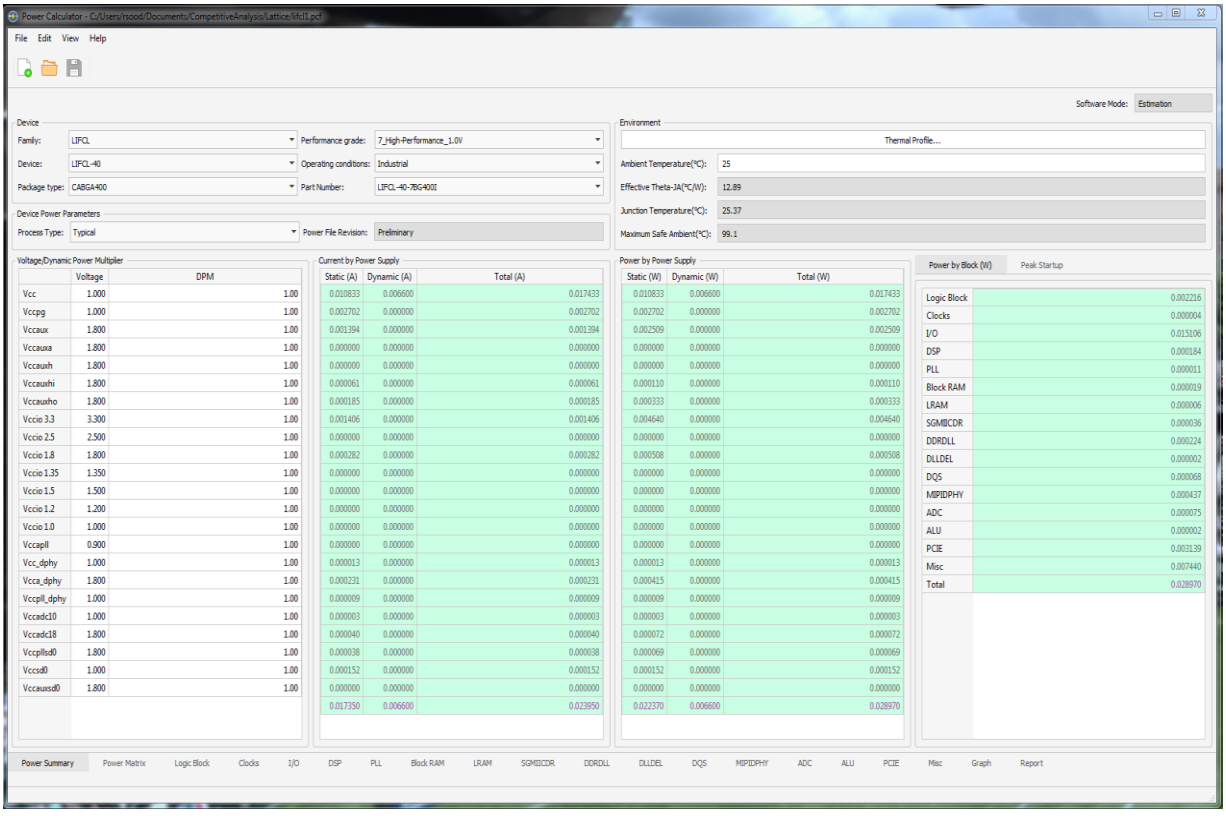

Figure 4.1. Power Calculator (Summary Tab for Certus-NX Devices)

It is important to understand how the options available in Power Calculator affect the power. For example, if the ambient temperature is changed, the junction temperature is affected according to the following equation:

$$T_J = T_A + \theta_{JA\_EFFECTIVE} * P$$

Where T_J and T_A are the junction and ambient temperatures, respectively, and P is the power.

$\theta_{JA\_EFFECTIVE}$ is the effective thermal impedance between the die and its environment.

The junction temperature is directly dependent on the ambient temperature. An increase in T_A increases T_J and results in an increase of the static leakage component.

Power can be affected by selecting the Process Type or the frequency at which the application runs. Process primarily changes the static leakage or Static Power. Frequency changes dynamic power. Increasing the frequency of toggling increases the dynamic component of power.

4.1.1. Typical and Worst Case Process

Process variation is a naturally occurring variation in the attributes of transistors such as length, widths, oxide thickness, when integrated circuits are fabricated. Process variation causes measurable and predictable variance in the output performance of all circuits.

Lattice Radiant software Power Calculator provides the option to select the Typical such as the mean current/power of distribution, and the Worst Case such as the maximum current/power of distribution, as a result of the variation. Process variation primarily affects the static leakage component of the device.

Process Type selection in Power Calculator allows you to understand the current and power variation of the devices, and predicts accurate results that are application specific. These can be used for power supply design, battery capacity design, and thermal management for each application.

4.1.2. Junction Temperature

Junction temperature is the temperature of the die during operation. It is one of the most important factors that affects the device power. For a fixed junction temperature, voltage and device package combination, static power is fixed.

Ambient temperature affects the junction temperature. Devices operating in a high-temperature environment have higher leakage since their junction temperature is higher. Power Calculator models the interdependence of ambient and junction temperature. When you provide an ambient temperature, it is rolled into an algorithm that calculates the junction temperature and power through an iterative process to find the thermal equilibrium of the system as defined in Lattice Radiant with respect to its thermal environment such as T_A and airflow.

Thermal Impedance plays an important role in determining the devices behavior, and the tool takes it into account to calculate maximum safe ambient temperature. See the Thermal Management section for details on how the Power Calculator uses thermal impedances.

4.1.3. Maximum Safe Ambient Temperature

Maximum Safe Ambient Temperature is one of the most important numbers displayed in the Summary tab of the Power Calculator. This is the maximum ambient temperature at which the device application can run without violating the junction temperature limits for the grade of the device, commercial or industrial.

Power Calculator uses an algorithm to accurately predict this temperature. The algorithm adjusts itself as the user changes options such as voltage, process, frequency, activity factor, thermal impedance and so on, or any factor that may affect the power dissipation of the device.

Thus it becomes extremely important to provide more accurate inputs to the tool for more accurate predicted results.

4.1.4. Operating Temperature Range

When designing a system, make sure a device operates at specified temperatures within the system environment. This is particularly important to consider before a system is designed. With Power Calculator, you can predict device thermodynamics and estimate the dynamic power budget. The ability to estimate device operating temperature prior to board design also allows you to better plan for power budgeting and thermal management.

Although total power, ambient temperature, thermal resistance and airflow all contribute to device thermodynamics, the junction temperature as specified in Operating Conditions in the Certus-NX Family Data Sheet (FPGA-DS-02078) is the key to device operation.

The allowed junction temperature range is 0 °C to 85 °C for commercial grade devices and –40 °C to 100 °C for industrial grade devices. If the junction temperature of the die is not within these temperature ranges, the performance, reliability, and functionality can get affected.

4.1.5. Dynamic Power Multiplier

In general, for semiconductors devices, the dynamic power consumption is independent of the variation in process and temperature. Power Calculator follows this rule, and hence any change to either process or temperature does not change the dynamic current or power.

In order to provide an option to add some safeguards, Power Calculator includes the Dynamic Power Multiplier or DPM column right next to the voltage supplies on the Summary tab. DPM allows you to add a multiplier for the dynamic current for each individual power supplies. This multiplier is included in the dynamic current equation.

Dynamic Power Multiplier has a default value 1 that means the dynamic power is what is predicted by the Power Calculator. If you want to add, say 20%, additional dynamic power, the DPM can be set to 1.2 (1 + 20%) and it can be placed against the appropriate power supply. This increases the dynamic power for that supply by 20% and provides you with some guard band.

4.1.6. Peak Startup Current

The bottom right panel of the Summary tab in Lattice Radiant software Power Calculator includes the Peak Startup tab. This tab provides an important piece of information, especially for designing the capacity for power supply or batteries.

The Peak Startup Current tab provides the current that the Certus-NX device pulls on each power supply when it is powered on. In certain cases, as applicable, this tab also includes the period of time period for which this current lasts.

4.1.7. Power Budgeting

Both the Peak Startup current and the operational current of the device should be considered when budgeting for power supply or battery capacity. It is recommended that the higher of the two numbers be used as reference for capacity calculations.

4.1.8. Device Operational Limits

Power Calculator provides the power dissipation of a design under a given set of conditions. It also predicts the junction temperature (T_J) for the design. Any time this junction temperature is outside the limits specified in Certus-NX Family Data Sheet (FPGA-DS-02078), the viability of operating the device at this junction temperature must be re-evaluated.

A commercial-grade device is likely to show speed degradation at junction temperatures above 85 °C and an industrial-grade device at junction temperatures above 100 °C. It is required that the die temperature be kept below these limits to achieve the guaranteed speed operation.

Operating a device at a higher temperature also means a higher static current and hence power. The difference between static current and total current, both static and dynamic currents, at a given temperature provides the power budget available. This is also very useful in power supply or battery capacity designs.

If the device runs at a current higher than this budget, the total ICC is also higher. This causes the die temperature to rise above the specified operating conditions. The four factors of power, ambient temperature, thermal resistance, and airflow, can also be varied and controlled to reduce the junction temperature of the device. Power Calculator is a powerful tool to help system designers manage FPGA power usage to improve overall system reliability.

Power Calculator clearly indicates when the application is running power higher than recommended. If the junction temperature goes beyond the grade limits, the box turns red in the Summary tab. The junction temperature calculations are provided up to 125 °C, which is also the reliability limit of the Certus-NX devices. If the junction temperature is beyond 125 °C under the conditions provided, the tool indicates it by 125+. This shows that the device achieves thermal equilibrium beyond 125 °C.

In certain cases, the thermal equilibrium cannot be achieved by the application under given conditions. In such situation, the device can continue to generate and not dissipate heat. Power Calculator has a built-in algorithm to determine such situations. This is indicated with 125++ under junction temperature calculation. This situation should be avoided under all circumstances, as this can cause permanent damage to the device.

4.1.9. Activity Factor Calculation

The Activity Factor % (or AF%) is defined as the percentage of frequency or time that a signal is active or toggling the output. Most resources associated with a clock domain are running or toggling at some percentage of the frequency at which the clock is running. You must provide this value as a percentage under the AF% column in the Power Calculator tool.

Another term for I/O is the I/O Toggle Rate. The AF% is applicable to the PFU, Routing, and Memory Read Write Ports, and so on. The activity of I/O is determined by the signals provided by you in the case of inputs, or as an output of the design in the case of outputs. The rates at which the I/O toggles define their activity. The I/O Toggle Rate or the I/O Toggle Frequency is a better measure of their activity.

The Toggle Rate (or TR) in MHz of the output is defined in the following equation:

$$\text{Toggle Rate (MHz)} = 1/2 * f * AF\%$$

You are required to provide the TR (MHz) value for the I/O instead of providing the frequency and AF% for other resources. AF can be calculated for each routing resource, output or PFU. However, this involves long calculations. The general recommendation for a design occupying roughly 30% to 70% of the device is an AF% between 15% and 25%. This is an average value. The accurate value of an AF depends upon clock frequency, stimulus to the design and the final output.

Power Calculator allows you to import a Value Change Dump (VCD) file from the simulation to accurately assess the activity factor of the design (Edit > Open Simulation File). The VCD file is based on Post-P&R simulation, and it is an ASCII file generated by the simulator. Check the simulation tool document on how to generate VCD file. The AF calculated from the VCD file is based on how accurate the test-bench or stimulus is for the simulation.

4.1.10. Power Calculator Assumptions

The following are the assumptions made by the Power Calculator:

- The Power Calculator tool uses default ambient temperature of 25°C which is the room temperature. This default temperature can be changed.
- You can define the ambient temperature (T_A) for device junction temperature (T_J) calculation based on the power estimation. T_J is calculated from the user-entered T_A and the power calculation of typical room temperature.
- I/O power consumption is based on an output loading of 5 pF. You can change this capacitive loading.
- You can estimate power dissipation and current for each type of power supply, V_{CC} and V_{CCIO}.
- The nominal V_{CC} is used by default to calculate power consumption. A lower or higher V_{CC} can be chosen from a list of available values.
- θ_{JA} can be changed to better estimate the operating system manually or by entering Airflow in Linear Feet per Minute (LFM) along with a Heat Sink options.
- The activity factor (AF) is defined as the toggle rate of the registered output. For example, assuming that the input of a flip-flop is changing at every clock cycle, 100% AF of a flip-flop running at 100 MHz, is 50 MHz.
- The default activity factor for logic is 10%.
- You can import the VCD file from the simulation to get activity factor based on the simulation. It is to be noted that the AF from VCD is as good as the coverage in the simulation.
- Unused I/O are configured as LVCMOS Inputs with weak internal pull ups.
- You can import the Frequency from a trace report (TWR).

- The operating junction temperature range for commercial grade devices is 0°C to 85°C, and Industrial grade devices is –40°C to 100°C. For details, refer to the DC Electrical Characteristics section of Certus-NX Family Data Sheet (FPGA-DS-02078).
- For thermal impedance, Power Calculator default value is based on a medium size board (6" × 6", 6 layers), with no heatsink and 200 LFM airflow. This can be changed as needed under Thermal Profile section in the tool.

5. Thermal Management

To improve reliability and prevent device failure, all electronic devices are required to dissipate the heat generated while running. Thermal management refers to the techniques used to improve heat dissipation. The methods include use of heatsinks, fans for air cooling, and also other forms of cooling like liquid cooling in modern computers.

Certus-NX devices are designed to be low power. By combining power reduction techniques and designing for low power, the average power consumption and heat generated can be reduced. This section covers the understanding and ways to improve thermal management for applications using Certus-NX devices.

5.1. Thermal Impedance and Airflow

A common method for characterizing a packaged device thermal performance is with Thermal Impedance, represented by θ. For a semiconductor device, thermal resistance indicates the steady state temperature rise of the die junction above a given reference for each watt of power (heat) dissipated at the die surface. Its units are degree Celsius per Watt (℃/W).

The most common examples are:

- θ_{JA}, Thermal Resistance Junction-to-Ambient (in℃/W)
- θ_{JC}, Thermal Resistance Junction-to-Case (in℃/W)
- θ_{JB}, Thermal Resistance Junction-to-Board (in℃/W)

Knowing the reference temperature such as the ambient, case, or board temperature, the power, P, and the relevant θ value, the junction temperature can be calculated per following equations.

- $T_J = T_A + \theta_{JA} * P$
- $T_J = T_C + \theta_{JC} * P$
- $T_J = T_B + \theta_{JB} * P$

Where T_J, T_A, T_C, and T_B are the junction, ambient, case/package, and board temperatures (in℃), respectively. P is the total power dissipation of the device.

θ_{JA} is commonly used with natural and forced convection air-cooled systems. θ_{JC} is useful when the package has a high conductivity case mounted directly to a PCB or heatsink. And θ_{JB} applies when the board temperature adjacent to the package is known.

To improve airflow effectiveness, it is important to maximize the amount of air that flows over the device or the surface area of the heat sink. The airflow around the device can be increased by providing an additional fan or increasing the output of the existing fan. If this is not possible, baffling the airflow to direct it across the device may help. This means the addition of sheet metal or objects to provide the mechanical airflow guides to guide air to the target device. Often the addition of simple baffles can eliminate the need for an extra fan. In addition, the order in which air passes over devices can impact the amount of heat dissipated.

5.2. Thermal Management in Power Calculator

Lattice Radiant software Power Calculator utilizes the ambient temperature (°C) to calculate the junction temperature (°C) based on the θ_{JA} for the targeted device. You can also provide the airflow values (in Linear Feet per Minute or LFM, that is also the same as Cubic Feet per Minute) to obtain a more accurate junction temperature value.

Thermal Environment options in the Power Calculators provide a thermal impedances for JEDEC (4”× 4”, 2S2P), small (6”× 6”, 6 layered board), medium (8”× 8”, 8 layered board), and large (10”× 10”, or larger board). There are also options to select copper heatsinks of different sized fins. These impedances and options are provided as a guidance. You have an option to provide their own thermal impedance, too.

As each application board can be different, it is recommended that accurate thermal impedance be provided. These can be obtained by measuring using a thermal lab or by using thermal simulation software.

5.3. DELPHI Models

DELPHI Models are thermo-mechanical models that can be used to simulate thermal behavior of the electronic devices in a system. These tools can simulate the thermal behavior of the system and predict the thermal impedance for each component. The thermal impedance obtained using simulation methods can be entered in the Thermal Environment in Power Calculator.

DELPHI Models for Certus-NX device can be downloaded from the web, and they are compatible with Mentor Graphics' FloTHERM® and Ansys Icepak tools.

6. Conclusion

Certus-NX devices provide you a number of options for managing power, and the Power Calculator tool complements by calculating power in different states of the device.

By utilizing the user-friendly interface to access these features in Lattice Radiant software, applications can utilize these features to maximum extent, and have predictable and reliable performance for these devices.

References

For more information, refer to the following documents:

- Certus-NX Family Data Sheet (FPGA-DS-02078)
- sysCLOCK PLL Design and Usage Guide for Nexus Platform (FPGA-TN-02095)
- sysI/O Usage Guide for Nexus Platform (FPGA-TN-02067)
- Memory Usage Guide for Nexus Platform (FPGA-TN-02094)
- I^2C Hardened IP Usage Guide for Nexus Platform (FPGA-TN-02142)

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.1, August 2020

Section	Change Summary
Thermal Management	Changed the wording in the introductory paragraph.

Revision 1.0, July 2020

Section	Change Summary
All	Initial release.

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