38-to-38 Bit Crosspoint Switch Using the ispMACH™ 51024VG

Introduction

Applications such as network switching, bus interfacing, distributed systems and reconfigurable computing frequently use Crossbar or Crosspoint switches. Crosspoint switches of varying sizes ranging from 8-bit to 128-bit are available in the market. This application note demonstrates the features of the Lattice ispMACH 51024VG by implementing a 38-to-38 bit crosspoint switch.

Overview

In an N-to-N bit crosspoint switch, the N sources can be connected to any of the N destinations available. Figure 1 shows an N-to-N bit crosspoint switch. The figure shows that Source 1 is now connected to the destination Destn 3. The dot denotes the connection made.

Figure 2 shows the 38-to-38 bit crosspoint switch implementation. The design consists of thirty-eight 38-to-1 multiplexers. Two 6-bit address lines (Sel[5:0] and Address[5:0]) are used to select the source and destination. The destination address lines (Address[5:0]) go to a decode logic which generates 38 enable signals (Enb[0] .. Enb[37]). The select lines to each of the multiplexers are latched by the respective enable signals (Enb[0] .. Enb[37]). Latching the select lines to the multiplexers ensures that the source line continues to be connected to the same destination, even if the destination address changes. This way, a single source can reach multiple destinations. Alternatively, other sources can be connected to any of the available destinations without disturbing the existing connections. The input to each of the select latches comes from the source address lines (Sel[5:0]). The data from the output of the multiplexers are registered to pipeline the system. The registers in the I/O cells are used for this purpose to reduce the Clock-to-Output delay.

ispMACH 51024VG Design Implementation

The 38-to-1 multiplexer functions in the design have 38 data inputs and six select inputs. This makes it a very wide input function (44 inputs). Most other CPLDs do not offer wide input logic blocks and such multiplexer functions would take up multiple levels of logic. Because the ispMACH 51024VG has 44-input Generic Logic Blocks (GLBs), this design will fit into an ispMACH 51024VG and only use 340 macrocells.

Figure 1. N-to-N Bit Crosspoint Switch

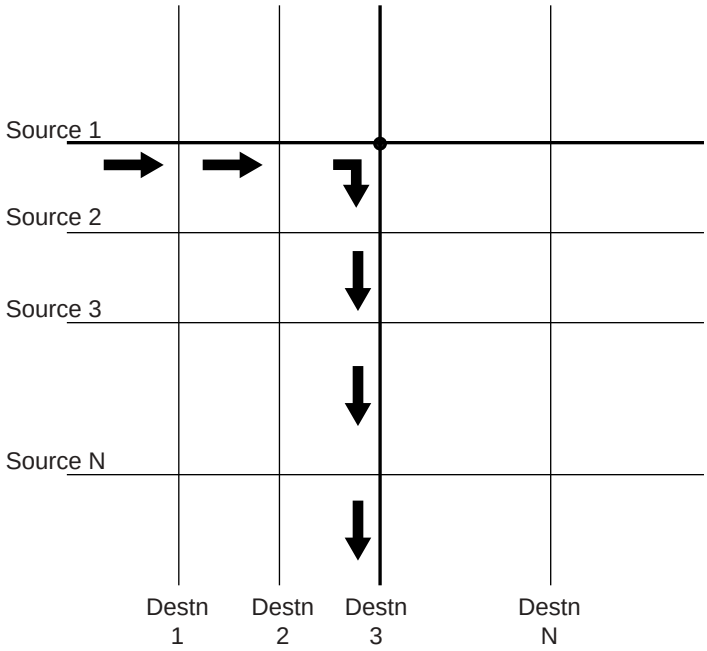

Figure 2. 38-to-38 Bit Crosspoint Switch Implementation

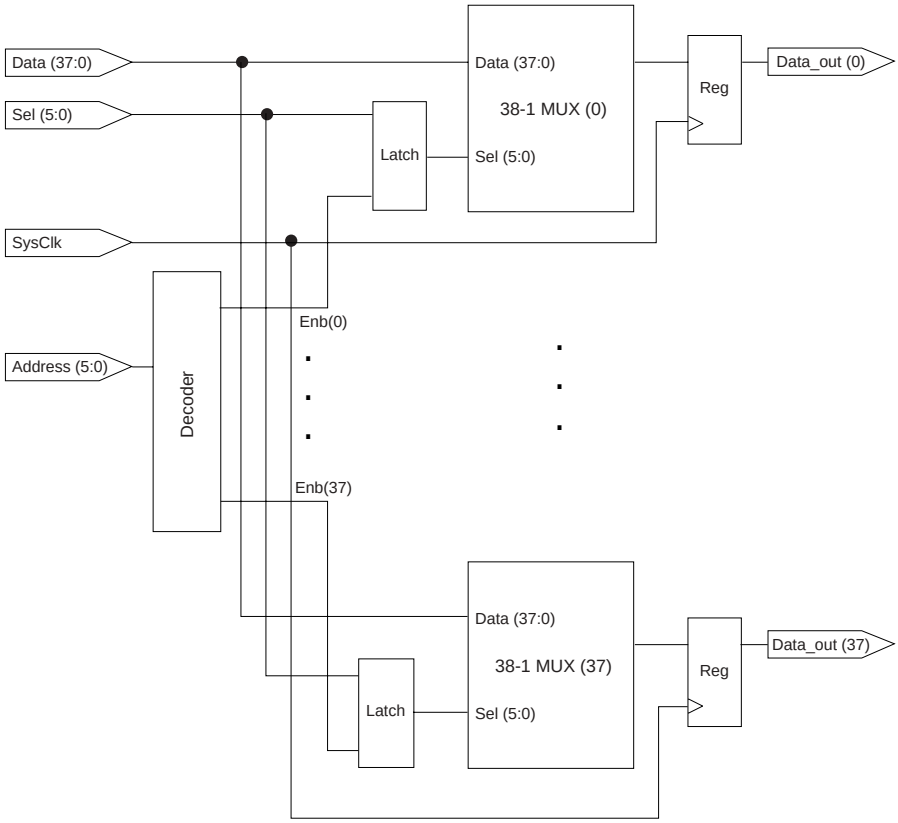

Table 1. Results

Parameter	ispMACH 51024VG-75F676C
Macrocells (Logic Elements) Used	536 out of 1024
Macrocell Utilization	52.3%
Setup Time (t_{SU})	14.8ns
Clock-to-Output Delay (t_{CO})	5.0ns

Conclusion

The Lattice SuperBIG™ ispMACH 51024VG CPLD with its superior and innovative architecture is targeted for applications requiring wide input functions, I/O capture registers and an internal tristate bus.

Technical Support Assistance

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