SONET Interrupt Controller

Introduction

SONET (Synchronous Optical Network) is a standard for transmission of data over optical fiber. The SONET format allows different types of formats to be transmitted over the same fiber optic line.

The various types of formats (such as DS-1, CEPT or DS-3) use different digital signal hierarchies, encoding techniques and multiplexing strategies. Therefore, communication between different networks requires a complicated multiplexing/demulitplexing and encoding/decoding process to convert a signal from one format to another.

To solve this problem, SONET standardizes transmission rates and formats. The different types of formats are multiplexed, using a SONET switch or SONET terminal, to form a single synchronous SONET signal at a line rate of 51.48Mbps. These electrical SONET signals are then converted to optical signals for transmission over the optical fiber.

SONET signals may be multiplexed to create higher line rates. Currently, the most widely supported line rates are 51.84Mbps and 1244.16Mbps (24 SONET signals multiplexed together).

This application note demonstrates the use of a Lattice ispMACH™ 51024 device as a SONET switch interrupt controller.

Overview

The ispMACH 51024VG is used in the port shelf section of the SONET switch. The device interacts with the SONET ports and the embedded microprocessor to generate the master interrupt for the switch (Figure 1). The ispMACH 51024VG receives the interrupt sources from the port and the microprocessor provides the address, read, write, clock and enable signals to the device.

Implementation

The implementation of the interrupt controller into the ispMACH 51024VG device can be divided into nine major functions: Decode Control Bit Generation, Select Control Bit Generation, Input Capture Registers, Enter/Exit Event Detection, Mask Bit Generation, Interrupt Register Generation, Clear Interrupt Register Control Bit Generation, Data Bus Selection and Master Interrupt Generation (Figure 2).

The ispMACH 51024VG receives a 16-bit address bus from the microprocessor. This address bus is decoded to generate the decode bus. The decode bus is used in the Mask Bit Generation, Interrupt Register Generation and Clear Bit Generation.

The decode bus and the Read signal from the microprocessor are used to generate the select bits for the Data Bus selection. The decode bus, the Write signal from the

Figure 1. SONET Switch Port Shelf Section

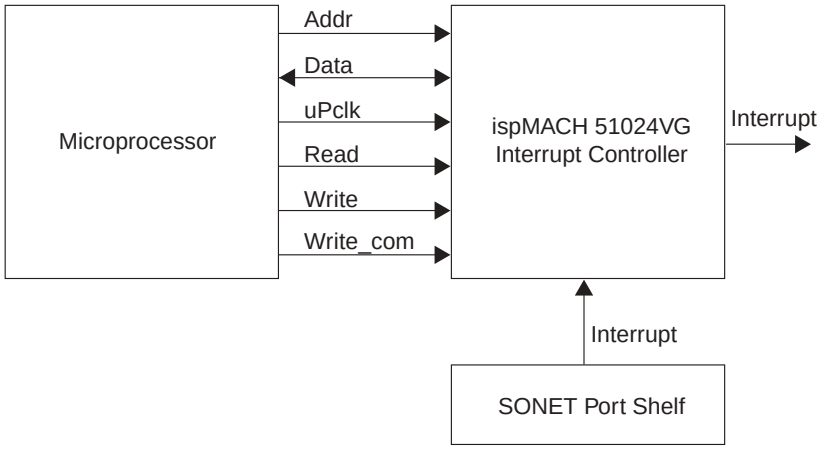
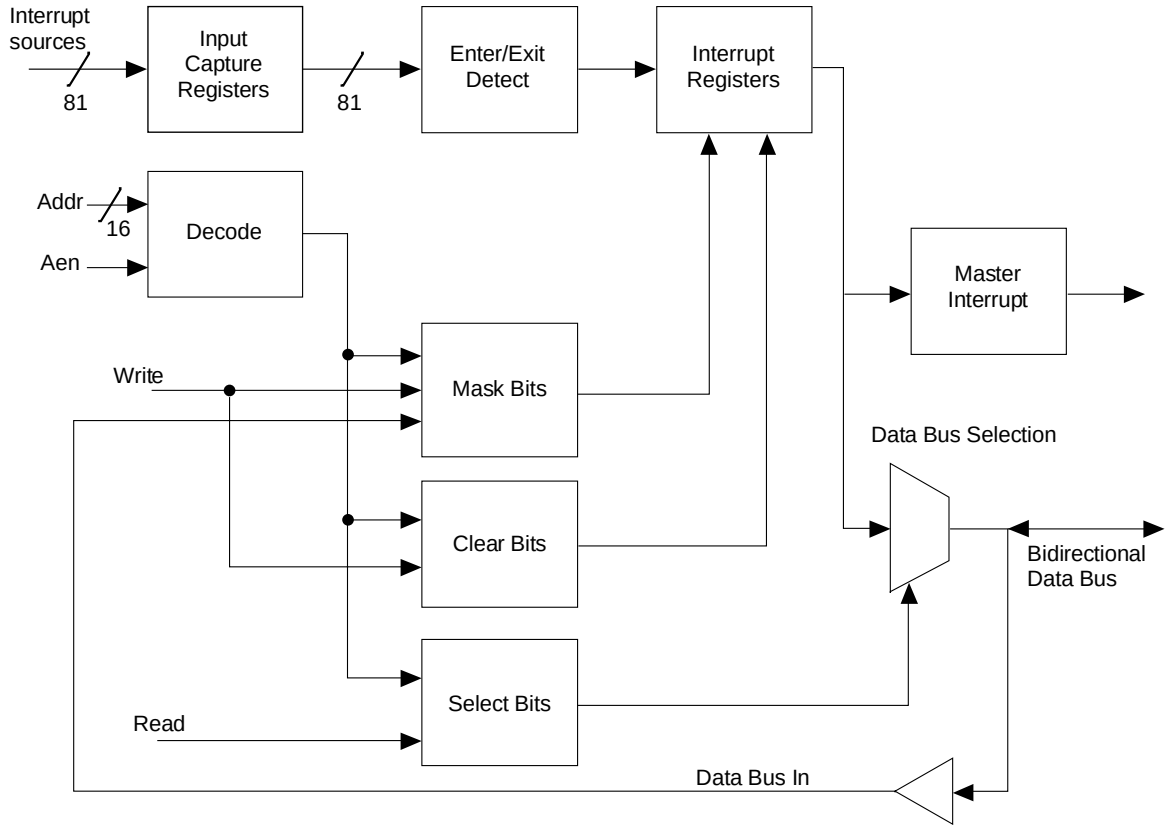


Figure 2. SONET Interrupt Controller Implementation



microprocessor and the input of the bi-directional data bus are used to generate the mask bits and to clear bits for the interrupt registers.

The Input Capture Registers capture the asynchronous interrupt sources in the I/O cell of the ispMACH 51024VG to prevent metastablity. These interrupt sources are sampled using the IOC registers and a clock from the microprocessor to form a synchronous interrupt source. The synchronous interrupt sources are used to detect an entering or exiting event on the interrupt source.

The Enter/Exit Event, Mask Bits and Clear Bits are used to generate the interrupt registers. The interrupt registers will be active on an entering or exiting event, unless the appropriate mask bit is active. The mask bits are used to prevent the interrupt register from determining an entering or exiting event. The clear bits are used as a synchronous clear for the interrupt registers.

The interrupt registers are used to generate the main function of the device, the master interrupt. The interrupt registers and the sampled interrupt sources (not shown in Figure 2) are also combined to feed into the data bus selection. The data bus selection is a multiplexer that will select the appropriate interrupt register bits and sampled interrupt bits. The Select Bit Generation section generates the select for the multplexer. The output of the bus feeds into the output of the bidirectional data bus.

Results

As seen in Table 1, the interrupt controller takes advantage of the efficient routing structure of the ispMACH 51024VG. This complex design requires only two GLB levels of delay and 539 macrocells.

Table 1. ispMACH 51024VG Results

Macrocells	539
GLBs	26
Pins	177
Input Registers	104
Macrocell Utilization	52.6%
Average Inputs per GLB	40.8
Clock Period	9.8ns
Maximum Frequency	102MHz

Conclusion

Lattice's ispMACH 51024 architecture, with wide inputs and flexible product term sharing, is optimized to efficiently implement large complex designs. The implementation of a SONET interrupt controller shows that large complex designs can be efficiently implemented within the ispMACH 51024.

In comparison to other CPLDs, the ispMACH 51024 is the largest and most flexible CPLD available in the market. The device offers clear architectural advantages over competing FPGAs, making the ispMACH 51024 an excellent choice for large, complex designs.

The source code files for this design are available from your local Lattice Field Applications Engineer or by e-mail from the Lattice Semiconductor Applications Engineering Group.

Technical Support Assistance

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