Powering Up and Programming the ispPAC-POWR1208

April 2003 Application Note AN6047

Introduction

This application note discusses the output pin modes and characteristics of the ispPAC®-POWR1208 during programming and power up. Special attention is given to interfacing external circuitry associated with controlling DC-to-DC converters (bricks) and other power-supply related circuits such as low-drop-out regulators. The operational modes of the output pins include open-drain pull down, open-drain high-z, and charge pump current source. The active mode of certain pins is a function of the following factors; programmed function, programmed reset level, state of the $\overline{\text{RESET}}$ pin, stage of power-up, and programming the device. The specific factors that affect the mode of the high-voltage (FET-driver), logic (open-drain), and comparator buffer pins will be discussed in the sections that follow.

Before the discussion on the output pins, the actual powering up of the ispPAC-POWR1208 will be covered in two separate sections; one deals with the power-on-reset ($\overline{\text{POR}}$) circuitry and the other deals with the startup of the internal clock. In the $\overline{\text{POR}}$ section it will be shown that both V_{DD} and CREF must reach their respective thresholds before the ispPAC-POWR1208 starts the sequence. In the clock section, the relationship between the start of the internal clock and the start of the sequence is described.

Furthermore, we discuss how best to interface with the in-system-programming circuitry and the ispDOWNLOAD® cable. An example circuit is provided that will support both device programming at 3.3V and operation at 5V. This simple circuit provides power only to the ispPAC-POWR1208 and ispDOWNLOAD cable to prevent bricks (DC-to-DC converters) and other power supply circuits from powering up (without control) during programming.

A design example is also presented. This example illustrates two methods of controlling an example brick and the characteristics of each, as well as the potential pitfalls and benefits of each.

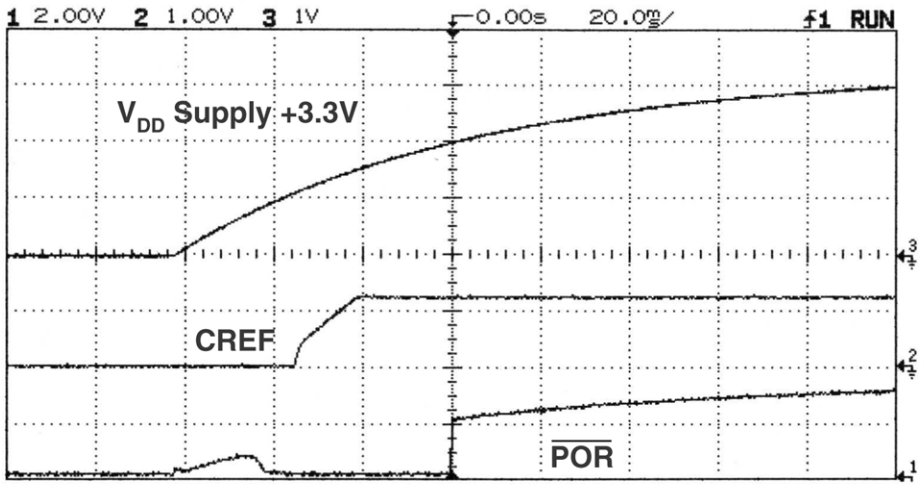
Power-on Reset

It is appropriate to first describe the function of the power-on-reset ($\overline{\text{POR}}$) circuitry. The oscilloscope plot in Figure 1 best illustrates the $\overline{\text{POR}}$ pin with a slow supply. The top trace shows the V_{DD} supply slowly rising from zero to 3.0V (in 160ms). The bottom trace shows the output of the $\overline{\text{POR}}$ pin that is connected to an external 10 kΩ pull-up resistor. The pull-up resistor is required because the $\overline{\text{POR}}$ output is open-drain. The center trace is the CREF pin of the ispPAC-POWR1208 that has the required 0.1 µF external capacitor connected to it.

The time between V_{DD} starting to rise and the rising edge of $\overline{\text{POR}}$ will be referred to as "during $\overline{\text{POR}}$." Before V_{DD} reaches 1.0V the external pull-up resistor pulls the $\overline{\text{POR}}$ pin up to the supply, because the internal circuitry has not yet turned on. After V_{DD} reaches 1.0V, $\overline{\text{POR}}$ is actively driven LOW until it goes HIGH, which happens in this case when V_{DD} crosses 2.0V (typical). On the rising edge of $\overline{\text{POR}}$, the internal programmable logic device (PLD) will be reset, including all the macrocells that control the output pins. Thus, it is when $\overline{\text{POR}}$ rises HIGH that the output pins will assume their respective reset states. In subsequent sections, the time after the rising edge of $\overline{\text{POR}}$ will be referred to as "after $\overline{\text{POR}}$."

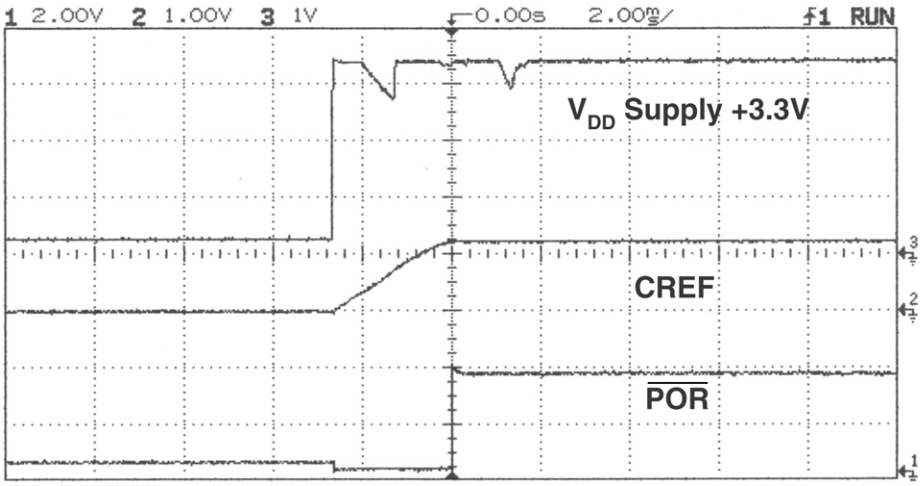
In contrast to the slow supply shown in Figure 1, an "instant-on" scenario is shown in Figure 2. Here the ispPAC-POWR1208 is powered up very quickly using a mechanical switch (note the contact bounce on the supply trace) and a 3.3V supply that has already stabilized. The time scale in this plot is ten times faster than that of the previous plot to reveal the detail of the traces. Now the rising edge of $\overline{\text{POR}}$ does not occur when the V_{DD} pin crosses the threshold. Rather the rising edge of $\overline{\text{POR}}$ occurs when the CREF pin reaches its threshold, which in this case is 1.2V (typical).

Figure 1. Power-on Reset of the ispPAC-POWR1208



From both of these plots, it can be seen that the rising edge of $\overline{POR}$ occurs after V_{DD} AND CREF cross their respective thresholds. Because of this condition, the "during $\overline{POR}$" time can vary from a minimum of 3 ms to 60 ms or more, depending upon the rise time of the supply. This time can become important, depending upon the power circuit and the type of output pin that is controlling it. This will be discussed in more detail in the following sections.

Figure 2. Instant Power-On Reset



Starting the Clock

The start-up of the internal clock may be important in some applications, as it will determine how long the outputs will stay in their reset state. As stated earlier, the output pins are placed in their reset-state at the rising edge of $\overline{POR}$; however, they may later change as a function of the LogiBuilder sequence. In Figure 3, the top trace is the V_{DD} supply (+3.3V) pin and the bottom trace is the $\overline{POR}$ pin. The center trace is the clock pin (CLK) pin, which has an external 10 kΩ pull-up at its open-drain output. Here we can see that the internal oscillator does not start until after the rising edge of $\overline{POR}$.

In Figure 4, we have zoomed in on the rising edge of $\overline{POR}$, and moved the probe for the top trace from the supply to an output. In the LogiBuilder sequence, the output is set low in the very first step. Thus, the first rising edge of the

clock occurs one clock period after the rising edge of $\overline{POR}$, which advances the sequencer from step zero to step one and sets the output low at the same time.

Figure 3. Power-On Reset of the Internal Clock

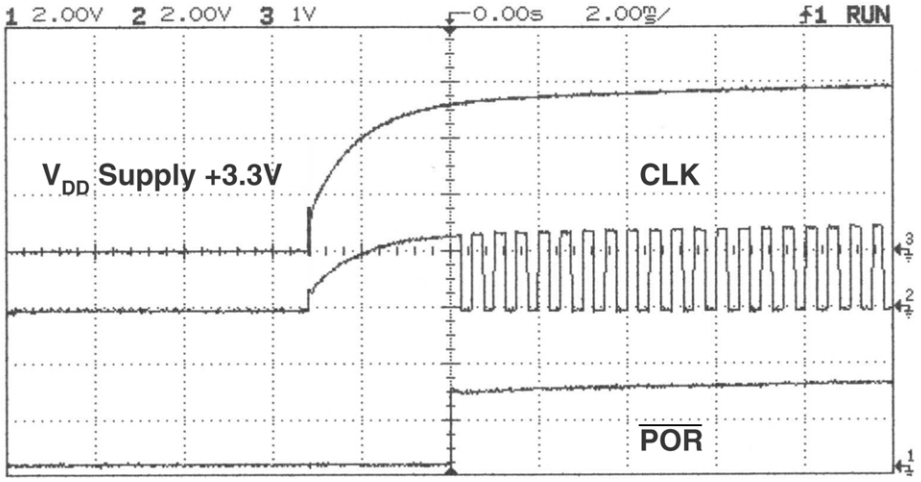
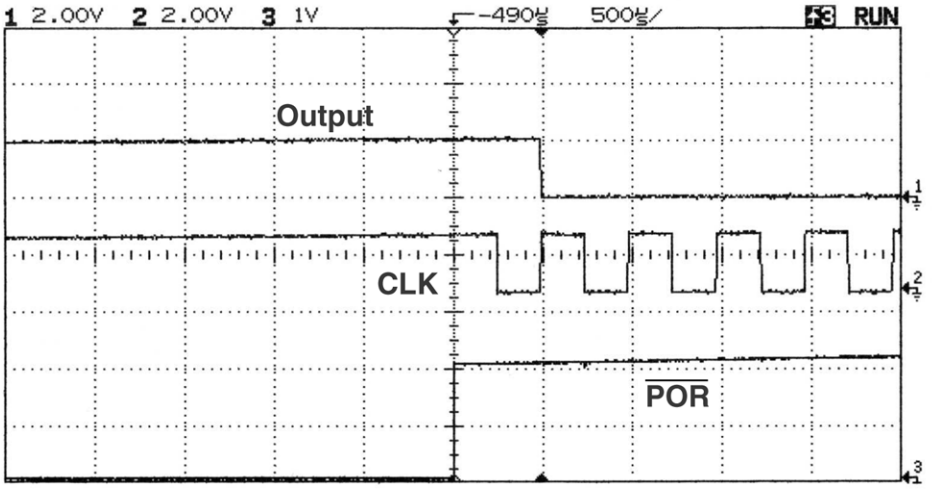


Figure 4. Clock Start-Up and Step Zero



High Voltage FET-Driver Pins

The ispPAC-POWR1208 has four FET driver pins that can be configured (using PAC-Designer®) as either charge-pump outputs to turn on power-FETs or as open-drain outputs for generating control or logic signals. When the ispPAC-POWR1208 is shipped from the factory, the outputs are configured as charge-pumps. In this mode, the outputs remain pulled down both during $\overline{POR}$ and after $\overline{POR}$ and while the device is being programmed (as listed in Table 1). Thus the FET drivers remain off, in all situations, until the sequencer ramps them up. For additional information regarding the capabilities of the FET-driver outputs, please read application note AN6043 *Using the ispPAC-POWR1208 MOSFET Driver Outputs.*

In the tables that follow, the first column describes the state of the device or pin, and the next column lists the state of the output pin during $\overline{POR}$. The third column describes the state of the output pin after $\overline{POR}$ or when the $\overline{RESET}$ pin is activated (pulled down). The last column shows the state of the output pin during programming or erasing.

When the FET-driver output pins are programmed as open-drains (using PAC-Designer), the output driver for the pin is high impedance (high-z) during $\overline{POR}$. However, during programming the output is pulled down. After $\overline{POR}$, or when the $\overline{RESET}$ pin is active, the state of the pin's output is determined by how its reset level was configured using PAC-Designer. If the reset level for the pin is configured to LOW then the output pin will go LOW after $\overline{POR}$ or when the $\overline{RESET}$ input pin is active (see Table 1 and Figure 5). Alternatively, if the reset level for the pin is configured as HIGH then the output pin will be HIGH (with an external pull-up resistor) both during and after $\overline{POR}$ or when the $\overline{RESET}$ input pin is active (see Table 1 and Figure 6).

Table 1. FET-Driver (High Voltage) Pin Modes

Part Condition	Power-Up During $\overline{POR}$	$\overline{RESET}$ Pin or $\overline{POR}$	Programming or Erasing
Programmed HVOUT (as shipped)	Pull Down	Pull Down	Pull Down
Programmed OD (RL = LOW)	High-Z	Pull Down	Pull Down
Programmed OD (RL = HIGH)	High-Z	High-Z	Pull Down

Notes: OD stands for open drain. RL stands for reset level.

Figure 5. Power-up of Open-Drain Output (Reset Level = LOW)

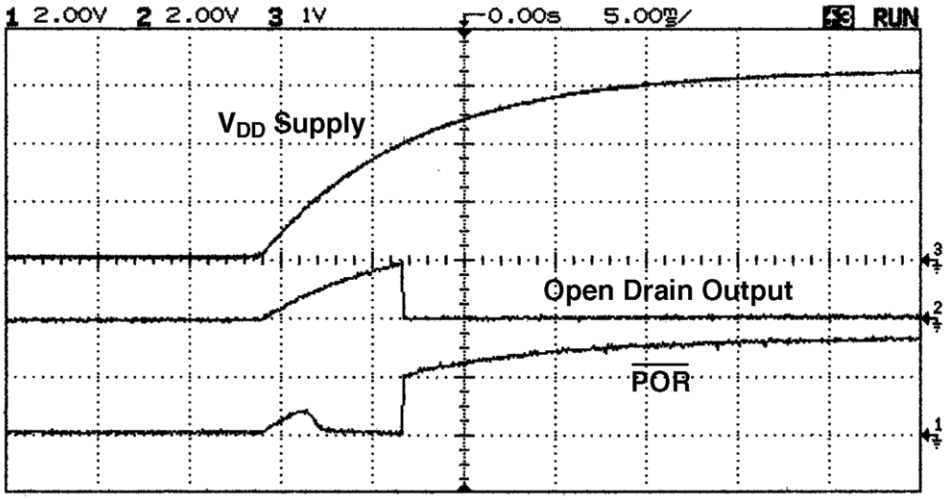
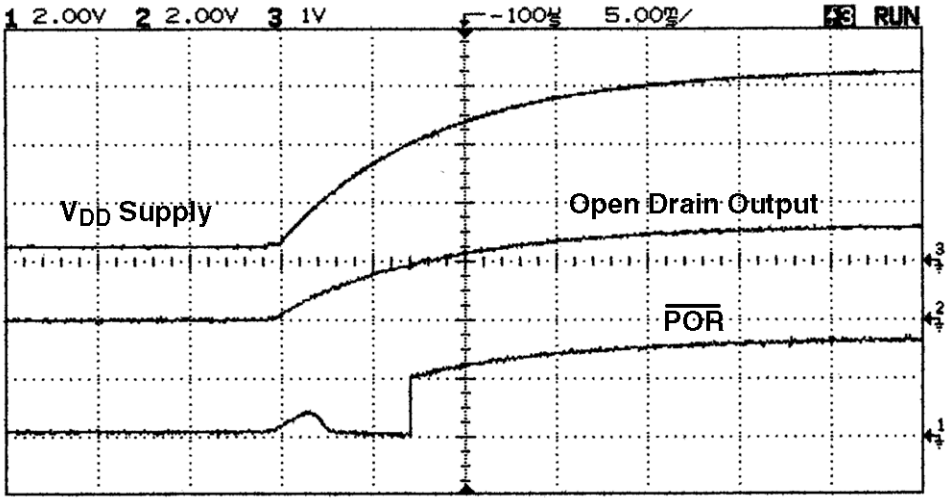


Figure 6. Power-up of Open-Drain Output (as Shipped, Reset Level = HIGH)



Logic Open-Drain Pins

The ispPAC-POWR1208 has four logic pins that have open-drain outputs. In all conditions, the outputs are in the high-z state until after $\overline{POR}$. The outputs are also high-z when the part is being erased or programmed. The state of the logic outputs after $\overline{POR}$ depends on how the reset level for the pin is configured. From the factory (as shipped) the reset level is configured as HIGH and the output will be HIGH (with an external pull-up resistor) both during and after $\overline{POR}$ or when the $\overline{RESET}$ input pin is active (see Table 2 and Figure 6). Alternatively, if the reset level is configured as LOW, then the output will go LOW after $\overline{POR}$ or when the $\overline{RESET}$ input pin is active (see Table 2 and Figure 5).

Table 2. Open-Drain (Logic) Pin Modes

Part Condition	Power-Up During $\overline{POR}$	$\overline{RESET}$ Pin or $\overline{POR}$	Programming or Erasing
Reset Level = HIGH (as shipped)	High-Z	High-Z	High-Z
Reset Level = LOW	High-Z	Pull Down	High-Z

Comparator Buffer Pins

In some cases, the open drain comparator buffer pins may be used to control or enable DC-to-DC converters or other circuits. Therefore, for a complete discussion of all the output pins, Table 3 describes the behavior of these pins for circuits or systems that may incorporate these outputs. Since the buffers themselves are not programmable, Table 3 does not contain an entry for the as shipped condition, although the default trip point is 1.036V.

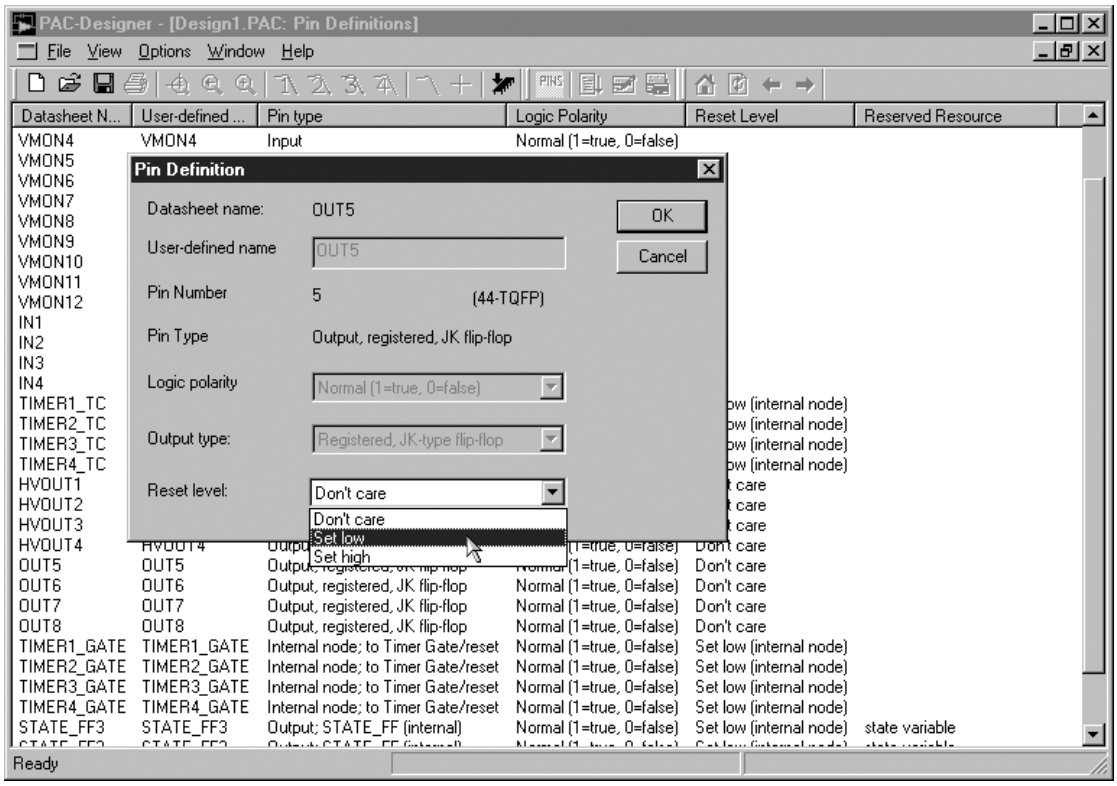
Table 3. Comparator Buffer Pin Modes

Part Condition	Power-Up During $\overline{POR}$	$\overline{RESET}$ Pin or $\overline{POR}$	Programming or Erasing
VMON < Trip Point	High-Z	Pull Down	High-Z
VMON > Trip Point	High-Z	High-Z	High-Z

Using PAC-Designer to Configure the Reset Level

As mentioned earlier, in the previous sections, the reset level of the open-drain outputs can be configured in PAC-Designer. This is done using the **PINS** window in PAC-Designer (see Figure 7). The **PINS** window is accessible from the LogiBuilder window by clicking on the "**PINS**" tool or the "**Pin definitions**" item from the **View** menu. To open the "**Pin Definition**" dialog box, double-click on the desired output pin that is listed in the **PINS** window. If the reset level for the pin is configured to "Set low" then the pin will go LOW after $\overline{POR}$ or when the $\overline{RESET}$ input pin is active. Alternatively, if the reset level is configured as "Set high" then the pin will be high-z (or is pulled HIGH from an external pull-up resistor) after $\overline{POR}$ or when the $\overline{RESET}$ input pin is active.

Figure 7. PAC-Designer PINS Window is Used to Set the Reset Level of the Output Pins



One application of the open-drain outputs is to drive the enable or control pin of DC-to-DC converters (bricks). In such applications the ability to specify the reset level of the output pins is a valuable feature, because the ispPAC-POWR1208 can interface to a variety of bricks and control circuits. However, during programming the output mode may be different than reset mode and multiple bricks may turn on with less than desirable results. Therefore, it is strongly recommended that only the ispPAC-POWR1208 be powered up during programming.

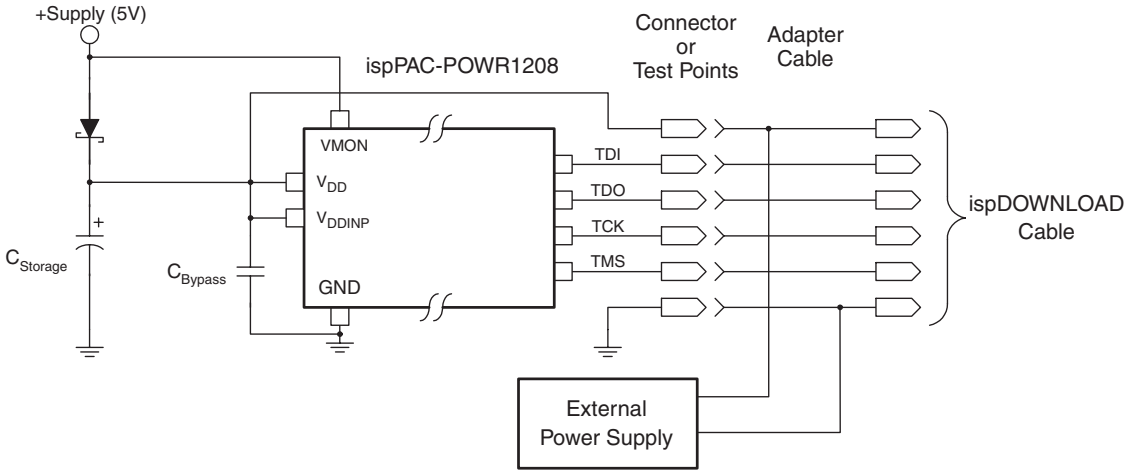
Power-Safe Programming Circuit

In many designs, the outputs may turn on bricks or enable supplies that should be off during programming. This is because of the different modes of the output pins and the variety of brick control logic available. In such designs, where the supplies or bricks are enabled, it is strongly recommended that only the IspPAC-POWR1208 receive power during programming to prevent spurious activation of the controlled supplies.

Although a simple jumper could suffice, a more elegant solution is offered in the following circuit. This circuit is an example of how the ispPAC-POWR1208 can be powered for both programming and normal operation. During programming, power is presented to the ispPAC-POWR1208 and the ispDOWNLOAD cable by using a modified cable, an adapter, or test fixture and an external supply. The diode prevents the rest of the circuitry from receiving power and provides a way to program the device. During normal operation, the Schottky diode is forward biased from the +Supply to energize the ispPAC-POWR1208.

An added feature of this circuit is that, during power down, the diode and storage capacitor will keep the ispPAC-POWR1208 powered up for a short time while the main power is decaying (typical I_{DD} is less than 10 mA). The ispPAC-POWR1208 can be used to monitor the +Supply to see when it falls below a certain threshold then generate a “Power Fail” signal (if needed) and sequence off the supplies, for a smooth shut-down.

Figure 8. Supplying Power to the IspPAC-POWR1208 for Programming



From Programming to Sequencing

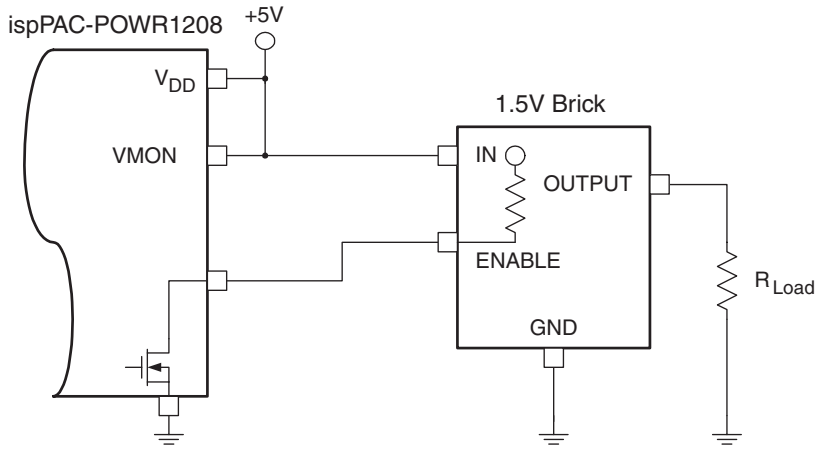
After programming, the sequence starts from step zero. However, a reset signal is not sent to the output macrocells following programming. Thus, output pins may not be in the desired state for the start of the sequence. This can be avoided by cycling the power after programming or using the $\overline{\text{RESET}}$ input. Also, the $\overline{\text{RESET}}$ pin could be held LOW during programming and then released to start the sequence.

Design Examples with Positive-Logic Bricks

When the reset level of open-drain outputs are configured LOW, a short high-z pulse will occur during $\overline{\text{POR}}$, as was seen in the previous sections. When such outputs are connected to the enable or control input of a brick with positive logic, the brick will turn on. If multiple bricks are all controlled in like manner (even using separate open-drain outputs), all the supplies could turn on at the same time. This could result in latch-up, excessive current flow, or permanent damage to the devices that are powered by the bricks. To see how this is possible and how to design an interface that will prevent such a scenario, let's look at a couple of examples.

In the following example, a brick that converts 5V to 1.5V (5 Amp) is controlled from an open-drain output of the IspPAC-POWR1208 (see Figure 9). When the ENABLE pin is grounded, the brick is turned off, and when the ENABLE pin is allowed to float, the brick is turned on. Note that several other types of brick enables are available and they are discussed in the application note AN6046 *Interfacing the ispPAC-POWR1208 with Modular DC-to-DC Converters.*

Figure 9. ispPAC-POWR1208 Controlling Positive Logic Brick



To control the brick in an orderly fashion, a simple LogiBuilder sequence was used to monitor the +5V supply. When the +5V supply reaches 4.5V, the output instruction will "Turn On/Assert" the open-drain (pin goes HIGH with external pull-up). The sequence was compiled and downloaded into the evaluation board (with power removed from the brick).

Figure 10. Power-up of 1.5V Brick

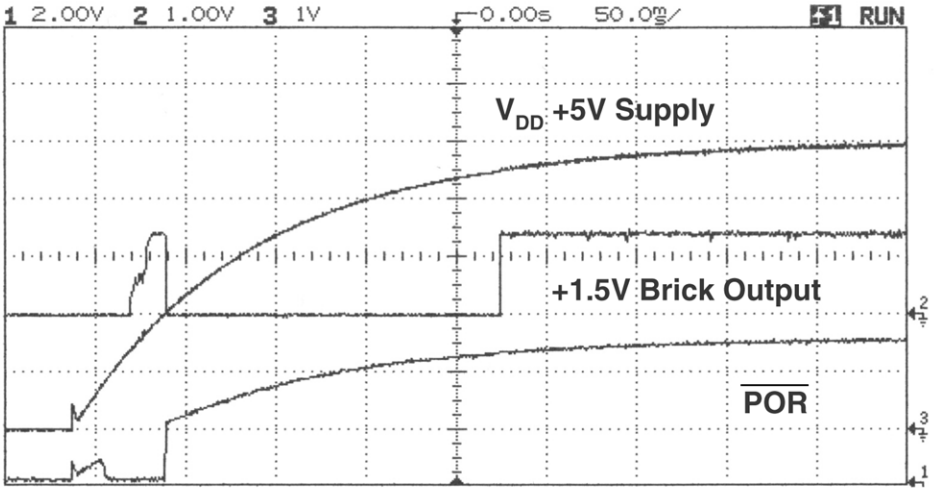
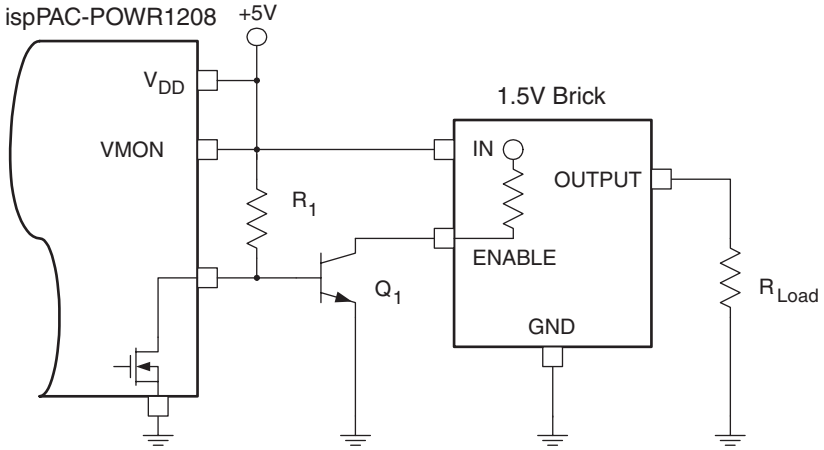


Figure 10 is the resulting oscilloscope plot with the top trace showing the slow ramp of the power supply. The center trace is the output of the brick, which has a 3 A load on it. The bottom trace is $\overline{POR}$. Notice that the 1.5V output of the brick reaches full voltage for 10 ms during $\overline{POR}$. This is the result of the open-drain output floating up as was seen in Figure 5. After $\overline{POR}$, the brick is disabled and the 1.5V output is off until the +5V supply reaches 4.5V, which takes about 200 ms, and then the brick is turned on by the sequence.

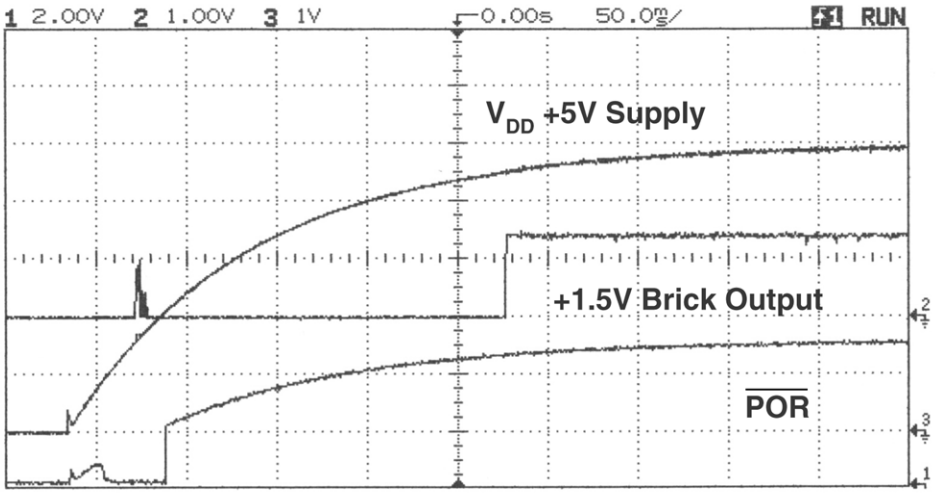
In many designs, this full voltage pulse may be too short to cause any problems. Also, after $\overline{POR}$ the bricks will be off and latch-ups should be reset, and then the bricks can be sequenced up in proper order. Additional things that would reduce the effectiveness of this pulse during $\overline{POR}$ include; having to charge a lot of by-pass and storage capacitors, or the brick output is slow or has just enough current capacity for the active load. In this example, a 6 A output is powering a 3 A passive load without any capacitors. However, if a design is sensitive to this type of pulse, a simple transistor inverter can be an effective solution (see Figure 11).

Figure 11. NPN Inverter to Enable 1.5V Brick



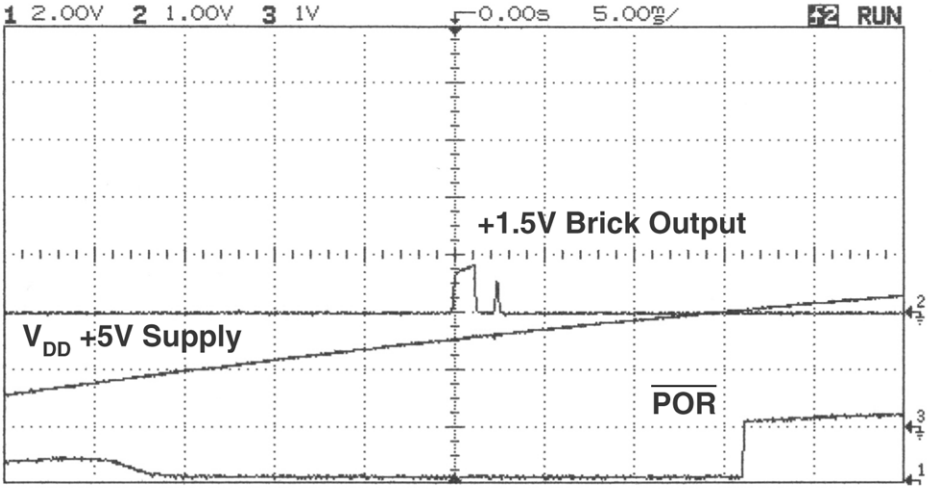
In this circuit Q_1 inverts the output of the open-drain output and R_1 provides both the bias of Q_1 and pull up on the open-drain. The reset level of the output pin was changed to HIGH and the output statement in the LogiBuilder sequence was changed to “Turn Off/Deassert” the open-drain (pin is pulled down). The resulting oscilloscope plot can be seen in Figure 12, where the 1.5V output of the brick fails to reach full voltage until it is sequenced on (when the input supply reaches 4.5V).

Figure 12. Power-up of 1.5V Brick Using an NPN Transistor



Notice there is still a short pulse in the output of this brick near the same time as in Figure 10. To determine the source of this pulse, the ENABLE pin of the brick was tied to ground and the measurement was repeated. In Figure 13 the time base is increased to see the details of the output pulse. Note that for this particular brick, the output sustains a 0.7V output for 1ms. A conclusion from this measurement is that some bricks may produce spurious output pulses (as the supply ramps up) even with their ENABLE pins disabled.

Figure 13. Power-up of 1.5V Brick with Enable Pin Grounded



Summary

To provide maximum protection to complex systems or boards, it is strongly recommended that power be applied to only the ispPAC-POWR1208 and ispDOWNLOAD cable during erasing or programming. This is easily accomplished using a few additional discrete components or jumpers. The reset level of the open-drain pins can be con-

figured using PAC-Designer to accommodate the plethora of power supply circuits and control logic. Whenever possible, select bricks that use negative-enable-logic and configure the reset level of ispPAC-POWR1208 open-drains to set HIGH. This will prevent the bricks from turning on during $\overline{\text{POR}}$. Alternatively an external inverter can be used to keep positive-logic bricks turned off during $\overline{\text{POR}}$. Finally, some bricks and power supplies may have momentary outputs during power-up, regardless of what is controlling them.

Related Literature

- ispPAC-POWR1208 Data Sheet
- AN6043 Using the ispPAC-POWR1208 MOSFET Driver Outputs
- AN6046 Interfacing the ispPAC-POWR1208 with Modular DC-to-DC Converters

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