Power Estimation in the ispGDX2 Family

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Introduction

The ispGDX2™V/B/C devices are built from the latest 1.8V core $E^2CMOS^®$ technology. The ispGDX2V/B device family uses an internal voltage regulator to interface with the 3.3V/2.5V power supply. As a result, a given ispGDX2V/B device will have a higher static power component compared to the similar density 1.8V core ispGDX2C device. The design of each of these device families design is based on the advanced low-power electrically erasable non-volatile memory cell with a full CMOS logic design approach.

Power Calculation

This technical note explains how to estimate power consumption of the ispGDX2 device based on the device utilization. It assumes that the user is familiar with the ispGDX2 architecture. The information for device utilization is generated by the ispGDX2 Compiler report file.

Power consumption in the ispGDX2 family is the sum of three components:

$I_{CC\text{-}TOTAL} = I_{CORE} + I_{PLL} + I_{HSI}$ ($I_{CC\text{-}TOTAL}$ combines current supplied via V_{CC} pins and V_{CCP} pins)

$I_{CORE} = I_{DC} + I_{REF} + I_{IN}$

= Blank chip background current including power regulator current
+ K_{REF} * Number of banks with V_{REF} active
+ (K_{IN} * Number of inputs + K_{CORE}) * Average Input Switching Frequency (MHz)

$I_{PLL} = I_{PLLD} + I_{PLLA}$

$= K_{PLLD} * F_{VCO} * \text{Number of PLLs used} + K_{PLLA} * F_{VCO} * \text{Number of PLLs used}$

$= (K_{PLLD} + K_{PLLA}) * F_{VCO}) * \text{Number of PLLs used}$

$I_{HSI} = I_{RX} + I_{TX}$

$= [(K_{RXD} + K_{RXA}) * F_{RX} + I_{RXSTBY}] * \text{Number of receiver channels}$
$+ [(K_{TXD} + K_{TXA}) * F_{TX} + I_{TXSTBY}] * \text{Number of transmitter channels}$

Where:

F_{VCO}: sysCLOCK™ PLL VCO Frequency in MHz
F_{RX}: sysHSI™ Receiver Serial Data Rate
F_{TX}: sysHSI Transmitter Serial Data Rate
K_{REF}: Reference voltage circuit current per bank
K_{IN}: I/O current per input per MHz
K_{CORE}: Core current per MHz with GRP fanout of 1
K_{PLLD}: PLL logic current per MHz per PLL
K_{PLLA}: PLL analog portion current per MHz per PLL
K_{RXD}: Receiver logic current per Mbps
K_{RXSTBY}: Receiver logic standby current
K_{RXA}: Receiver analog portion current per Mbps
K_{TXD}: Transmitter logic current per Mbps
K_{TXSTBY}: Transmitter logic standby current
K_{TXA}: Transmitter analog portion current per Mbps

I_{CC} Calculation Example

Assume the following operational conditions:

- Room temperature
- V_{CC} = 1.8V
- 64 inputs are used at average switching frequency of 20 MHz
- One sysHSI Block (two transmitters and two receivers) is configured at 622 Mbps
- One sysCLOCK PLL is used
- sysCLOCK PLL Input Freq(Fin) = 100 MHz and N(Multiplier) / M(divider) = 4:
- F_{VCO} = 400 MHz
- One GRP fanout per input
- All eight banks use V_{REF}

$$
\begin{aligned}
I_{CC\text{-}TOTAL} &= I_{CORE} + I_{PLL} + I_{HSI} \\
&= I_{DC} + I_{REF} + I_{IN} + I_{PLLD} + I_{PLLA} + I_{RX} + I_{TX} \\
&= I_{DC} + K_{REF} * \text{Number of banks with } V_{REF} \text{ active} \\
&\quad + (K_{IN} * \text{Number of inputs} + K_{CORE}) * \text{Average input switching frequency (MHz)} \\
&\quad + [(K_{PLLD} + K_{PLLA}) * F_{VCO}] * \text{Number of PLLs used} \\
&\quad + [(K_{RXD} + K_{RXA}) * F_{RX} + I_{RXSTBY}] * \text{Number of receiver channels} \\
&\quad + [(K_{TXD} + K_{TXA}) * F_{TX} + I_{TXSTBY}] * \text{Number of transmitter channels} \\
&= 4.0 + 1.334 * 8 \\
&\quad + (0.0213 * 64 + 0.239) * 20 \\
&\quad + (0.179 + 0.024) * 400 * 1 \\
&\quad + (0.019 + 0.004) * 622 + 3.7) * 2 + (0.011 + 0.0023) * 622 + 1.2) * 2 \\
&= 183 \text{ mA}
\end{aligned}
$$

The I_{CCP} is supplied through the V_{CCP0} and V_{CCP1} pins for the PLL and sysHSI analog portions. The equation of I_{CCP} can be derived from the equations above.

$$
\begin{aligned}
I_{CCP} &= I_{PLL\_A} + I_{HSI\_A} \\
&= (K_{PLLA} * F_{VCO}) * \text{Number of PLLs used} \\
&\quad + (K_{RXA} * F_{RX}) * \text{Number of receiver channels} \\
&\quad + (K_{TXA} * F_{TX}) * \text{Number of transmitter channels}
\end{aligned}
$$

To calculate the analog portion current consumption of the sysHSI Block, the equation of I_{HSI} can be reorganized as follows.

$$
\begin{aligned}
I_{HSI} &= I_{HSI\_D} + I_{HSI\_A} \\
&= (K_{RXD} * F_{RX} + I_{RXSTBY}) * \text{Number of receiver channels} \\
&\quad + (K_{TXD} * F_{TX} + I_{TXSTBY}) * \text{Number of transmitter channels} \\
&\quad + (K_{RXA} * F_{RX}) * \text{Number of receiver channels} \\
&\quad + (K_{TXA} * F_{TX}) * \text{Number of transmitter channels}
\end{aligned}
$$

I_{CC} estimates are based on typical conditions (V_{CC} = 1.8V, room temperature). These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

Technical Support Assistance

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