Power Estimation in ispXPLD 5000MX Devices

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Introduction

The ispXPLD™ 5000MX family is a unique architecture built around the Multi-Function Block (MFB). This block allows users to implement CPLD logic, dual-port memory (DPRAM), single port-memory (SRAM), pseudo dual-port memory (PDPRAM), contents addressable memory (CAM), and FIFO memory.

This technical note explains how to estimate current consumption for the ispXPLD 5000MX devices based on device utilization and operating frequency. These power estimates should be confirmed with devices operating in the actual system. It is assumed that the reader has knowledge of the ispXPLD5000MX architecture. Please refer to the ispXPLD 5000MX family data sheet for more details. The device utilization information in this technical note can be obtained from the ispLEVER™ design tool.

Power Supply Current Calculations

The ispXPLD 5000MX devices have multiple power pins: V_{CCJ}, V_{CCO}, V_{CC}, and V_{CCP}. This section provides the detail to calculate current requirements for each of the power supplies.

V_{CCJ} Supply

The JTAG power supply pin (V_{CCJ}) current has two components: background current and I/O related current.

- Background current consumption for the V_{CCJ} pin is minimal.
  - At 2.5V, less than 0.5mA
  - At 3.6V less than 1.3mA
- I/O related current is dependent on loads connected to the JTAG pins. The JTAG pins are tri-stated and only have background current consumption when the JTAG port is inactive.

V_{CCO} Supply

The power supply pins for I/O banks (V_{CCO0}, V_{CCO1}, V_{CCO2}, V_{CCO3}) are used to drive the four bank output pins. The typical unloaded (DC) V_{CCO} current (per I/O bank) is 3mA. The AC current component is dependent on capacitance, output voltage swing, number of outputs, and average output frequency. Each bank supply has associated current, therefore use the equation for each of the four banks.

V_{OH} and V_{OL} can be found in the sysIO™ sections of the ispXPLD 5000MX Family data sheet.

Parameters:

- I_{VCCO} = Total current of V_{CCO} per I/O bank
- F_n = Output frequency of output (MHz)
- C_n = Capacitive loading of output (when the output pin is connected to a CMOS input, typical load is 5-10pf)
- V_{OH} = Output voltage high of the output (V)
- V_{OL} = Output voltage low of the output (V)
- V_{CC} = Operating voltage of the device (V)
- n = Number of outputs in the bank
- I_{VCCO_DC} = Typical unloaded V_{CCO} current per I/O bank = 3mA

$$I_{VCCO} = [\Sigma_{n=1} C_n * (V_{OH} - V_{OL}) * F_n] + I_{VCCO\_DC}$$

V_{CC} Supply

The power supply pin for core logic (V_{CC}) is divided into six components for current consumption calculations:

$I_{CC} = I_{CC\_DC} + I_{MFB\_CPLD} + I_{MFB\_ SRAM/PDPRAM/FIFO} + I_{MFB\_DPRAM} + I_{MFB\_CAM} + I_{PLL\_D}$

Where:

- I_{CC} = Current consumption of V_{CC} power supply (mA)
- I_{CC_DC} = I_{CC} DC component - Current consumption at 0MHz (mA)
- I_{MFB_CPLD} = CPLD (non-memory logic) current consumption (mA)
- $I_{MFB\_SRAM/PDPRAM/FIFO}$ = Current consumption for SRAM, PDPRAM, and FIFO (mA)
- I_{MFB_DPRAM} = Current consumption for DPRAM (mA)
- I_{MFB_CAM} = Current consumption for CAM (mA)
- I_{PLL_D} = PLL current consumption of digital V_{CC} power supply (mA)

Current Estimation Equations for V_{CC} Supply

The ispXPLD 5000MX data sheet Power Estimation Coefficient tables specify the coefficient values for each of the devices in the family. The coefficients are defined as:

- K0 = Current per MFB input (μA/MHz)
- K1 = Current per Product Term (μA/MHz)
- K2 = Current per Global Routing Pool (GRP) line driven from MFB (μA/MHz)
- K3 = Current per GRP line driven from I/O (μA/MHz)
- K4 = Global clock tree current (μA/MHz)
- K5 = PLL digital (mA/MHz)
- K6 = PLL analog (mA/MHz)
- K7 = PLL analog baseline (mA)
- DC = Baseline current at 0MHz (mA)
- K8 = CAM frequency component (mA/MHz)
- K9 = CAM DC component (mA)
- K10 = Current per row decoder (μA/MHz)
- K11 = Current per column driver (μA/MHz)

I_{CC_DC} (mA)
Use the appropriate value for ispXPLD 5000MC (1.8V power supply) or ispXPLD 5000MV/B (2.5V/3.3V power supply) from the data sheet.

I_{MFB_CPLD} (mA)
= (((**K0** * CPLD MFB inputs + **K1** * CPLD Logical Product Terms +
K2 * CPLD GRP from MFB + **K3** * CPLD GRP from IFB) * AF+ **K4**) / 1000μA/mA) * FREQ

$I_{MFB\text{-}CAM}$ (mA)
= CAM Memory MFBs * ((FREQ * **K8**) + **K9**) (CAM operating in typical mode)

$I_{MFB\_ SRAM/PDPRAM/FIFO}$ (mA)
= ((WR_ PERCENT * (**K1** + WR_ PERCENT * 8 * **K0** + **K10** + **K11**) +
RD_ PERCENT * (**K1** + 128 * RD_PERCENT * **K0** + 8 * OSW_PERCENT * **K2**))
* SRAM/PDPRAM/FIFO Memory MFBs / 1000μA/mA) * FREQ

I_{MFB_DPRAM} (mA)
= (WR_ PERCENT * (2 * **K1** + 2 * WR_ PERCENT * 8 * **K0** + **K10** + **K11**) +
RD_ PERCENT * (2 * **K1** + 2 * 128 * RD_PERCENT * **K0** + 8 * OSW_PERCENT * **K2**))
* DPRAM Memory MFBs / 1000μA/mA) * FREQ

I_{PLL_D} (mA)
= **K5** * PLL_FREQ * number of PLLs used
I_{PPL_D} is the PLL digital component of the V_{CC} supply current.

Current Estimation Equations for V_{CCP} Supply

The power supply for PLLs (V_{CCP} pin) has current consumption if the PLL is used. If the PLL is not used, the current consumption on the V_{CCP} pin is minimal.

- I_{PLL_A} = PLL analog power pin current consumption (V_{CCP} pin)

I_{PLL_A} (mA)
= (**K6** * PLL_FREQ + **K7**) * number of PLLs used

Equation Parameters

Design-Based Parameters

Design-based parameters need to be determined or estimated when using the current calculation equations:

- FREQ = Average frequency of device operation (MHz).
- AF = PLD activity factor as a percentage (12.5% for a 16-bit counter). As a rule of thumb, use 25% if this can't be estimated (%).
- PLL_FREQ = Average PLL input frequency (MHz).
- WR_ PERCENT = Writes as a percentage of memory accesses. As a rule of thumb, use 50% if this can't be estimated (%).
- RD_PERCENT = Reads as a percentage of memory accesses. As a rule of thumb, use 50% if this can't be estimated (%).
- OSW_PERCENT = RAM output switching activity factor (how often the outputs change on the RAM). As a rule of thumb, use 50% if this can't be estimated (%).

CPLD Parameters

Device statistics are taken from the ispLEVER design tool report file. If memory is used, the resources associated with the memory need to be removed to get an accurate CPLD I_{CC} estimate. The Cluster_Table section of the report file will show which MFBs are used for memory. If a memory needs to use any portion of a MFB, the entire MFB is used and unused MFB resources are not available for CPLD logic. This equation will help determine unknown CPLD parameters:

TOTAL report file parameter = CPLD related parameter + Memory related parameter

- **CPLD MFB Inputs:**
  Total MFB Inputs are reported in Device_Resource_Summary. Use this if no memory is used in the design. In the MFB_Resource_Summary section, the "Fanin" column is equivalent to MFB Inputs. Determine the CPLD MFB inputs by using the MFB_Resource_Summary, not counting the memory MFB related "Fanin".
- **CPLD Logical Product Terms:**
  Total Logical Product Terms are reported in Device_Resource_Summary. Use this if no memory is used in the design. In the MFB_Resource_Summary section, the "Logic PTs" column is equivalent to Logical Product Terms. Determine the CPLD Logical Product Terms by using the MFB_Resource_Summary, not counting the memory MFB related "Logic PTs".

- **CPLD GRP from MFB: (MFB Feedback to the Global Routing Pool)**
  Total GRP from MFB is reported in the Device_Resource_Summary. Use this if no memory is used in the design. Determine the number of CPLD GRPs from MFB by estimating the number of memory inputs from CPLD logic and subtracting this from the total GRPs from MFB.
- **CPLD GRP from IFB: (I/O Feedback to the Global Routing Pool)**
  Total GRP from IFB is reported in the Device_Resource_Summary. Use this if no memory is used in the design. Determine the number of CPLD GRPs from IFB by estimating the number of input pins used for CPLD logic. Alternatively, estimate the number of pins used for memory, and subtract this number from Total GRPs from IFB.

Note: the Logic_Array_Fanin section gives source information per MFB (pin or macrocell). It can be used to estimate CPLD GRP from MFB (macrocell) and CPLD GRP from IFB (pin), but duplicated signals should be counted only once and will complicate using this information.

Memory Parameters

Memory usage is reported per macrocell in the report file. In the ispXPLD family, there are 32 macrocells per MFB.

- **SRAM/PDPRAM/FIFO Memory MFBs:**
  Memory MFBs used by SRAM/PDPRAM/FIFO (at 16k bits per MFB). For example, if a 16k x 2 SRAM is used, with 64 memory macrocells reported, two Memory MFBs are used.
- **DPRAM Memory MFBs:**
  Memory MFBs used by DPRAM (at 8k bits per MFB). For example if a 4k x 4 DPRAM is implemented, two Memory MFBs will be used (16k / 8k = 2).
- **CAM Memory MFBs:**
  Memory MFBs used by CAM (at 16k bits per MFB).
- **Number of PLLs used:**
  This is reported in the PLL section of the report file if PLLs are used.

Sample I_{CC} vs. Frequency Curves

Figure 1 and Figure 2 show trends of V_{CC} pin current versus frequency for two ispXPLD 5512MX designs.

Figure 1. I_{CC} vs. Frequency of ispXPLD 5512MX Filled with 16-Bit Counters (12.5% Activation Factor)

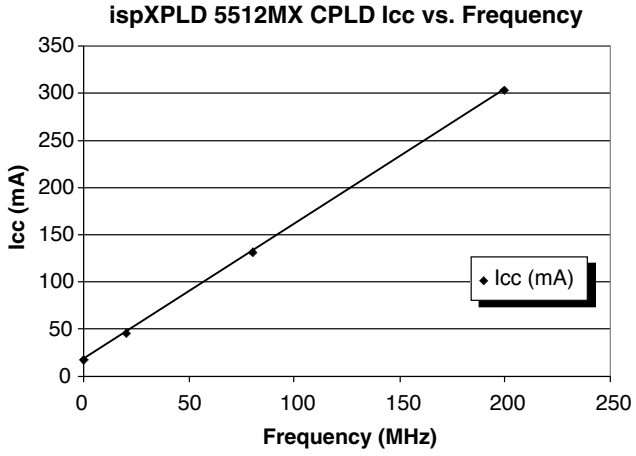
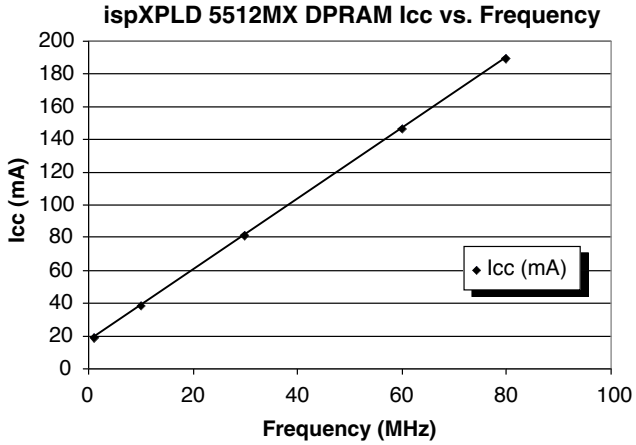


Figure 2. I_{CC} vs. Frequency of ispXPLD 5512MX Filled with 14 GLB 1x8 DPRAM at 12.5% Output Switching Levels



Note: The power calculations as described in this technical note are only estimates. These estimates should be confirmed with devices operating in the actual system.

V_{CC} Supply Current Calculation Example

As an example calculation, a sample design was fit into an ispXPLD 5512MC device. The design contains one 8k x 2-bit DPRAM, and four 16-bit counters all running at 80MHz. Below is an abbreviated ispLEVER report file from the design.

```
Device_Resource_Summary

                              Total
                            Available  Used  Available  Utilization
-------------------------------------------------------------------
Dedicated Pins
  Clock Pins                    2        2      0     -->   100
  Clock/Clock Enable Pins       2        2      0     -->   100
  Enable Pins                   2        0      2     -->     0
  Reset Pins                    1        0      1     -->     0
I/O Pins                      253      102    151     -->    40
Logic Macrocells              765      274    491     -->    35
  Input Registers             253        0    253     -->     0
  Unusable Macrocells          ..        0     ..     -->    ..

MFB Inputs                   1088      216    872     -->    19
Logical Product Terms        2560      611   1949     -->    23
Occupied MFBs                  16       13      3     -->    81
Occupied Macrocells           512      222    290     -->    43
  Two Function Macrocells      ..        1     ..     -->    ..
  One Function Macrocells      ..      107     ..     -->    ..
  Zero Function Macrocells     ..        2     ..     -->    ..
  Memory Macrocells            ..       64     ..     -->    ..
  Arithmetic Macrocells        ..       48     ..     -->    ..
Occupied Product Terms        2624      747   1877     -->    28

Control Product Terms:
  Segment Product Term Enable   16        0     16     -->     0
  MFB Clocks                    16        0     16     -->     0
```

```
  MFB Resets                        16        9      7    -->    56
  Macrocell Clocks                 512        0    512    -->     0
  Macrocell Clock Enables          512        0    512    -->     0
  Macrocell Enables                512        0    512    -->     0
  Macrocell Resets                 512       15    497    -->     2
  Macrocell Presets                512        3    509    -->     0

Global Routing Pool                765      147    618    -->    19
  GRP from IFB                      ..       34     ..    -->    ..
    (from input signals)            ..       34     ..    -->    ..
    (from output signals)           ..        0     ..    -->    ..
    (from bidir signals)            ..        0     ..    -->    ..
  GRP from MFB                      ..      113     ..    -->    ..
-------------------------------------------------------------------

<Note> 1 : IFB is I/O feedback.
<Note> 2 : MFB is macrocell feedback.

...

MFB_E_CLUSTER_TABLE

    MMMM MMMM MMMM MMMM MMMM MMMM MMMM MMMM GGGGSBBB      I    P  P
    EEEE EEEE EEEE EEEE EEEE EEEE EEEE EEEE CCORECCA      /    B  T
    MMMM MMMM MMMM MMMM MMMM MMMM MMMM MMMM KEEEBKER Type O    Y  E      Signal
-------------------------------------------------------------------------------
M00 U0\RamBaseBlockInst0{RAMB8K_X2_X2}      --------
M01 U0\RamBaseBlockInst0{RAMB8K_X2_X2}      --------
M02 U0\RamBaseBlockInst0{RAMB8K_X2_X2}      --------
...


MFB_F_CLUSTER_TABLE

    MMMM MMMM MMMM MMMM MMMM MMMM MMMM MMMM GGGGSBBB      I    P  P
    EEEE EEEE EEEE EEEE EEEE EEEE EEEE EEEE CCORECCA      /    B  T
    MMMM MMMM MMMM MMMM MMMM MMMM MMMM MMMM KEEEBKER Type O    Y  E      Signal
-------------------------------------------------------------------------------
M00 U0\RamBaseBlockInst1{RAMB8K_X2_X2}      --------
M01 U0\RamBaseBlockInst1{RAMB8K_X2_X2}      --------
M02 U0\RamBaseBlockInst1{RAMB8K_X2_X2}      --------
...
```

MFB_Resource_Summary

		Fanin	I/O Pins	Input Regs	Macrocells Used	Macrocells Unusable	Macrocells available	Logic PTs	# of PT clusters used
Maximum									
MFB		68	*(1)	16	--	--	32	160	32
MFB	A	13	10/16	0	22	0	10	46	22
MFB	B	14	6/16	0	16	0	16	28	16
MFB	C	0	0/11	0	0	0	32	0	0
MFB	D	0	0/14	0	0	0	32	0	0
MFB	E	35	0/14	0	32	0	0	160	32
MFB	F	35	0/14	0	32	0	0	160	32
MFB	G	32	8/16	0	24	0	8	39	24
MFB	H	22	8/16	0	17	0	15	23	17
MFB	I	1	10/16	0	1	0	31	1	1
MFB	J	0	0/16	0	0	0	32	0	0
MFB	K	19	16/18	0	29	0	3	53	29
MFB	L	9	16/18	0	9	0	23	22	9
MFB	M	8	11/18	0	4	0	28	6	4
MFB	N	9	3/18	0	6	0	26	7	6
MFB	O	13	10/16	0	22	0	10	46	22
MFB	P	6	4/16	0	8	0	24	20	8

<Note> 1 : For LC5000MX devices, the number of IOs depends on the MFB.
<Note> 2 : Four rightmost columns above reflect last status of the placement process.

To calculate I_{CC} for the V_{CC} supply:

$I_{CC} = I_{CC\text{-}DC} + I_{MFB\_CPLD} + I_{MFB\_SRAM/DPRAM/FIFO} + I_{MFB\_CAM} + I_{PLL\_D}$

$I_{CC\text{-}DC}$
= 17mA

I_{MFB_CPLD}
= (((**K0** * CPLD MFB inputs + **K1** * CPLD Logical Product Terms + **K2** * CPLD GRP from MFB + **K3** * CPLD GRP from I_{FB}) * AF+ **K4**) / 1000μA/mA) * FREQ

Looking at the cluster table, MFB E and MFB F are where the DPRAM is placed. Therefore, remove resources associated with these memory MFBs.

- CPLD MFB inputs: 216 (total MFB inputs) - 70 (MFB E, MFB F Fanin) = 146.
- CPLD Logical Product Terms: 611 (Total Logical Product Terms) - 320 (MFB E, MFB F Logic PTs) = 291.
- CPLD GRP from MFB: 113 (Total GRP from MFB). Memory is connected to external pins. Assume 0 GRP from MFB associated with memory. Use CPLD GRP from MFB = 113.
- CPLD GRP from I_{FB}: 34 (Total GRP from IFB). Memory is connected to pins, 0 input pins used for counters (don't count clock and reset). Use CPLD GRP from I_{FB} = 0.
- AF = 12.5% (for 16-bit counters)
- FREQ = 80MHz

$I_{MFB\text{-}CPLD}$
= (((2.2µA/MHz * 146 + 8.4µA/MHz * 291+ 9.4µA/MHz * 113 + 27.6µA/MHz * 0) * .125 + 151µA/MHz) 1000µA/mA) * 80MHz/
= 50mA

I_{MFB_CAM}
= 0 (CAM Memory MFBs = 0)

$I_{MFB\_SRAM/PDPRAM/FIFO}$
= 0 (Memory MFBs = 0)

I_{MFB_DPRAM}
= ((WR_ PERCENT * (2 * **K1** + 2 * WR_ PERCENT * 8 * **K0** + **K10** + **K11**) + RD_ PERCENT * (2 * **K1** + 2 * 128 * RD_PERCENT * **K0** + 8 * OSW_PERCENT * **K2**)) * DPRAM Memory MFBs / 1000µA/mA) * FREQ

Where:

- WR_PERCENT = 50%
- RD_ PERCENT = 50%
- OSW_PERCENT = 50%
- DPRAM Memory MFBs = 2
- FREQ = 80MHz

I_{MFB_DPRAM}
= (.5 * (2 * 8.4µA/MHz + 2 * .5 * 8 * 2.2µA/MHz + 4.4µA/MHz + 2.9µA/MHz) + .5 * (2 * 8.4µA/MHz + 2 * 128 * .5 * 2.2µA/MHz + 8 * .5 * 9.4µA/MHz)) * 2 / 1000µA/mA) * 80MHz
= 30mA

I_{PLL_D}
= 0 (number of PLLs used = 0)

$I_{CC} = I_{CC\text{-}DC} + I_{MFB\_CPLD} + I_{MFB\_SRAM/DPRAM/FIFO} + I_{MFB\_CAM} + I_{PLL\_D}$
I_{CC} = 17mA + 50mA + 0 + 30mA + 0 + 0
= 97mA

Technical Support Assistance

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