Power Estimation in ispMACH 5000VG Devices

Introduction

Several elements must be considered when determining the power requirements for a given design in a programmable logic device. These issues include frequency of operation, device utilization and external I/O loading. This application note describes a formula for estimating P_{TOTAL} or the total power dissipated by a given design for an ispMACH™ 5000VG device. Refer to the Thermal Management document on the Lattice Semiconductor web site (www.latticesemi.com) or CD-ROM for additional information necessary to conduct a thermal analysis. This document provides an estimation for power. The designer should check actual power consumption after implementation to ensure there will be no thermal issues.

ispMACH 5000VG devices are designed to optimize speed and power for high-performance, low-power designs. The Lattice ispIMPACT™ software tool allows a designer to control power consumption on a signal by signal basis by assigning low power attributes to a given signal. This allows for complete flexibility in routing and placing signals within a device. An additional power management feature defaults unused product terms to a powered-off state

Estimating Total Power (P_{TOTAL})

The formula below is for estimating total power consumption or P_{TOTAL} for an ispMACH 5000VG device design:

$$P_{TOTAL} = P_{DC\text{-}LOAD} + P_{AC\text{-}LOAD} + P_{DEVICE} \tag{Eq.1}$$

$P_{DC\text{-}LOAD}$ is the component due to the resistive I/O loads. $P_{AC\text{-}LOAD}$ is the I/O power component that scales with the average frequency of the design and P_{DEVICE} is the DC and AC power component of the device itself determined with all I/Os disabled.

Estimating $P_{DC\text{-}LOAD}$

The DC load power is a function of the number of steady-state I/O pins that are resistively loaded. The power necessary to maintain a DC level when driving a purely capacitive CMOS load is negligible.

The equation for calculating $P_{DC\text{-}LOAD}$ is:

$$P_{DC\text{-}LOAD} = (P_{PULL\text{-}UP} \cdot \#Pull\text{-}up) + (P_{PULL\text{-}DOWN} \cdot \#Pull\text{-}down) \tag{Eq. 2}$$

- $P_{PULL\text{-}UP}$ = see Table 1 for appropriate factor
- #Pull-up = the number of I/Os resistively pulled up
- $P_{PULL\text{-}DOWN}$ = see Table 1 for appropriate factor
- #Pull-down = the number of I/Os resistively pulled down

Table 1. DC Load Power Factors

Load	V_{CC}	1K	2K	5K
Pull-up	3.3V	TBD	TBD	TBD
Pull-down	3.3V	TBD	TBD	TBD

Estimating $P_{AC\text{-}LOAD}$

The AC power component is dependent on operating voltage, capacitance, output voltage swing, number of output, and average output frequency. The variable n in Equation 3 is the number of outputs in the design. V_{OH} and V_{OL} can be found in the ispMACH 5000VG Family data sheet in the corresponding device section.

$$P_{AC\text{-}LOAD} = V_{CC} \cdot \left[\sum_{n=1} C_n \cdot (V_{OH} - V_{OL}) \cdot F_n \right] \qquad \text{(Eq. 3)}$$

- $P_{AC\text{-}LOAD}$ = Power from AC Component
- F_n = Output frequency of output
- C_n = Capacitive loading of output
- V_{OH} = Output Voltage High of the output
- V_{OL} = Output Voltage Low of the output
- V_{CC} = Operating Voltage of the device
- n = Number of Outputs

Estimating P_{DEVICE}

Device power is calculated from Equation 4. P_{DEVICE} is dependent on signal power settings, power constants, operating voltage, PLL usage and the average switching frequency of the device as estimated by the designer. The total number of product terms used and their corresponding power mode, either high or low power, can be found in Lattice's design tool report file.

$$P_{DEVICE} = P_{DEVICE\text{-}AC} + P_{DEVICE\text{-}DC} \qquad \text{(Eq. 4)}$$

Each term in P_{DEVICE} is further defined as:

$$P_{DEVICE\text{-}AC} = V_{CC} \cdot [F_{AVE} [(K_0 \cdot PT_{HP}) + (K_1 \cdot PT_{LP}) + (K_2 \cdot GRP_{LINES})] + (K_3 \cdot F_{PLL0}) + (K_3 \cdot F_{PLL1})] \quad \text{(Eq. 5)}$$

$$P_{DEVICE\text{-}DC} = V_{CC} \cdot [(K_4 \cdot PT_{HP}) + (K_5 \cdot PT_{LP}) + (K_6 \cdot \#PLL) + I_{DC}] + V_{CCON} \cdot I_{DCO} \qquad \text{(Eq. 6)}$$

Where:

- PT_{LP} = Number of product terms in low power
- PT_{HP} = Number of product terms in high power
- PLL = Number of Phase Lock Loop circuits utilized
- F_{AVE} = Average Output Frequency of Switching product terms in MHz
- $I_{DC\text{-}PLL}$ = Static PLL power
- I_{DC} = Static device current with all product terms powered off
- $K_0...K_5$ = Device Power Constants listed in the device data sheet
- V_{CC} = Operating Voltage of Device
- V_{CCON} = Operating voltage of I/O bank *N*, where *N* is between 0-3.
- I_{DCO} = Static I/O bank current

The K-constants for each the device are found in the Power Consumption section of the ispMACH 5000VG Family data sheet.

Technical Support Assistance

Hotline: 1-800-LATTICE (Domestic)

   1-408-826-6002 (International)

e-mail: techsupport@latticesemi.com