Optimizing Jitter Performance in ispClock5500 Programmable PLL Clock Generators

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Introduction

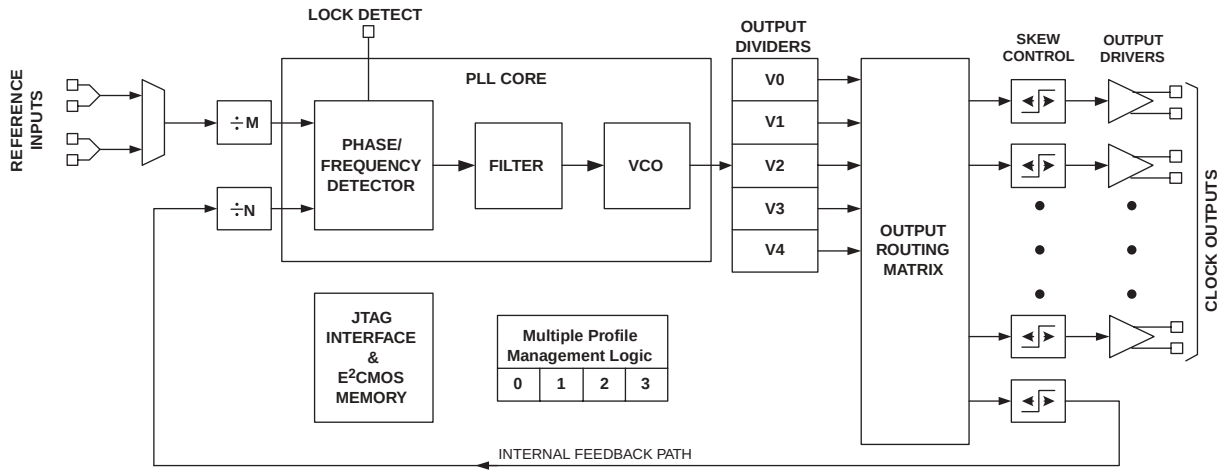
The flexibility provided by the ispClock™5500 programmable Phase-Locked-Loop clock generators allows the device to meet a wide range of system design requirements, and replace numerous fixed-function and application-specific clock generator and buffer chips. The ispClock5500 is able to meet the requirements of a broad range of applications through programmability.

One of the most important performance criteria for system clock generators and buffers is jitter. This application note will discuss some simple strategies the system designer can use to optimize the ispClock5500's jitter performance.

ispClock5500 Description

The ispClock5500 is a programmable clock generator which uses a phase-locked loop (PLL) to perform clock synthesis functions. The PLL allows the device to generate output frequencies which may be equal, less than, or greater than the input reference frequency. A simplified block diagram of the ispClock5500 is shown in Figure 1.

Figure 1. ispClock5500 Organization



Some of the ispClock5500's key programmable features are:

- M, N and V dividers
- PLL loop filter
- Output skew (delay)
- Input logic type and parallel termination
- Output logic type, slew rate and series termination

Of these features, all except output skew can have an effect on the device's output jitter performance.

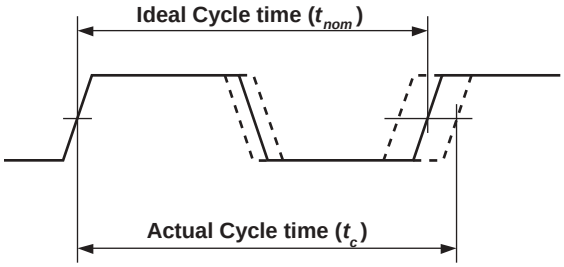
What is Jitter?

In the case of a periodic clock signal, one would ideally like to have the time between consecutive cycles to be identical. For real-world clock sources, however, there is always a small amount of variation in the duration of each cycle. This variation is called jitter.

Because clock signals are used for many different purposes, there are several ways of characterizing jitter. Two of the most common measures are period jitter, and adjacent-cycle (or cycle-cycle) jitter.

Period jitter ($t_{jit(per)}$) is defined by JEDEC standard JESD65-A as the deviation in cycle time of a signal with respect to that of an ideal period over a random sampling of cycles, as shown in Figure 2.

Figure 2. Measurement of Period Jitter

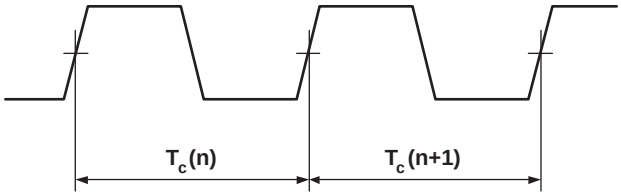


The 'ideal' period t_{nom} is defined as 1/fo, where fo is the frequency of the signal. The period jitter of a given cycle is defined by

$$V_{jit(per)} = t_c - t_{nom}$$

While period jitter measures variation from an ideal clock signal, adjacent cycle jitter $t_{jit(cc)}$ measures the deviation between two successive cycles, as shown in Figure 3.

Figure 3. Measurement of Adjacent-cycle Jitter



As in the case of measuring period jitter, each adjacent cycle pair is sampled at random from the clock signal. The adjacent cycle jitter of a given pair of cycles is defined by

$$V_{jit(per)} = t_{c(n)} - t_{c(n+1)}$$

To make meaningful statements about the level of jitter present in a signal, one must consider the statistics from a large number of samples. For this reason jitter is usually characterized as a peak-peak or RMS (Root-Mean-Square) measurement.

Peak-peak jitter is the difference between the greatest (most positive) value of jitter measured in a set of samples, minus the smallest (most negative) value in the same set. Peak-peak jitter is normally specified over a given number of samples, and will tend to increase as one looks at sets of larger and larger samples. Given a sample of 'n' individual jitter measurements t_{j1} through $t_{jn,}$ one can calculate peak-peak jitter for the sample as

$$V_{jpp} = \max(t_{j1}...t_{jn}) - \min(t_{j1}...t_{jn}) \quad (1)$$

Although a useful means of characterizing a jitter signal, in that it gives one a good intuitive idea of what the 'worst case' jitter will be over a given time horizon, peak-peak jitter measurements have the drawback of being difficult to accurately measure. This is because they are usually specified over a relatively small sample sizes (1,000-10,000), where the statistical nature of the measurement contributes significantly to the measurement error.

An alternate method of characterizing a set of jitter measurements is by its RMS magnitude, relative to its mean. RMS jitter characterization has the advantage of providing a more stable, repeatable measurement, which is

largely independent of the number of samples made. Given a sample of 'n' individual jitter measurements t_{j1} through $t_{jn,}$ one can calculate RMS jitter for the sample as

$$t_{jRMS} = \sqrt{\frac{\sum_{i=1}^{n} (t_{ji} - \bar{t_j})^2}{n}} \quad (2)$$

Where $\bar{t_j}$ is the mean of the jitter measurements. One may recognize this expression as also representing the sigma, or standard deviation of a population. This is significant because when the jitter measurements have a normal (bell-curve) distribution (a common condition for clock signals) knowing the RMS jitter allows one to make estimates of peak-peak jitter for an arbitrary number of samples, as well as other statistic inferences relating to performance.

Effects of Divider Settings

Of all of the ispClock5500's programmable options, divider settings have the most significant effect on output jitter. While the input and output frequency requirements of a design may sharply curtail the number of viable divider configurations, there are often still at least a few options which will satisfy the requirements. In many cases there will be a noticeable difference in jitter performance among the available divider configuration options.

While the interaction among dividers is complex, the following two rules will often provide significant reductions in output jitter:

1. Choose a divider configuration that maximizes VCO frequency
2. Choose as small an 'M' divider as possible

Choosing a divider configuration that maximizes the VCO frequency (rule #1) lowers jitter because the VCO's jitter decreases as its operating frequency increases. Increasing the VCO frequency also requires that the values of the V dividers also be increased to compensate. In addition to reduced jitter, running at maximal VCO frequency also provides more configuration flexibility.

The object of minimizing the M divider setting (rule #2) is that this maximizes the input frequency presented to the phase detector. This also maximizes the frequency of the phase detector's output error signal, which is then more effectively filtered by the PLL's loop filter, reducing the ripple in the VCO's control signal, and effective output jitter.

Effects of Loop Filter Settings

The choice of loop filter settings is determined by the product of the N-divider and the V-divider used in the feedback loop. Recommended filter settings for a given configuration may be found in both the datasheet and the PAC-Designer software. Although it may be possible in some situations to slightly improve jitter by using a non-recommended setting, this is strongly discouraged, as doing so may decrease the loop's overall stability. While this may not be an issue when working with a limited number of devices during development, the potential reduction in stability resulting from using non-recommended filter settings may pose problems in high-volume manufacturing.

I/O Signal Considerations

As in the case of many other systems, the concept of 'Garbage-In, Garbage-Out' also applies to PLL jitter performance. Much of the jitter present at the input reference signal will be passed along to the outputs. The input jitter will be filtered and attenuated, however, by the ispClock5500's loop filter. Because the loop filter can have corner frequencies on the order of several hundred kHz, significant amounts of input jitter can still be passed through. For this reason it is very important to have a low-jitter input reference. One cannot depend on the PLL to remove jitter present on the input reference signal.

One can also add jitter to a signal by slowing down the rise and fall times of input signals. This is not because signals with slower edges intrinsically have more jitter than signals with faster edge rates, but because they are more susceptible to noise. The increase in jitter on slow-edged signals occurs because slower rise and fall times combine with noise present in the system to create a greater uncertainty of when the signal passes through HIGH and LOW thresholds on the inputs. Similarly, the use of slow edge rates on outputs will also increase the effective total jitter of the output signals. For this reason it is important to use the fastest edge rates that are compatible with functional and EMC (Electro-Magnetic Compatibility) performance requirements.

Example

As an example, consider an ispClock5500 configured to accept an 80 MHz input signal and provide an output at the same frequency. Table 1 presents an 'optimal' configuration (lowest achievable jitter), and shows the effects of variations from this optimum point resulting from violations of the guidelines described above.

Table 1. Effects of Violating Jitter Reduction Guidelines

M	N	V	Output Slew Rate	Period Jitter (ps RMS)	Jitter 'Penalty' (ps)	Comments
1	1	8	Fastest	13.7	—	'Optimal' configuration
4	4	8	" "	18.3	4.6	M-divider not minimized
1	1	6	" "	18.7	5.0	FVCO not maximized
1	1	8	Slowest	14.8	1.1	Output slew rate not maximized

As one can see from the examples above, the VCO frequency and the M-divider value have by far the greatest effect on overall jitter performance, with output slew rate having a relatively small effect. One can expect to see qualitatively similar results for other device configurations.

Summary

This application note has described the architecture of the ispClock5500 and briefly discussed what jitter is and how it is measured. Some simple strategies for reducing jitter when designing with the ispClock5500 were then described. Finally, an example was presented showing the effects of each of the recommendations.

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