ORCA Series Boundary Scan

August 2004 Application Note AN8073

Introduction

The increasing complexity of integrated circuits and packages has increased the difficulty of testing printed-circuit boards. As integrated circuits become more complex, testing of the loaded board is one of the most difficult tasks in the design cycle. Advanced package technology has led to the need to develop new ways to test the printed-circuit boards instead of conventional probing techniques.

To cope with these testing issues, the IEEE Std. 1149.1-1990 (IEEE Standard Test Access Port and Boundary-Scan Architecture) was developed to provide a solution to the problem of testing the printed circuit board. IEEE Std. 1149.1-1990 defines a test access port and boundary-scan architecture so that circuitry can test interconnections between integrated circuits on the printed-circuit board, test the integrated circuit itself, and analyze functionality of the device on the printed-circuit board.

To address these issues, the IEEE Std. 1149.1-1990 compatible boundary-scan architecture and test access port are implemented in the ORCA® series. The boundary-scan logic, including a boundary-scan test access port (BSTAP) and other associated circuitry, is placed at the upper left corner of the device, while boundary-scan shift registers are located near each I/O pad.

The boundary-scan test access port controller conforms to the standard for the three mandatory instructions (bypass, extest, and sample/preload). This conformance was tested with vectors generated by the internal Lattice Semiconductor program Tapdance (boundary-scan conformance vector generator). In addition to the three mandatory instructions, four user-defined instructions are provided to support additional testability of the ORCA series.

Overview of Boundary-Scan Architecture

Figure 1 shows a block diagram of the boundary-scan architecture that is implemented in the ORCA series. There are three input pins (TDI, TMS, and TCK) and one output pin (TDO). The built-in power on reset circuitry resets the boundary-scan logic during powerup. This is essential to prevent all I/O buffers from contention during power-on. In addition, an external pin ($\overline{\text{PRGM}}$) can be used to reset boundary-scan logic at any time when it is necessary, but this pin is not a standard reset pin as defined in IEEE Std. 1149.1-1990. The three input pins to the boundary-scan logic are user-accessible PIC I/O pins whose location varies from part to part, and the output pin is the dedicated TDO/RD_DATA output pin. The functionality of these pins is as follows:

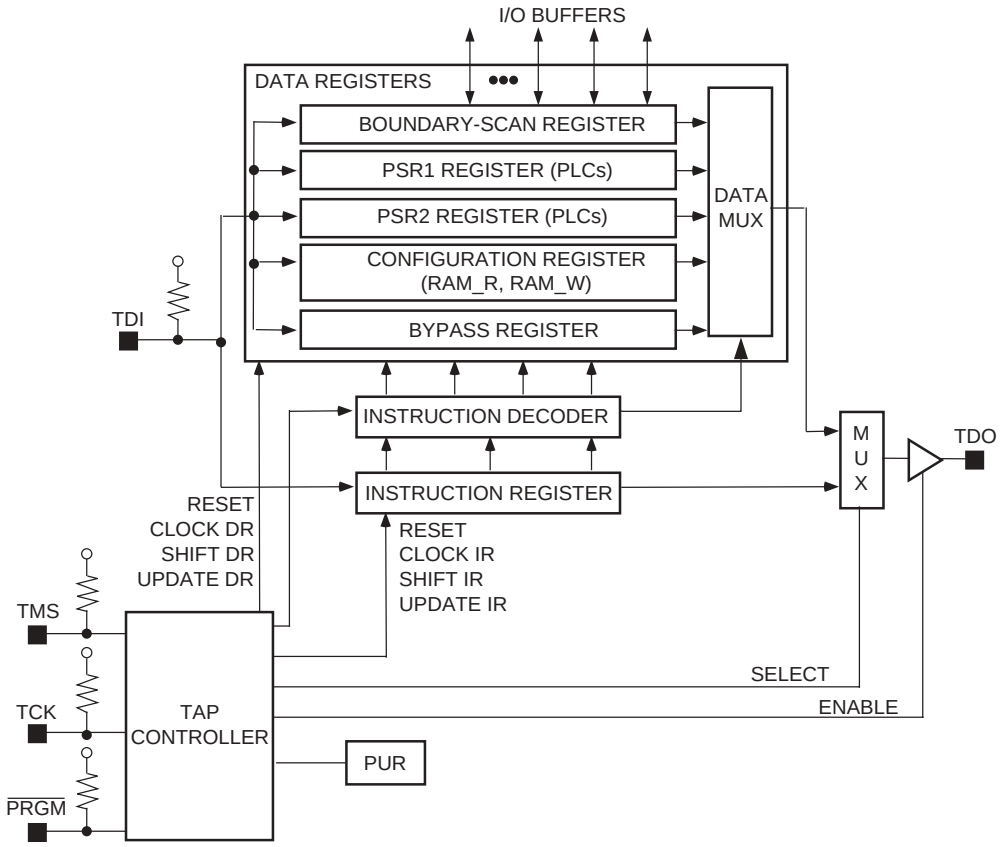
- Test data input (TDI): Serial input data.
- Test mode select (TMS): Controls the BSTAP controller.
- Test clock (TCK): Test clock.
- Test data output (TDO): Serial data output.

There are five data registers and one instruction register in the boundary-scan architecture, as shown in Figure 1.

- The primary data register is a boundary-scan register, comprising a shift register around the peripheral of the chip. This shift register is used for controlling the functionality of the I/O pins of the device. CCLK, DONE, and the four boundary-scan interface pins (TCK, TDI, TMS, and TDO) are not included in the boundary-scan chain.
- The bypass register, a single flip-flop, allows the serial input data from TDI to be shifted out of the TDO output without interfering with the FPGAs normal functionality.
- A pair of user-defined internal scan data registers can be optionally configured by using the registers in the PLCs. This allows user scan data to be shifted out of the TDO output.

- The existing configuration data shift register can be controlled by the BSTAP controller to either write the configuration memory or read back its contents.
- A 3-bit instruction register is implemented for the three mandatory instructions and the four user defined instructions.

Figure 1. Boundary-Scan Functions



The boundary-scan logic is always enabled before configuration so that the user can activate the boundary-scan instructions. After configuration, a configuration RAM bit is used to determine whether the boundary-scan logic is to be used or not. If boundary-scan is not used, the I/O pins TCK, TDI, and TMS can be used as normal user-defined I/O pins, and the TDO/RD_DATA output pin can be used to output configuration RAM read back data.

Boundary-Scan Circuitry

The boundary-scan circuitry includes a test access port controller, a 3-bit instruction register, a boundary-scan register, and a bypass register. It also includes other circuitry to support the four user-defined instructions.

The BSTAP controller in the ORCA series is an IEEE Std. 1149.1-1990 compatible test access port controller. The 16 state assignments, from the IEEE Std. 1149.1-1990 specification, are implemented in the BSTAP, which is controlled by TCK and TMS. All control signals are issued on the rising edge of TCK, except the ENABLE signal, which switches on the falling edge of the TCK.

The BSTAP controller state diagram is shown in Figure 2, and each state is described below.

Test-Logic-Reset

The boundary-scan logic is in reset mode, which allows the device to be in normal operation in this state. This state is entered during power-on and can be reached two different ways: holding the TMS at a logic 1 and applying five TCK clock cycles, or holding $\overline{\text{PRGM}}$ pin low.

Run-Test/Idle

The operation of the boundary-scan logic depends on the instruction held in the instruction register.

Select-DR/IR

Either the data register or the instruction register is selected. Thus, TDI is the input and TDO the output of the selected path.

Capture-DR/IR

Data or instructions (whichever is selected) are loaded from the parallel inputs of the selected data or instructions registers into their shift register paths.

Shift-DR/IR

The captured data or instructions (whichever is selected) are shifted out while new data or instruction is shifted in the selected registers.

Update-DR/IR

This state marks the completion of the shifting process, and either the instruction register is loaded for instruction decode or the boundary-scan register is updated for I/O pin control.

Other States

Pause and exit states are provided to allow the shifting process to be temporarily halted for any test reason.

For ORCA Series 3 devices, the 3-bit instruction register and the instruction decoder are provided for the three mandatory instructions and the four user-defined instructions, as shown in Table 1. The instruction register provides one of the serial paths between TDI and TDO, as shown in Figure 1.

For ORCA Series 4 devices, the 6-bit instruction register and the instruction decoder are provided for the three mandatory instructions and multiple user-defined instructions, as shown in Table 2. The instruction register provides one of the serial paths between TDI and TDO, as shown in Figure 1.

The instruction register is a two-stage register in which the instruction data is shifted serially into the first stage and then updated in parallel into the second stage.

After the assertion of Update-IR, a new instruction can be shifted into the first stage of the instruction register without altering the previous instruction.

The output of the second stage makes up a 3-bit parallel instruction word that is sent to the instruction decoder. The instruction decoder will decode the signals (mode, capture, shiftn, update, etc.) to control the boundary-scan shift register and other test data registers.

The bypass register is a single-bit shift register so that the serial scan data (TDI) can be shifted out to TDO with a delay of one TCK clock period.

Table 1. Boundary-Scan Instructions, ORCA Series 3 Devices

Code	Instruction
000	Extest
001	PLC Scan Ring 1
010	RAM Write (RAM_W)
011	Reserved
100	Sample
101	PLC Scan Ring 2
110	RAM Read (RAM_R)
111	Bypass

Table 2. Boundary-Scan Instructions, ORCA Series 4 Devices

Code	Instruction
000000	EXTEST
000001	SAMPLE
000011	PRELOAD
000100	RUNBIST
000101	IDCODE
000110	USERCODE
001000	ISC_ENABLE
001001	ISC_PROGRAM
001010	ISC_NOOP
001011	ISC_DISABLE
001101	ISC_PROGRAM_USERCODE
001110	ISC_READ
010001	PLC_SCAN_RING1
010010	PLC_SCAN_RING2
010011	PLC_SCAN_RING3
010100	RAM_WRITE
010101	RAM_READ
111111	BYPASS

Figure 2. TAP Controller State Diagram

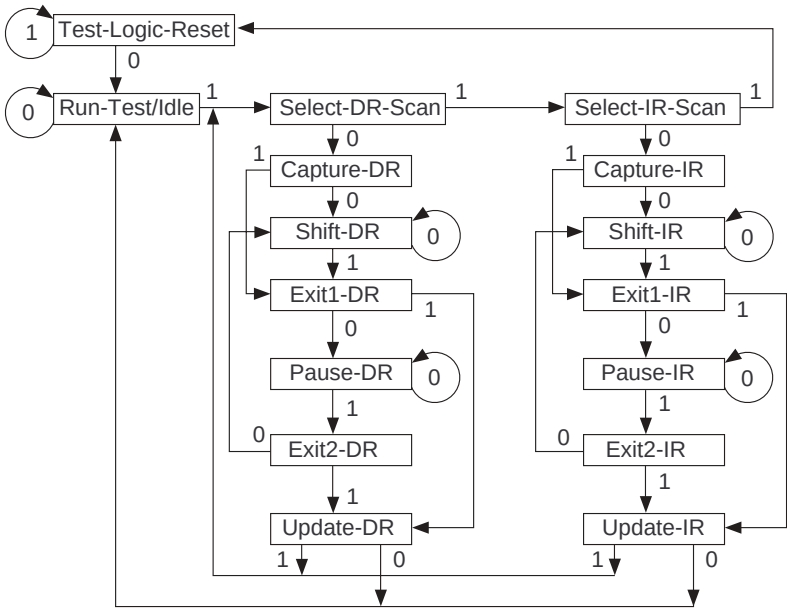


Figure 3. Boundary-Scan Cell (BSC), ORCA Series 3 Devices

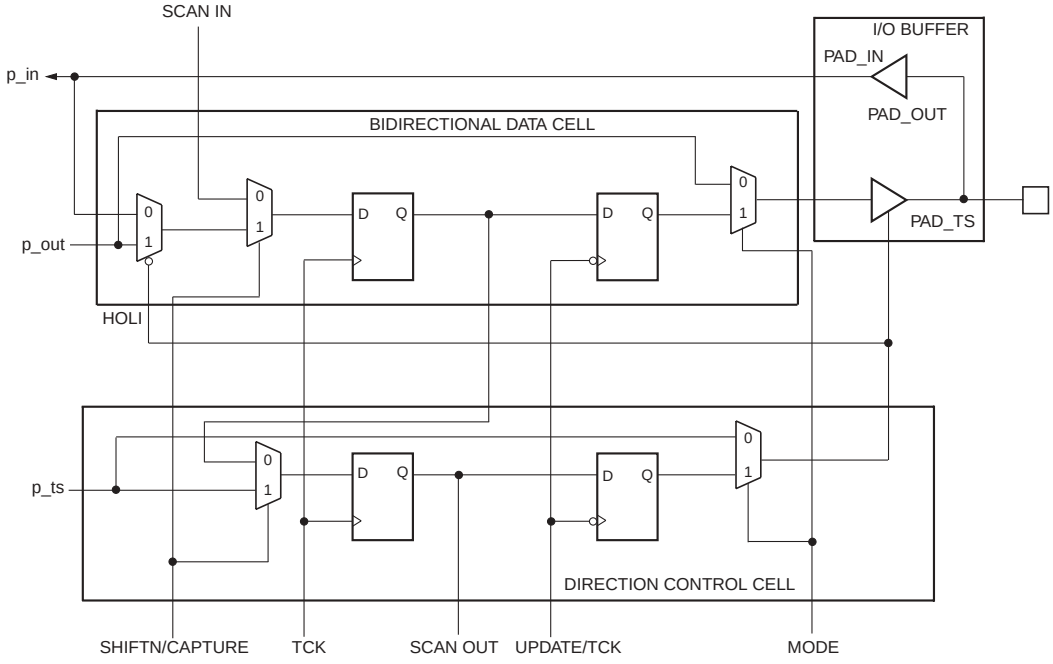
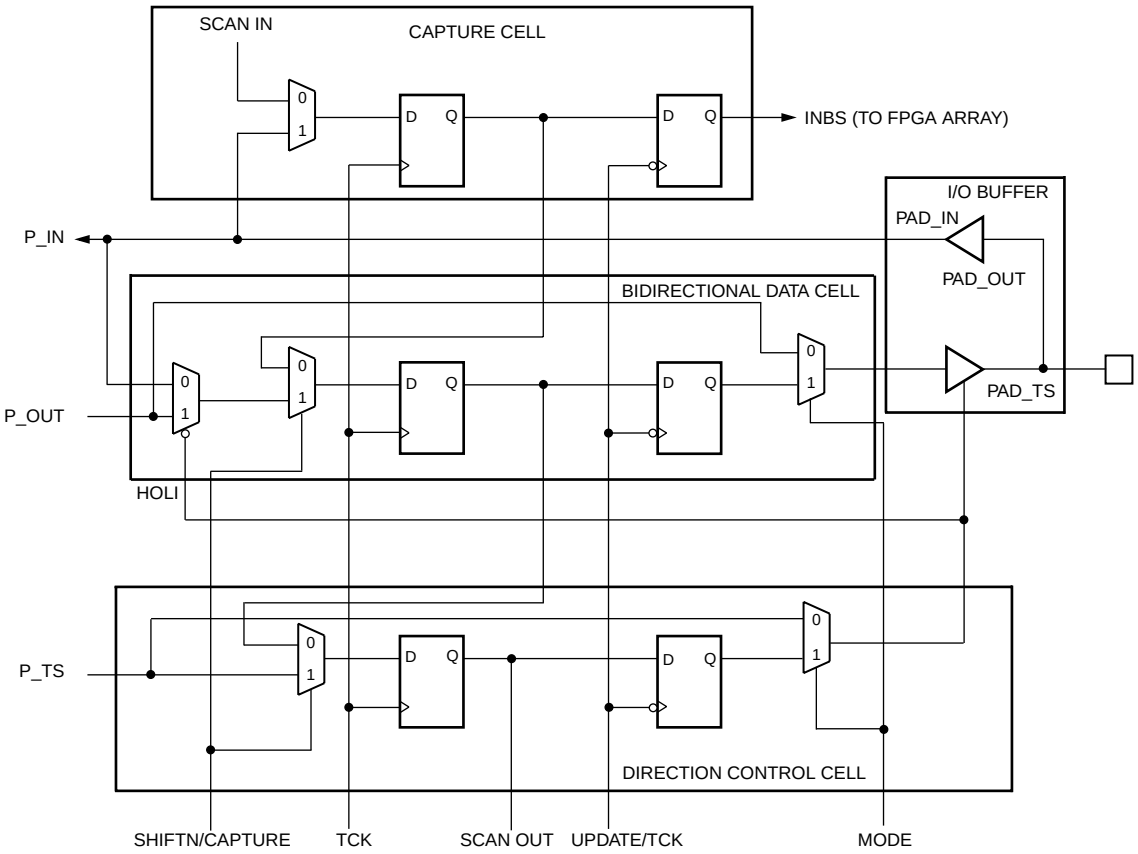


Figure 4. Boundary-Scan Cell (BSC), ORCA Series 4 Devices



The user-accessible I/O pins in the PICs are configured as bidirectional buffers during the device-level boundary-scan test. Therefore, two registers are needed to access the input, output, and 3-state values for each programmable I/O pin. The first is the bidirectional data cell which is used to access the input or output data. The second is the direction control cell which is used to access the 3-state value. The boundary-scan shift register is a series connection of a bidirectional data cell and a direction control cell for each I/O in the boundary-scan chain, as shown in Figure 3 for ORCA Series 3 devices and Figure 4 for ORCA Series 4 devices.

The bidirectional data cell and direction control cell each include a flip-flop used to shift scan data and an update flip-flop to control the I/O buffer. The bi-directional data cell is controlled by the high out, low in (HOLI) signal generated by the direction control cell.

When HOLI is low, the bidirectional data cell takes input buffer data into the boundary-scan register. When HOLI is high, the boundary-scan register is loaded with functional data from the internal core logic.

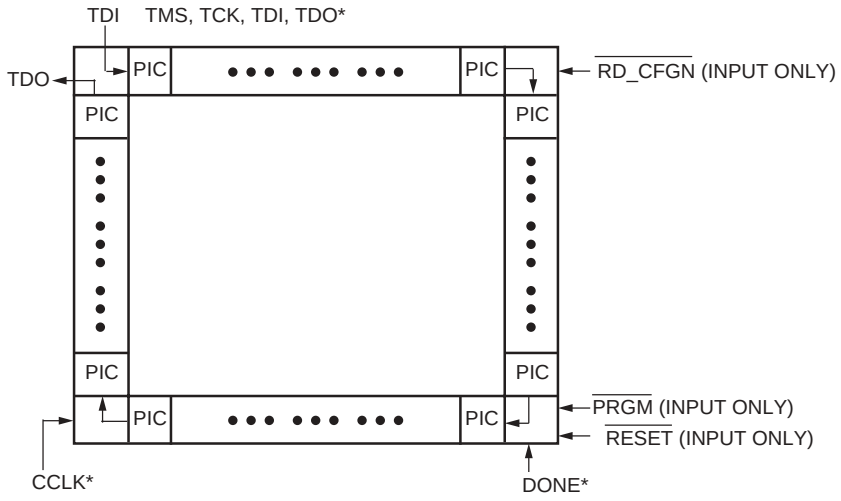
When the MODE signal that is generated by the instruction decoder is high (extest mode) and the buffer is configured as an output, the scan data is propagated to the output buffer. When the MODE signal is low (bypass or sample modes) and the buffer is configured as an output, functional data from the internal core is propagated to the output buffer.

Four other global signals (capture, update, shiftn, and treset) that are generated by BSTAP controller, as well as the boundary-scan clock (TCK), are used to control the shift register containing the bidirectional data cells and the direction control cells.

The first flip-flop in the boundary-scan shift register is for the first PIC I/O pin on the left of the top side of the ORCA device. The shift register then proceeds in a clockwise motion until reaching the first PIC I/O pin on the top of the

left side of the ORCA device. Figure 5 shows the full chip arrangement of this boundary-scan chain for the ORCA series.

Figure 5. ORCA Series Boundary-Scan Chain



* TMS, TCK, TDI, TDO, CCLK, and DONE are not included in the boundary-scan register.

Description of the Three Mandatory and the Four User-Defined Instructions

ORCA boundary-scan logic supports three mandatory instructions in IEEE Std. 1149.1-1990 and four user defined instructions as shown in Table 1.

When the EXTEST instruction is activated in an ORCA device, either the scan data at input pins is loaded into the boundary-scan shift register with the rising edge of TCK in Capture-DR controller state, or the scan data at output pins is updated from the boundary-scan shift register with the falling edge of TCK in Update-DR controller state (depending on the value of the 3-state signal).

The SAMPLE/PRELOAD instruction allows a snapshot of the functional data present at the I/O pins. When the sample/preload instruction is selected in a device, the functional data at the pins is loaded into the boundary-scan shift register with the rising edge of TCK in the Capture-DR controller state and the captured functional data is shifted out to the TDO output pin with the Shift-DR controller state. The selection between input data and output data at each pin is determined by whether the pin is currently an input or an output.

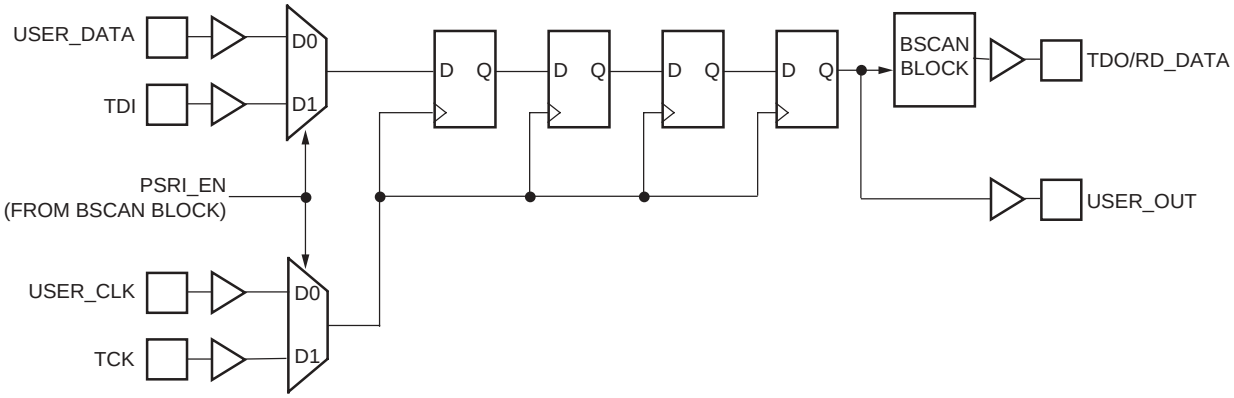
The BYPASS instruction allows the serial scan data (through the TDI input pin) to be shifted out of the TDO output with a delay of one TCK clock period without interfering with the FPGA's normal functionality.

The PSR1 and PSR2 user instructions are provided to allow the implementation of a pair of user-defined internal scan paths using the PLC registers. The data is shifted in on TDI and shifted out on TDO by the test clock (TCK). Connectivity to the general FPGA routing is provided for TCK, TDI, a scan path enable signal, and a shift data out signal for each instruction. An example of these scan paths is shown in Figure 6.

The RAM_W (configuration RAM write) allows the user to program the configuration memory by shifting serial configuration data in on TDI with the test clock (TCK). This instruction is available both before and after configuration.

The RAM_R (readback RAM read) allows the user to read back the configuration memory by shifting the data out on the TDO output pin. This instruction is only available after configuration.

Figure 6. Example of Boundary-Scan User-Defined Scan Path Logic



Usage of Boundary-Scan Logic

As mentioned earlier, the power-on reset circuitry resets the boundary-scan logic during power-on to prevent all I/O pins from causing contention. In addition, an external $\overline{\text{PRGM}}$ pin is provided not only to reset the boundary-scan logic but also to reprogram the ORCA device when the $\overline{\text{PRGM}}$ pin is low.

The $\overline{\text{PRGM}}$ pin is a part of the boundary-scan chain. However, this pin must be high during boundary-scan operation, configuration, and normal operation unless it is necessary to reset the boundary-scan logic or to reconfigure the ORCA device. This pin is not considered the optional reset pin as defined in IEEE Std. 1149.1-1990.

The boundary-scan function is always enabled during initialization and configuration. Therefore, the bypass instruction is always available and can be executed at any time without any restriction. Although the boundary-scan logic is enabled during initialization, other instructions (extest, sample/preload) are not allowed to be used during initialization. This requires that the user keep the boundary-scan logic in either reset mode or bypass mode during initialization. This is also true during configuration when boundary-scan is not being used.

It is recommended that either the TMS or the TCK pin be tied high so that the boundary-scan logic will be in the test-logic reset state when the boundary-scan logic is not to be used during initialization and configuration. This recommendation also applies to the user who is not using boundary-scan as well to avoid the accidental activation of the boundary-scan logic.

The three mandatory instructions (bypass, extest and sample/preload) and the ram_w instruction are available as soon as the $\overline{\text{INIT}}$ pin goes high (indicating the completion of initialization). Before configuration, the three mandatory instructions are fully supported and can be exercised to test interconnections between the integrated circuits on the board.

Because all the I/O buffers can be bidirectional buffers, it is necessary to avoid the simultaneous switching of too many output buffers when the Update-DR controller state is asserted. The normal rules in the ORCA data sheet for simultaneous switching outputs should be followed at all times.

The ORCA device can be configured by using the ram_w instruction. If this instruction is to be applied before configuration, the $\overline{\text{INIT}}$ pin must be high, signaling the end of initialization. Serial configuration data is then supplied on TDI and is clocked in with TCK. The special configuration pins $\overline{\text{LDC}}$, HDC, $\overline{\text{INIT}}$, and DONE function the same as during any other configuration process.

If the ram_w instruction is asserted after configuration is done, the FPGA is first reinitialized. Thus, the user must wait until the $\overline{\text{INIT}}$ pin is high before applying the serial configuration data. In order to guarantee that the ram_w instruction works properly after configuration, the user should apply at least three TCK cycles after applying the ram_w instruction. Timing diagrams of the ram_w instruction both before and after configuration are shown in Figures 6 and 7.

Figure 7. ram_w Timing Diagram Before Configuration

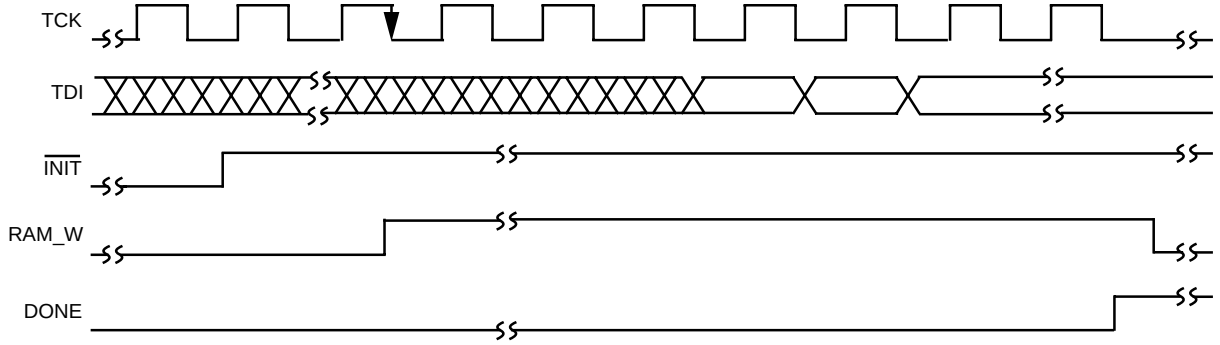


Figure 8. ram_w Timing Diagram After Configuration

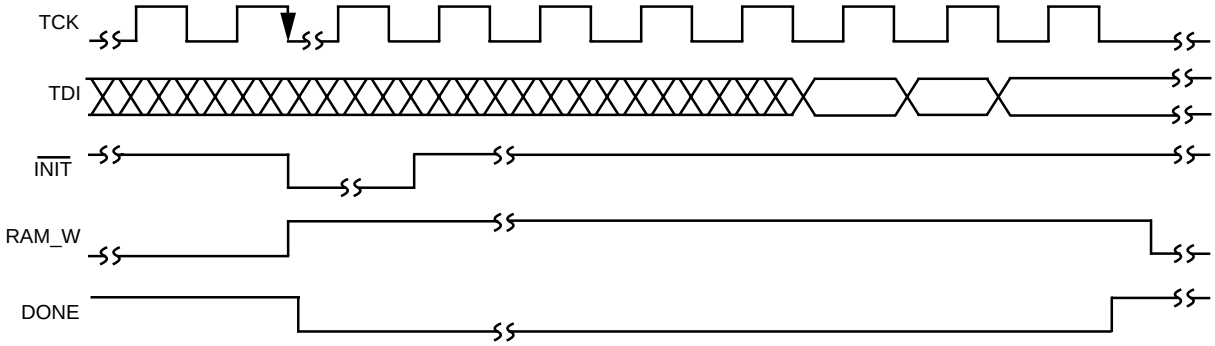
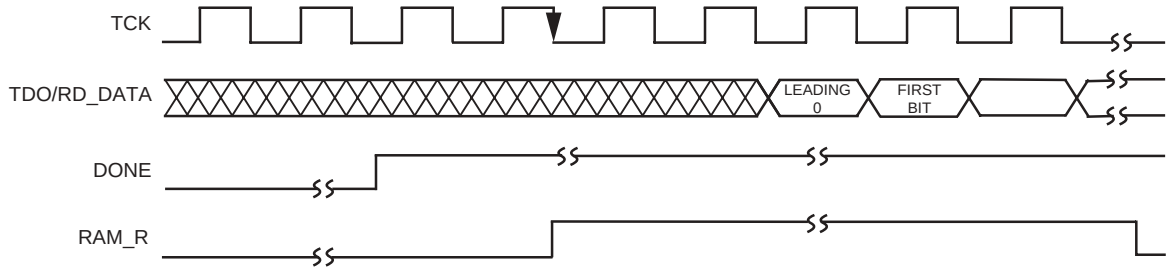


Figure 9. ran_r Timing Diagram After Configuration



The three mandatory and the four user-defined instructions are available after configuration when the boundary-scan logic is selected by setting the jtag_en ram bit high. If this RAM bit is not set, the boundary-scan logic is disabled and the TMS, TCK, and TDI pins can be used as normal I/O pins. When a ram_r instruction is asserted after configuration, the configuration memory contents is shifted out of the TDO output buffer. It should be noted that this readback data is clocked out of TDO on the falling edge of TCK and is valid two TCK clock cycles after the ram_r instruction is asserted. The maximum frequency of TCK is 10 MHz. Figure 9 is a timing diagram of the ram_r instruction.

Boundary-Scan Description Language

The boundary-scan description language (BSDL) files are generated by software and follow the standard format. These BSDL files provide the pinout for all of the different package types supported by ORCA as well as additional boundary-scan information. The BSDL files can be obtained from your Lattice Semiconductor FAE.

User Design Guidelines

To enable boundary-scan in a user design after configuration, the BNDSCAN element must be instantiated. The BNDSCAN component's inputs and outputs should be connected in accordance with the Boundary Scan informa-

tion in the ORCA data sheet, and the description of the BNDSCAN element in the macro library. Typically PTDI, PTMS, and PLCK are connected to the I/O-TDI, I/O-TMS, I/O-TCK pad inputs of the device, respectively. The BSO1 and the BSO2 inputs, if not used, should be grounded. The standard I/Os TDI, TMS, TCK serve as test inputs for boundary scan and for normal operation. The TDO output is connected to the RD_DATA/TDO pin of the device. All the above connections should be made in the source code (HDL or schematic), before mapping.

It should be noted that after routing a design containing a BNDSCAN component, the connections to the component have disappeared, but the JTAG component is active (highlighted in blue in EPIC). This is a correct implementation as the TDI, TMS, TCK, and RD_DATA/TDO are dedicated for boundary scan only, and the connections are IMPLICITLY understood when the JTAG component is activated. The important point is that the JTAG component must be active, to initiate boundary scan after configuration.

The last requirement to enable boundary-scan after device configuration is to set the “Generate Bitstream Data” “Advanced Option” property “JTAG after Configuration” to True in the ispLEVER™ software package.

The following is a VHDL example of instantiating the BNDSCAN component in a user design.

```
-- this library must be in the VHDL code !
library ORCA4;
use ORCA4.orcacomp.all;

-- add this to your architecture, No component declaration
is needed !
-- the jtag_t* must be placed to the dedicated I/O's

J1 : BNDSCAN
   port map
       (
        PTDI  => jtag_tdi,
        PTMS  => jtag_tms,
        PTCK  => jtag_tck,
        BSO1  => low,
        BSO2  => low,
        TDI   => open,
        TCK   => open,
        BSEN1 => open,
        BSEN2 => open,
        TDO   => jtag_tdo
       );
```

References

The following list contains the names of publications that can provide more detailed information about the IEEE Std. 1149.1-1990 boundary-scan specification and application.

C. M. Maunder & R. E. Tulloss. “An Introduction to the Boundary-Scan Standard,” Journal of Electronic Testing and Applications, 1991, pp. 27-42.

IEEE Std. 1149.1-1990 Test Access Port and Boundary-Scan Architecture, IEEE Computer Society, May 1990.

Parker, Kenneth P., The Boundary-Scan Handbook, Kluwer Academic Publishers.

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