Application Note
January 2002

ORCA® Series 3 to Series 4 FPGA Design Conversion

Introduction

A major design consideration of the *ORCA* Foundry software was to facilitate easy migration. The Series 4 software has been designed to provide maximum compatibility for users to migrate their Series 3 designs to Series 4 devices. It should involve minimum conversion effort for most designs. This application note explains caveats and conversion steps for sucessful migration into the Series 4 device domain.

Clock Controllers

There are no clock controllers in Series 4 FPGAs like there were for Series 3 FPGAs. For Series 3, the macro library elements for the clock controllers are:

- CLKCNTLB clock control/shutoff (in LOW state)—bottom mid site
- CLKCNTLL clock control/shutoff (in LOW state)—left mid site
- CLKCNTLR clock control/shutoff (in LOW state)—right mid site
- CLKCNTLT clock control/shutoff (in LOW state)—top mid site
- CLKCNTHB clock control/shutoff (in HIGH state)—bottom mid site
- CLKCNTHL clock control/shutoff (in HIGH state)—left mid site
- CLKCNTHR clock control/shutoff (in HIGH state)—right mid site
- CLKCNTHT clock control/shutoff (in HIGH state)—top mid site

If your design has any of these elements, they need to be removed for the design to be implemented in a Series 4 device. To do this, just connect the input signal of the clock controller to the output signal of the clock controller and remove any instance of the clock controller and shut-off signal and driver. There is no shut-off feature for clocks in the Series 4 devices. In other words, make the clock controller a short. See Figure 1.

Clock Controllers (continued)

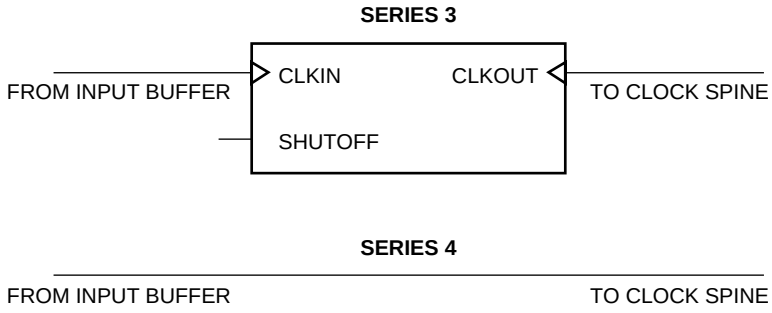

Figure 1. Clock Controller Conversion

The main function of the clock controllers in the Series 3 FPGA devices was to provide access to the express clock (ECLK). For Series 4, the express clock equivalent is the new edge clock. The Series 4 edge clocks can be driven by any external I/O buffer or PLL. Refer to the *Series 4 Clocking Strategies* Application Note (AP00-073FPGA) for details about edge clock usage.

Programmable Clock Managers

The pair of Series 3 programmable clock managers (PCMs) are replaced by eight (8) phase-lock loop (PLL) filters in the Series 4 FPGA devices. There are two methods for converting these clock management library macro elements. One is to simply leave the Series 3 PCM instantiations in your design with a possible attribute change, to be explained below. The other method is to replace any Series 3 PCM with a new, functionally equivalent, Series 4 PLL library macro element.

The Series 3 PCM library elements are:

- DLL1XB programmable clock manager (delay-locked loop)—bottom
- DLL1XT programmable clock manager (delay-locked loop)—top
- DLLPDB programmable clock manager (programmable delay, delay-locked loop)—bottom
- DLLPDT programmable clock manager (programmable delay, delay-locked loop)—top
- PLLB programmable clock manager (phase-locked loop)—bottom
- PLLT programmable clock manager (phase-locked loop)—top
- PCMB programmable clock manager—bottom
- PCMT programmable clock manager—top
- PCMBUFB programmable clock manager in bypass mode—bottom
- PCMBUFT programmable clock manager in bypass mode—top

Method 1

The user can keep the same Series 3 library elements with the following attribute modifications. Replace the DUTY duty cycle attribute for DLL1XT and DLL1XB elements with the VCOTAP attribute. Replace the PDELAY phase delay attribute for DLLPDB and DLLPDT elements with the VCOTAP attribute.

In Series 3, the PLL voltage-controlled oscillators have 32 taps, and in Series 4, they have eight taps. The VCOTAP attribute controls which of the eight taps to source from; thus, this attribute controls the quanta of phase shift or duty cycle adjustment for the Series 4 programmable PLLs. Please refer to the *Series 4 PLL* Application Note for more details about usage and capabilities of these elements.

For PLLT and PLLB elements, the user has to connect the FB input pin; it cannot be left open like allowed with the Series 3 PCMs.

Method 2

Replace any Series 3 PCM element with a Series 4 programmable PLL (PPLL). The ports for this element are:

INPUTS: CLKIN, FB

OUTPUTS: MCLK, NCLK, LOCK, INTFB

In Series 4, the MCLK port is replacing the Series 3 ECLK port and the Series 4 NCLK port is replacing the Series 3 SCLK port.

The following shows the attribute values to use on the PPLL Series 4 library element when replacing a Series 3 PCM library element. Note that these element instantiations, with their respective attached attributes, can be generated in HDL by the *ORCA* Foundry *SCUBA*® program; please see the ORCA *Series 4 PLL* Application Note for more details.

For replacing DLL1XB use: (FB and INTFB to be tied together)

DIV0: 1, 2, 3, 4, 5, 6, 7, 8

MCLKMODE: DUTYCYCLE

NCLKMODE: DUTYCYCLE

VCOTAP: 0, 1, 2, 3, 4, 5, 6, 7

Programmable Clock Managers

(continued)

For replacing DLL1XT use (FB and INTFB to be tied together):

DIV0: 1, 2, 3, 4, 5, 6, 7, 8

MCLKMODE: DUTYCYCLE

NCLKMODE: DUTYCYCLE

VCOTAP: 0, 1, 2, 3, 4, 5, 6, 7

For replacing DLLPDB use (FB and INTFB to be tied together):

DIV0: 1, 2, 3, 4, 5, 6, 7, 8

DIV2: 1, 2, 3, 4, 5, 6, 7, 8

MCLKMODE: DELAY

NCLKMODE: DELAY

VCOTAP: 0, 1, 2, 3, 4, 5, 6, 7

For replacing DLLPDT use (FB and INTFB to be tied together):

DIV0: 1, 2, 3, 4, 5, 6, 7, 8

DIV2: 1, 2, 3, 4, 5, 6, 7, 8

MCLKMODE: DELAY

NCLKMODE: DELAY

VCOTAP: 0, 1, 2, 3, 4, 5, 6, 7

For replacing PCMBUFB use:

MCLKMODE: BYPASS

NCLKMODE: BYPASS

For replacing PCMBUFT use:

MCLKMODE: BYPASS

NCLKMODE: BYPASS

For replacing PLLB use:

DIV0: 1, 2, 3, 4, 5, 6, 7, 8

DIV1: 1, 2, 3, 4, 5, 6, 7, 8

DIV2: 1, 2, 3, 4, 5, 6, 7, 8

MCLKMODE: DELAY

NCLKMODE: DELAY

For replacing PLLT use:

INPUTS: CLKIN, FB

OUTPUTS: MCLK, NCLK, LOCK, INTFB

PROPERTIES DIV0: 1, 2, 3, 4, 5, 6, 7, 8

DIV1: 1, 2, 3, 4, 5, 6, 7, 8

DIV2: 1, 2, 3, 4, 5, 6, 7, 8

MCLKMODE: DELAY

NCLKMODE: DELAY

I/O Cell Output Multiplexers

There are logic elements in the programmable I/O cells (PICs) in both the Series 3 and the Series 4 FPGA devices. From the user's perspective, this logic is the same between the two Series, except for the case of the 2-input ouput MUXes. These are the OSMUX21 and OEMUX21 library elements, with the SCLK or ECLK as the select input. These can still be used in the Series 4 devices, but their connectivity is different. When converting a Series 3 design to a Series 4 device, any of these elements in the design must be rewired as follows.

With Series 3, the D0 and the D1 inputs of the multiplexor could be driven by any array logic (PFU). With Series 4, the D1 input must come from the PIO output register. Therefore, in 4E designs, this element must be paired with a flip-flop or a latch.

To get the same functionality of the Series 3 design in the Series 4 device, instantiate a positive-level I/O latch (e.g., an OFS1S1B library element), connect the former D1 data signal to the D data input to this latch, connect the Q output of the latch to D1 input port of the OSMUX21 (or OEMUX21), and connect the same clock on the MUX select to the clock input port on the latch. See Figure 2.

The data will be captured on the positive level of the SCLK (or ECLK) and then, a half cyle later, on the negative level of the clock, the same clock will select this Q data (connected to the MUX D1 input) as the output of the MUX.

I/O Cell Output Multiplexers (continued)

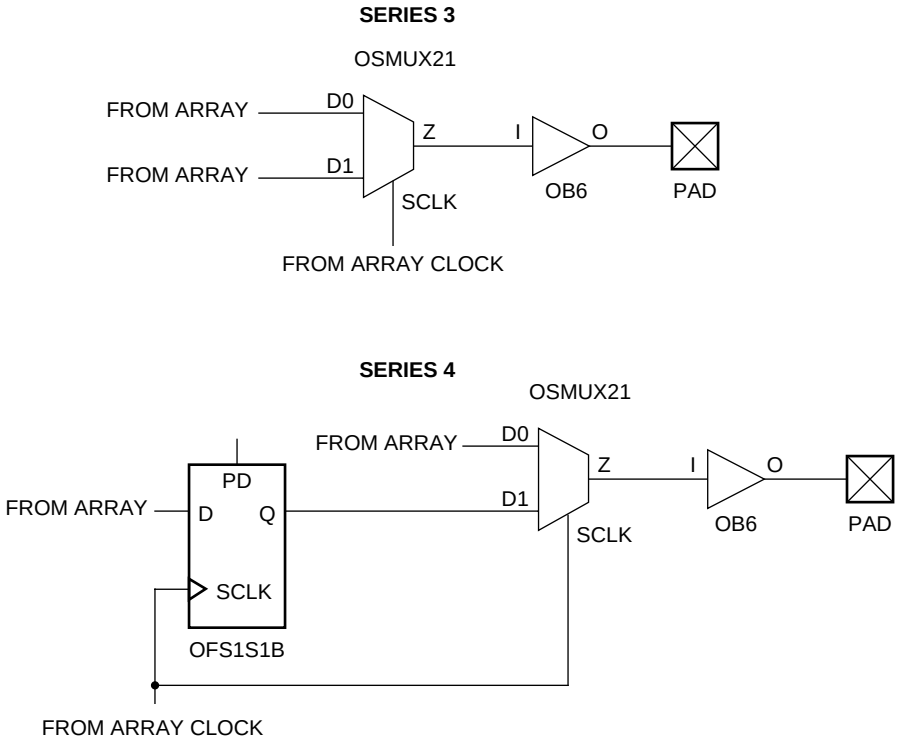

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Figure 2. I/O MUX Conversion

Miscellaneous Tips

In addition to the library element changes discussed above, observe the following items when migrating to Series 4 devices.

- When retargeting 3C designs to the 4E, make sure that the .EDI.F file does not have the LIBRARY property set to or3c00; if it does, just delete it with a text editor.
- Do not run the Series 4 mapper with a Series 3 .ngd file.
- Series 3 macros cannot be used in Series 4 designs.
- Netlists using obsolete library cells migrated from Series 2 designs (e.g., pfund, pfund0, pfuxr, pfumxn, and pfundn) are not supported.
- When viewing the 4E architecture in EPIC, expect to see the following:
  — The upper left PFU in each device is at R3C2.
  — Buses are routed on half-length lines.
  — The PIOs and block RAMs look unconnected from the rest of the device. This is on purpose; it is the basis of the platform technology for which Series 4 is designed. The connections to the rest of the device will be visible after routing in some cases.

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Lattice Semiconductor Corporation