

Introduction

The memory in LatticeECP™ and LatticeEC™ FPGAs is built using volatile SRAM. When the power is removed, the SRAM cells lose their contents. A supporting non-volatile memory is required to configure the device on power-up and at any time the device needs to be updated. The LatticeECP/EC devices support a sysCONFIG™ interface that provides multiple configuration modes as well as the dedicated ispJTAG™ port and boundary scan. The different programming modes are listed below.

- SPI
- SPIX
- Master Serial
- Slave Serial
- Master Parallel
- Slave Parallel
- ispJTAG (1149.1 Interface)

This technical note covers all the configuration options available for LatticeECP/EC devices.

Configuration Pins

The LatticeECP/EC devices support two types of sysCONFIG pins, dedicated and dual-purpose. The dedicated pins are used exclusively for configuration; the dual-purpose pins are available as extra I/O pins. If a dual-purpose pin is to be used both for configuration and as a general purpose I/O the user must adhere to the following:

- The general purpose I/O (GPIO) must maintain the same direction as it has during configuration, in other words, if the pin is an input during configuration it must remain an input as a GPIO, if an output during configuration it must remain an output as a GPIO, if a bi-directional it must remain a bi-directional as a GPIO.
- The I/O type must remain the same, in other words if the pin is a 3.3V CMOS pin (LVCMOS33) during configuration it must remain a 3.3V CMOS pin as a GPIO.
- The Persistent option must be set to OFF. The Persistent option can be accessed by using the Preference Editor in ispLEVER®.
- The user is responsible for insuring that no internal or external logic will interfere with device configuration.

Also note, if a parallel configuration mode is not being used then one or both of the parallel port chip selects (CSN, CS1N) must be high or tri-state during configuration.

Programmable options control the dual-purpose configuration pins. These options are controlled via a preference in Lattice ispLEVER software, or as an HDL source file attribute. The LatticeECP/EC devices also support the ispJTAG port for configuration, including transparent read back and JTAG testing. The following sections describe the functionality of the sysCONFIG and JTAG pins. Table 13-1 is provided for reference.

Table 13-1. Configuration Pins for LatticeECP/EC Devices

Pin(s)	Description	Default Pin Function	Mode Used
CFG[0:2]	Input	Dedicated	All
PROGRAMN	Input	Dedicated	All
INITN	Bi-directional open drain	Dedicated	All
DONE ¹	Bi-directional	Dedicated	All
CCLK	Output or input	Dedicated	MASTER = output, SLAVE = input
DI/CSSPIN	Input/output with weak pull-up	—	SERIAL/SPI
DOUT/CSON	Output	—	SERIAL/PARALLEL
CSN	Input	—	PARALLEL
CS1N	Input	—	PARALLEL
WRITEN	Input	—	PARALLEL
BUSY/SISPI	Output	—	PARALLEL/SPI
D[0:7]/SPID[7:0]	Input or output	—	PARALLEL/SPI
TDI	Input with pull-up	Dedicated	JTAG
TDO	Output	Dedicated	JTAG
TCK	Input with hysteresis, no pull-up	Dedicated	JTAG
TMS	Input with pull-up	Dedicated	JTAG

1. Defaults to open drain with an internal pull-up.

Dedicated Control Pins

The following is a description of the LatticeECP/EC's dedicated sysCONFIG pins used for controlling configuration.

CFG[0:2]

The Configuration Mode pins CFG[0:2] are input pins. They are used to select the configuration mode. Depending on the configuration mode selected, different groups of dual-purpose configuration pins will be activated on Power-On-Reset or when the PROGRAMN pin is driven low.

PROGRAMN

The PROGRAMN pin is an input to the device used to initiate a Programming sequence. A high to low signal applied to the pin sets the device into configuration mode. The PROGRAMN pin can be used to trigger programming other than at powering up. If the device is using JTAG, the device will ignore the PROGRAMN pin until the device is released from the JTAG mode.

INITN

The INITN pin is a bidirectional open drain control pin. It is capable of driving a low pulse out as well as detecting a low pulse driven in. When the PROGRAMN Pin is driven low, or after the internal Power-On-Reset signal is released during Power-up, the INITN pin will be driven low to reset the configuration circuitry and any External PROM. The configuration memory will be cleared and the INITN pin will remain low as long as the PROGRAMN pin is low. To delay configuration the INITN pin can be held low externally. The device will not enter configuration mode as long as the INITN pin is held low. Toggling the PROGRAMN pin in Serial and Parallel programming modes will initiate the configuration sequence and reset the INITN pin. For SPI mode, power cycling the device will initiate the reconfiguration sequence.

During configuration, the INITN pin becomes an error detection pin. It will be driven low whenever a configuration error occurs.

DONE

The DONE pin is a bidirectional control pin. It can be configured as an open drain or active drive control pin. The DONE pin will be driven low when the device is in configuration mode and the internal DONE bit is not programmed. When the INITN and PROGRAMN pins are high and the DONE bit is programmed, the DONE pin will be

released. An open drain DONE pin can be held low externally and, depending on the wake-up sequence selected, the device will not become functional until the DONE pin is released.

CCLK

The CCLK pin is a bi-directional pin. The direction depends on whether a Master Mode or Slave Mode is selected. If a Master Mode is selected when the CFG pins are sampled, the CCLK pin will become an output pin; otherwise CCLK will become an input pin. If the CCLK pin becomes an output pin, the internal programmable oscillator is connected to the CCLK and is driven out to slave devices. CCLK will stop 120 clock cycles after the DONE pin is brought high and the device wake-up sequence completed. The extra clock cycles are provided to ensure that enough clock cycles are provided to wake up other devices in the chain. When stopped, CCLK will become tri-stated as an input. The CCLK will restart on the next configuration initialization sequence, such as the PROGRAMN pin being toggled. The MCCLK_FREQ Parameter controls the CCLK Master frequency. See the Master Clock Selection section of this document for more information. For Serial and Parallel Slave modes, it is recommended that CCLK is continuously active during configuration and error recovery sequence.

Dual-Purpose sysCONFIG Pins

The following is a list of dual-purpose sysCONFIG pins. If any of these pins are used for configuration and user I/O, the user must adhere to the requirements listed above in the section entitled Configuration Pins.

DI/CSSPIN

The DI/CSSPIN dual-purpose pin is designated as DI (Data Input) for all of the serial bit stream configurations, such as Slave Serial. DI has an internal weak pull up.

In either SPI or SPIX mode, the DI/CSSPIN becomes the dedicated Chip Select output to drive the SPI Flash chip select. CSSPIN will drive high when the LatticeECP/EC device is not in the process of configuration through the SPI Port.

D[0:7]/SPID[7:0]

The D[0:7] pins support both the SPI mode and Parallel configuration modes. In the Parallel configuration modes, the D[0:7] pins are tri-stated bi-directional I/O pins used for parallel data write and read. A byte of data is driven into or read from these pins. When the WRITEN signal is low and the CSN and CS1N pins are low, the D[0:7] pins will become an input. When the WRITEN signal is driven high and the CSN and CS1N pins are low, the pins become output pins for reading. The PERSISTENT preference must be set to support read back to preserve the D[0:7] pins so the device can monitor for the read back instruction. The CSN and CS1N pins will enable the Data D[0:7] pins.

In SPI mode, the D[0:7]/SPID[7:0] pins become individual inputs for one or more SPI memory outputs. If more than one SPI memory is used, SPI memory zero output will be wired to D7/SPID0, SPI memory one output will be wired to D6/SPID1, the data fed to these pins will be interleaved and then sent to the internal configuration engine. For SPIX Mode, the D[0:7]/SPID[7:0] pins will also support sampling of external resistors for determining the Read Op Code.

DOUT/CSON

The DOUT/CSON pin is an output pin and has two purposes. For serial and parallel configuration modes, when the BYPASS mode is selected, this pin will become DOUT. When the device in BYPASS becomes fully configured, a BYPASS instruction will be executed and the data on DI or D[0:7] will then be presented to the DOUT pin through a bypass register to serially pass the data to the next device. In a parallel configuration mode D0 will be shifted out first followed by D1, D2, and so on.

For parallel configuration modes, when the FLOW_THROUGH mode is selected, this pin will become the Chip Select OUT (CSON). In the FLOW_THROUGH mode, when the device is fully configured, the Flow Through instruction will be executed and the CSON pin will be driven low to enable the next device chip select pin.

The DOUT/CSON bypass register will drive out a HIGH upon power up and continue to do so till the execution of the Bypass/Flow Through instruction within the bit stream.

CSN and CS1N

Both CSN and CS1N are active low control input pins. When CSN OR CS1N are high, D[0:7] and BUSY pins are tri-stated. When the CSN and CS1N pins are both high, they will reset the flow-through/bypass register. CSN and CS1N are interchangeable when controlling the D[0:7], INITN and BUSY pins.

WRITEN

The WRITEN pin is an active low control input pin. The WRITEN pin is used to determine the direction of the data pins D[0:7]. The WRITEN pin is driven low when a byte of data is to be shifted into the device during programming. The WRITEN pin will be driven high when data is to be read from the device through a parallel configuration mode. The WRITEN pin is not used for serial configuration modes.

BUSY/SISPI

The BUSY/SISPI pin is a dual function pin. In the parallel configuration mode, the BUSY pin is a tri-stated output. The BUSY pin will be driven low by the device only when it is ready to receive a byte of data at D[0:7] pins or a byte of data is ready for reading. The BUSY pin can be used to support asynchronous peripheral mode. This is to acknowledge that the device might need extra time to execute a command.

In the SPI configuration modes, the BUSY/SISPI pin becomes an output pin that drives read control data back to the SPI memory.

ispJTAG Pins

The ispJTAG pins are the standard IEEE 1149.1 TAP pins. The ispJTAG pins are dedicated pins and are always accessible when the LatticeECP/EC device is powered up. In addition, the dedicated sysCONFIG pins such as the DONE pin as described in the Dual-Purpose Control Pins section of this document are also available when using LatticeECP/EC ispJTAG pins. The dedicated sysCONFIG pins are not required for JTAG operation, but may be useful at times.

TDO

The Test Data Output pin is used to shift out serial test instructions and data. When TDO is not being driven by the internal circuitry, the pin will be in a high impedance state.

TDI

The Test Data Input pin is used to shift in serial test instruction and data. An internal pull-up resistor on the TDI pin is provided. The internal resistor is pulled up to V_{CCJ} .

TMS

The Test Mode Select pin controls test operations on the TAP controller. On the falling edge of TCK, depending on if TMS is high or low, a transition will be made in the TAP controller state machine. An internal pull-up resistor on the TMS pin is provided. The internal resistor is pulled up to V_{CCJ} .

TCK

The test clock pin TCK provides the clock to run the TAP controller, loading and reloading the data and instruction registers. TCK can be stopped in either the high or low state and can be clocked at frequencies up to the frequency indicated in the device data sheet. The TCK pin supports hysteresis, with the value shown in the DC parameter table of the LatticeECP/EC Family Data Sheet.

Optional TRST

The JTAG Test Reset pin TRST is not supported in the LatticeECP/EC devices.

 V_{CCJ}

JTAG V_{CC} supplies independent power to the JTAG port to allow chaining with other JTAG devices at a common voltage.

Configuration and JTAG Pin Physical Description

All of the control pins and programming bus default to LVCMOS. The bank V_{CCO} pin determines the voltage level of the sysCONFIG pins. The JTAG pin voltage levels are determined by the V_{CCJ} pin voltage level. Controlling the

JTAG pin by V_{CCJ} allows the device to support different JTAG chain voltages. For further JTAG chain questions, see *In-System Programming Design Guidelines for ispJTAG Devices*, available on the Lattice web site at www.lattice-semi.com.

Configuration Modes

The LatticeECP/EC devices support many different types of configuration modes utilizing either serial or parallel data inputs. On power-up or upon driving the PROGRAMN pin low, the CFG[2:0] pins are sampled to determine the mode the devices will be configured in. Table 13-2 lists the Mode, CFG[0:2] state and the software CONFIG_MODE parameters. The following subsections break down each configuration mode individually.

Table 13-2. Configuration Modes for the LatticeECP/EC Devices

Mode	CFG[2]	CFG[1]	CFG[0]	CONFIG_MODE Parameter
SPI Master	0	0	0	SPI
SPIX Master	0	0	1	SPIX
Master Serial (Bypass OFF)	1	0	0	MASTER_SERIAL
Master Serial (Bypass ON)	1	0	0	MASTER_SERIAL_BYPASS
Slave Serial (Bypass OFF)	1	0	1	SLAVE_SERIAL
Slave Serial (Bypass On)	1	0	1	SLAVE_SERIAL_BYPASS
Master Parallel (Flow Through OFF)	1	1	0	MASTER_PARALLEL
Master Parallel (Flow Through ON)	1	1	0	MASTER_PARALLEL_FLOWTHR
Slave Parallel	1	1	1	SLAVE_PARALLEL
Slave Parallel (Bypass ON)	1	1	1	SLAVE_PARALLEL_BYPASS
Slave Parallel (Flow Through ON)	1	1	1	SLAVE_PARALLEL_FLOWTHR
ispJTAG (1149.1 interface)	X	X	X	Any CONFIG_MODE or NONE1

Configuration Options

Several configuration options are available for each configuration mode. When daisy chaining multiple FPGA devices, an overflow option is provided for serial and parallel configuration modes. By setting the proper parameter in the Lattice design software, the selected configuration options are set in the generated bit stream. As the bit stream is loaded into the device, the selected configuration options will take effect. These options are described in the following sections and are software selectable by the Lattice design software.

Bypass Option

The Bypass option is used in parallel and serial device daisy chains. When the device has completed configuration and the Bypass option preference is selected, data coming into the device configuration port will overflow serially out of DOUT to the DI of the next slave serial device. The Bypass configuration selection is supported in the CONFIG_MODE selections as shown in Table 13-2.

In serial configuration mode, the Bypass option connects the DI to DOUT, via a bypass register upon completion of configuration. The bypass register is initialized with a '1' at the beginning of configuration. In parallel configuration mode, the Bypass option causes the data incoming from D[0:7] to be serially shifted to DOUT after completion of configuration. The serialized byte wide register will be shifted to DOUT through the bypass register. D0 of the byte wide data will be shifted out first and followed by D1, D2, and so on.

Once the Bypass option starts, the device will remain in Bypass until the Wake-up sequence completes. One option to get out of the Bypass option is to toggle CSN and CS1N, which will act as a reset signal. Refer to the Master Parallel Mode section of this document for more details.

Flow Though Option

The Flow Through option pulls the CSON pin low when the device has completed its configuration. The Flow Through option can be implemented with either Master or Slave Parallel configuration modes as referenced in

Table 13-2. The Flow Through option will drive out a static low signal on the CSON pin. The Flow Through option will also tri-state the device D[0:7] and BUSY pins when configuration is completed on the device in order to not interfere with the next daisy chained device to be configured.

Once the Flow Through option starts, the device will remain in Flow Through until the Wake-up sequence completes. One option to get out of the Flow Through option is to toggle CSN and CS1N, which will act as a reset signal. Refer to the Master Parallel Mode section of this document for more details.

Master Clock

When the user has determined that a device will be a Master, the CCLK will become an output clock with the frequency set by the user. Until early in the configuration, the device is configured with a default Master Clock Frequency of 2.5MHz. One of the first configuration bits set will be the Master Clock. See the device-specific section of the CFG[0:2] descriptions.

The user can select which Master Clock frequency to use by setting the MCCLK_FREQ preference in the Lattice design software. The MCCLK_FREQ preference will set the frequency of the Master Clock if selected by the CONFIG_MODE and the CFG[0:2] pins. Default is the lowest frequency supported by the device. The user can select a different clock speed, which will take effect just after configuration starts or if the device is reconfigured prior to power down. Configuration time is computed by dividing the maximum configuration bits to be loaded, as given in Figure 13-7, by the Master Clock frequency. See the *LatticeECP/EC FPGA Family Data Sheet* for MCLK_FREQ selections.

SPI Mode

Mode	CFG[2]	CFG[1]	CFG[0]	CONFIG_MODE Parameter
SPI Master	0	0	0	SPI

The LatticeECP/EC devices offer a direct connection for memories that support the SPI standard. By setting the configuration pins CFG[0:2] = b'000, the LatticeECP/EC devices will configure using the SPI interface. The SPI interface offers several combinations of memory to FPGA.

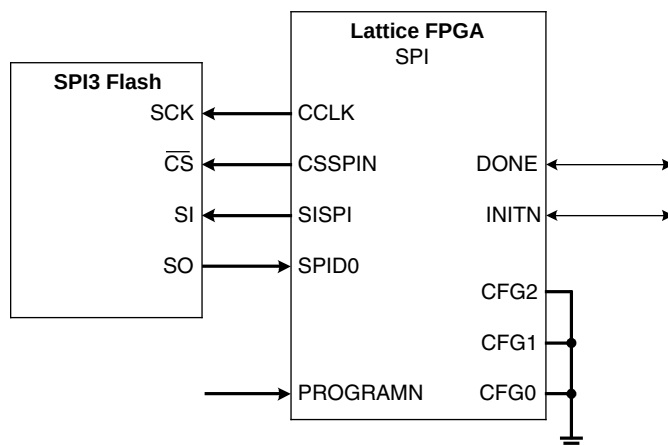
1. One FPGA, one SPI Flash
2. Multiple FPGA, one SPI Flash
3. One FPGA, two SPI Flash
4. Multiple FPGA, multiple SPI Flash is not allowed because the circuitry to support serialization of multiple SPI Flash through DOUT is not available.

For a more detailed discussion the EC/ECP to SPI interface requirements please refer to TN1078.

One FPGA, One SPI Flash

The simple SPI application is one SPI Flash serial connected to the SPID0 of the LatticeECP/EC devices in SPI mode, as shown in Figure 13-1.

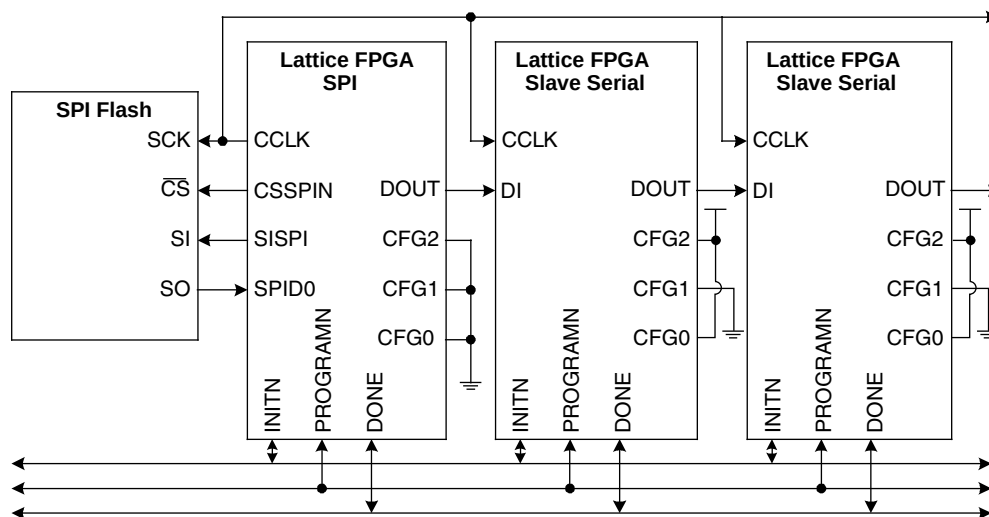
Figure 13-1. Simple Interface for FPGA Bootup in SPI Mode



Multiple FPGA, One SPI Flash

With a sufficiently large SPI Flash, multiple FPGAs can be configured as shown in Figure 13-2. The first FPGA is configured in SPI Mode, the following FPGAs are configured in Slave Serial Mode.

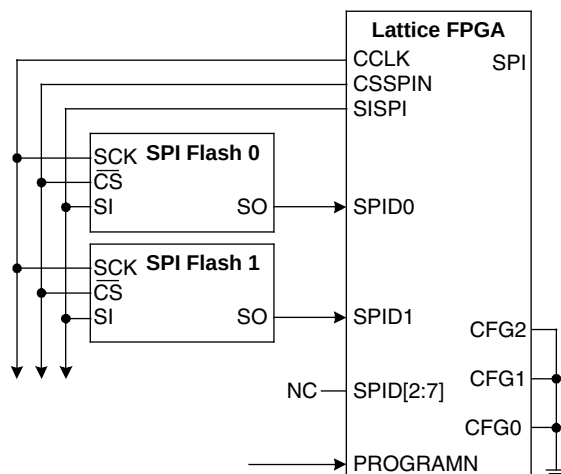
Figure 13-2. Multiple FPGAs Configured by One SPI Flash



One FPGA, Two SPI Flash

The LatticeECP/EC devices support two Flash to configure a single device as shown in Figure 13-3. The two Flash option is supported to allow use of smaller SPI Flash devices to configure a larger FPGA. Lattice's ispVM[®] System software divides the configuration bit stream evenly among each selected SPI memory. As the LatticeECP/EC device starts to download from the two SPI memories, the data streams feed into SPID0 and SPID1 in a parallel fashion and are reassembled internally.

Figure 13-3. Two SPI Flash



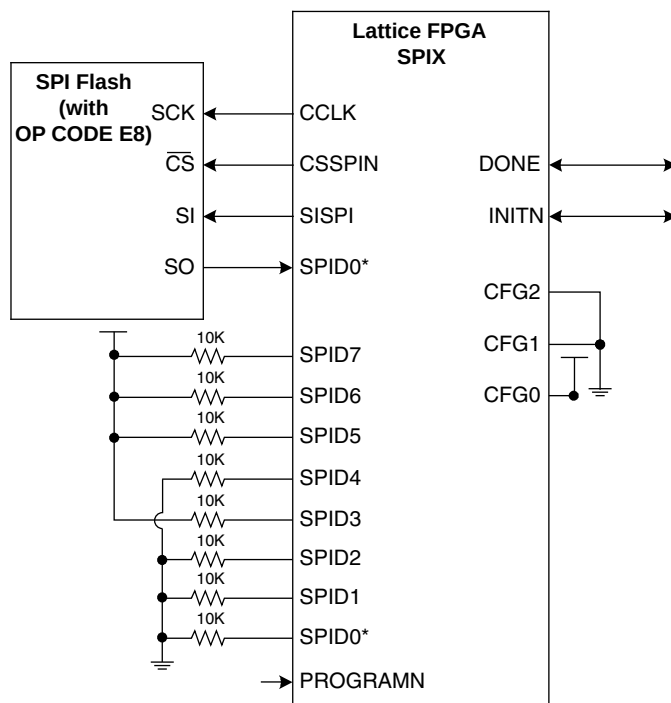
SPIX Mode

Mode	CFG[2]	CFG[1]	CFG[0]	CONFIG_MODE Parameter
SPIX Master	0	0	1	SPIX

Not all SPI memories are the same. A read operation code is required to be fed to the SPI Flash at the time configuration starts. For many, that op code is 03 Hex. For other memories that require a different read operation code other than 03 Hex, the SPIX format is supported. In SPIX mode the read operation code is coded into the SPID[7:0] pins through the use of pull-ups and pull-downs as shown in Figure 13-4. When configuration begins in the SPIX mode the SPID[7:0] pins are sampled and the corresponding sampled read operation code will be fed to the SPI device so the FPGA can begin read back.

All combinations of SPI Flash and LatticeECP/EC FPGAs are valid in the SPIX mode as well. The only addition is the pull-up and pull-down resistors placed on SPID[7:0] as shown in Figure 13-4.

Figure 13-4. Simple SPIX Example with OP CODE Resistors



*SPID0 connects to SO and resistor.

Master Serial Mode

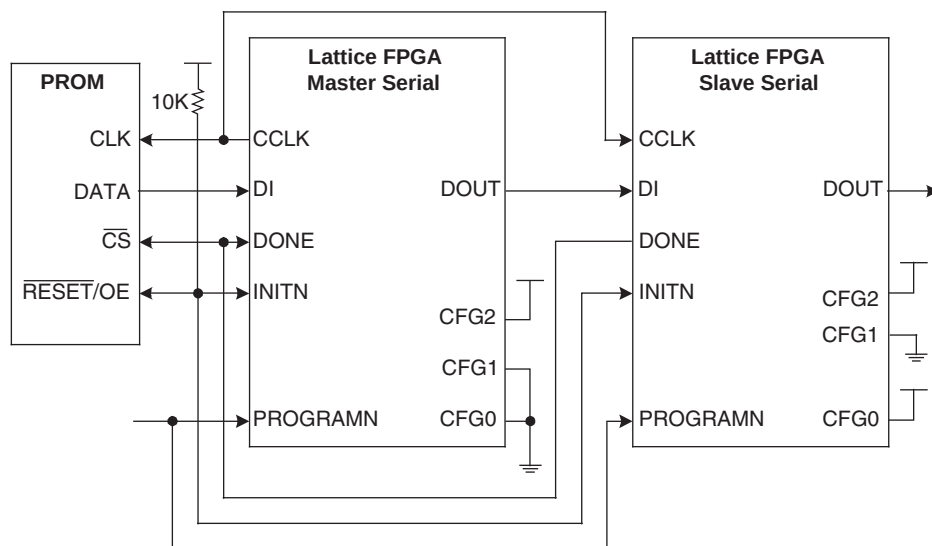
Mode	CFG[2]	CFG[1]	CFG[0]	CONFIG_MODE Parameter
Master Serial (no overflow option)	1	0	0	MASTER_SERIAL
Master Serial (Bypass ON)	1	0	0	MASTER_SERIAL_BYPASS

Configuration of the LatticeECP/EC device in Master Serial mode will drive the CCLK signal out to the Slave Serial devices in the chain and the SPROM that will provide the serial bit stream. The device accepts the data at DI on the rising edge of CCLK. The Master Serial device starts driving CCLK after INITN transitions from low to high and continues to drive the CCLK until the external DONE pin is driven high and one hundred plus clock cycles have been generated. The CCLK frequency on power-up defaults to 2.5MHz. The master clock frequency default remains until the new clock frequency is loaded from the bit stream into the device.

If a Master Serial device is daisy chained with other serial devices, once the master device is fully configured, the bypass option will take effect. As additional data is presented to the Master DI pin, the data will be bypassed to the next device on the DOUT pin.

Figure 13-5 shows a master serial daisy chain. The daisy chain method allows multiple Lattice FPGA devices to be configured together. The first device in the daisy chain operates in Master Serial Mode with the Bypass option, while the other Lattice FPGA devices in the daisy chain operate in Slave Serial Mode.

Figure 13-5. Master and Slave Serial Daisy Chained



Slave Serial Mode

Mode	CFG[2]	CFG[1]	CFG[0]	CONFIG_MODE Parameter
Slave Serial (no overflow option)	1	0	1	SLAVE_SERIAL (Default)
Slave Serial (Bypass On)	1	0	1	SLAVE_SERIAL_BYPASS

Slave Serial Mode is the default mode for configuration in the Lattice design software. In Slave Serial mode the CCLK pin becomes an input and will receive the incoming clock. The device accepts the data at DI on the rising edge of CCLK. After the device is fully configured, if the Bypass option has been set, data sent to DI will be presented to the next device on the DOUT pin as shown in Figure 13-5.

Master Parallel Mode

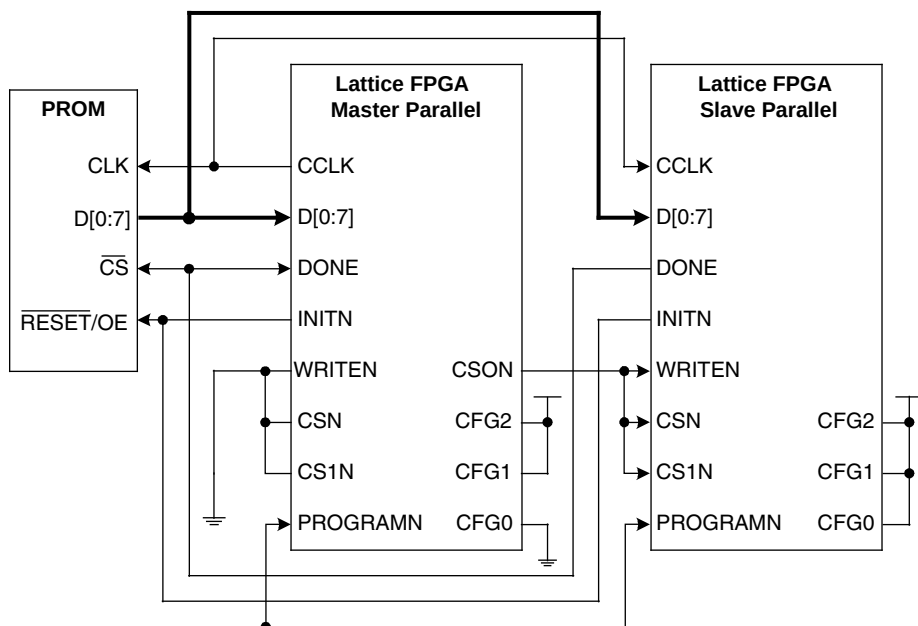
Mode	CFG[2]	CFG[1]	CFG[0]	CONFIG_MODE Parameter
Master Parallel (no overflow option)	1	1	0	MASTER_PARALLEL
Master Parallel (Bypass ON)	1	1	0	MASTER_PARALLEL_BYPASS
Master Parallel (Flow Through ON)	1	1	0	MASTER_PARALLEL_FLOWTHR

Configuration using Master Parallel Mode is used to work together with a parallel port PROM without additional external logic. When Master Parallel Mode is chosen, the device will generate CCLK as specified by the MCLK_FREQ preference. The CCLK signal is used to provide a programming clock to the PROM and slave devices. Data is transferred byte wide to the D[0:7] pins. The WRITEN pin must be held low to write to the device. If an overflow option is not selected, the CSN and CS1N pins must be driven low to enable configuration and read back.

The Master Parallel Mode can support two types of overflow, Bypass and Flow Through. If the Bypass option is set, the data presented to the D[0:7] pins will be serialized and bypassed to the DOUT pin when the configuration is complete. If the Flow Through option is set, upon completion of the configuration, the CSOUT signal will drive the following Parallel Mode device chip select as shown in Figure 13-6.

If either overflow option is selected, the CSN or CS1N pins can be toggled to reset the Master Parallel device out of the Overflow option, otherwise both chip select pins should be held low to keep the device active for configuration.

Figure 13-6. Master and Slave Parallel Daisy Chain



Slave Parallel Mode

Mode	CFG[2]	CFG[1]	CFG[0]	CONFIG_MODE Parameter
Slave Parallel (no overflow option)	1	1	1	SLAVE_PARALLEL
Slave Parallel (Bypass ON)	1	1	1	SLAVE_PARALLEL_BYPASS
Slave Parallel (Flow Through ON)	1	1	1	SLAVE_PARALLEL_FLOWTHR

In Slave Parallel Mode, a host system sends the configuration data in a byte wide stream to the device. The CCLK, CSN, CS1N and the WRITEN signal are provided by the host system such as a Master Parallel mode device as shown in Figure 13-6.

The Slave Parallel configuration mode allows multiple devices to be chained in parallel.

To support asynchronous configuration, where the host may provide data faster than the FPGA can handle it, the Slave Parallel mode can use the BUSY signal. By driving the BUSY signal high, the Slave Parallel device tells the host to pause sending data.

Figure 13-7. Asynchronous Usage of Slave Parallel Configuration Mode

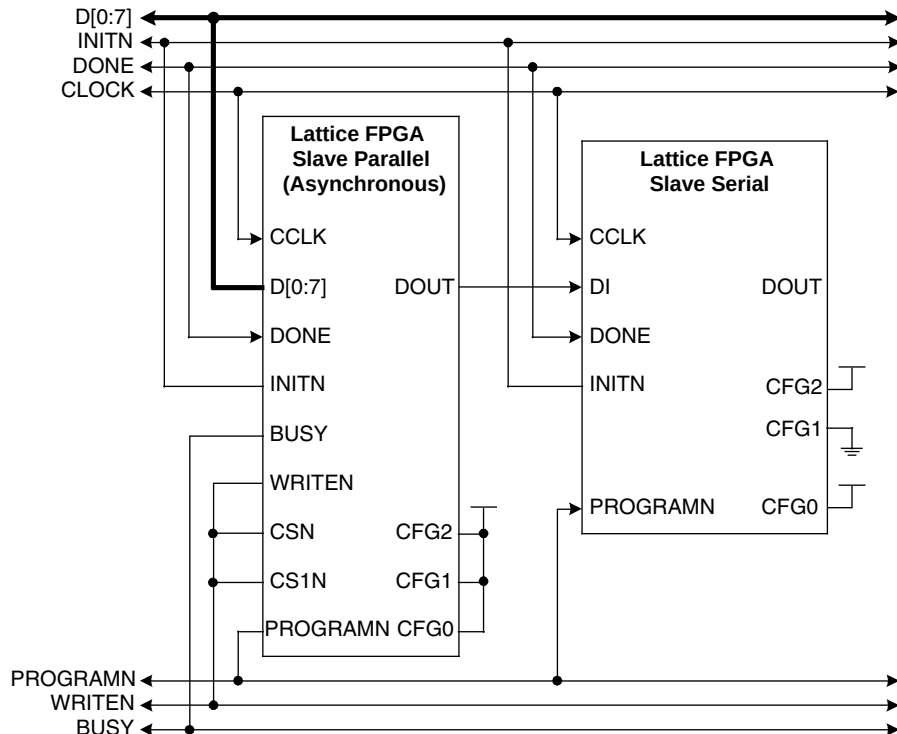


Figure 13-7 shows the Asynchronous peripheral write sequence using the Bypass option. To send configuration data to a device, the WRITEN signal has to be asserted. During the write cycle, the BUSY signal provides hand-shaking between the host system and the LatticeECP/EC device. When the BUSY signal is low, the device is ready to read a byte of data at the next rising edge of CCLK. The BUSY signal is set high when the device reads the data and the device requires extra clock cycles to process the data.

The CSN or CS1N signals can be used to temporarily stop the write process by setting either to a high state if the host system is busy. The LatticeECP/EC device will resume the configuration when the both CSN and CS1N signals are set low again.

ispJTAG Mode

Mode	CFG[2]	CFG[1]	CFG[0]	CONFIG_MODE Parameter
ispJTAG (1149.1 interface)	X	X	X	Any CONFIG_MODE or NONE1

The LatticeECP/EC device can be configured through the ispJTAG port. The JTAG port is always on and available, regardless of the configuration mode selected. The NONE mode (1) can be selected in the Lattice design software to say that the JTAG port will be used exclusively, but is not required.

ISC 1532

Configuration through the JTAG port conforms to the IEEE 1532 Standard. The Boundary Scan cells take control of the I/Os during any 1532 mode instruction. The Boundary Scan cells can be set to a pre-determined values whenever using the JTAG 1532 mode. Once configuration is complete, an internal Done bit is set, which will release the DONE pin.

Transparent Read Back

The ispJTAG transparent read back mode allows the user to read the content of the device while the device remains in a functional state. The I/O and non-JTAG configuration pins remain active during a Transparent Read Back. The device will enter the Transparent Read Back mode through a JTAG instruction. The user must ensure

that User Mode read/write operations from/to the EBR and distributed RAM do not interfere with the transparent read back.

Boundary Scan and BSDL Files

The LatticeECP/EC BSDL files can be found on the Lattice Semiconductor web site. The boundary scan ring will cover all the I/O pins, dedicated and dual-purpose sysCONFIG pins. The sysCONFIG pins can be observed using the Boundary Scan.

Configuration Flow

The writing to the configuration SRAM memory can generally be split into three phases.

1. **Clear the configuration memory.**

After power-up or toggling the PROGRAMN pin low, the configuration memory is cleared automatically. The INITN pin is driven high by the EC/ECP device when the device has finished clearing the configuration memory and Done bit. The INITN pin can also be driven externally by the user to delay the configuration process.

2. **Load configuration data into the memory.**

Loading the bit stream from DI or D[0:7], depending on the selected configuration mode. The INITN pin is set to low on any error and BUSY can be used to delay configuration

3. **Wake up the device.**

The Wake-up sequence puts the device into functional mode after full configuration. Choosing a proper Wake-up sequence is important, to prevent contention.

The following sections describe the three steps to configure LatticeECP/EC devices.

Clearing the Configuration Memory

Two possible methods can clear the internal configuration memory of the LatticeECP/EC device. The first is when the device powers up, the second is by toggling the PROGRAMN pin.

Power-up Sequence

On power-up the device tri-states all the I/Os, sets them to LVCMOS type, and sets the INITN and DONE pin to low. The device prepares for configuration by resetting the configuration circuitry, clearing the DONE bit and CRC registers. The device clears the configuration memory, including I/O options such as PCI clamp, and gets ready to start configuration. The JTAG port is ready to be used as soon as the device clears the configuration memory.

After the device clears the POR, the device samples the Configuration Mode pins CFG[0:2] and recovers the relevant configuration pins according to the Configuration Mode pin settings. The device will then release the INITN pin if the PROGRAMN pin is high. If a Master Mode is selected, the device starts driving the master clock out of the CCLK pin. The INITN pin can be driven low externally to delay device configuration. Once the INITN pin goes high, the device is ready for configuration to start.

Toggling the PROGRAMN Pin

After a device is powered up, toggling the PROGRAMN pin will initiate a sequence to prepare the LatticeECP/EC device for re-configuration from an external memory source. Upon driving the PROGRAMN pin low, the INITN and DONE pins will drive low, the memory will start clearing, and the I/O pins will become tri-stated and pulled up to V_{CCIO} .

Upon driving the PROGRAMN pin high, the CFG[0:2] are sampled to determine the configuration mode to implement as well as which configuration pins will be used for configuration. If a master mode is selected, CCLK will be driven. The INITN pin will be released once the configuration memory is cleared and the PROGRAMN pin is driven high. Holding the INITN pin low will delay configuration. Configuration will begin as soon as the INITN pin is released and pulled high.

Loading the Configuration Memory

Once the PROGRAMN and INITN pins are high, configuration can begin. Depending on the configuration mode selected, data will be accepted on either the DI or D[0:7] pins on the rising edge of CCLK. If an error occurs at any time during transfer of the data, the INITN pin will be driven low by the LatticeECP/EC device. For handshaking configurations, the CSN or CS1N pin can be driven high to pause configuration and stop the Master clock. The BUSY pin can be used by the LatticeECP/EC device to pause the configuration host EC/ECP. Once the full data stream has been shifted in a CRC calculation done during configuration will be compared to the bit stream CRC. If they match, the device will either proceed to the Wake-up sequence or overflow the next data to the next device. If the CRC does not match, then the INITN pin will be driven low and the device will remain in configuration mode.

Wake Up the Device

When configuration is complete, the device will wake up in a predictable fashion. The following selections determine how the device will wake up. Two synchronous wake-up processes are available. One automatically wakes the device up when the internal Done Bit is set even if the DONE pin is held low externally. The other waits for the DONE pin to be driven high externally before starting the wake-up process. The DONE_EX preference determines if the synchronous wake up will be controlled by the external driving of the DONE pin or ignores the external driving of the DONE pin. Table 13-3 provides a list of the wake-up sequences supported by the devices.

Table 13-3. Wake-up Sequences supported by LatticeEC

Sequence	Phase T0	Phase T1	Phase T2	Phase T3
Default		GOE	GSR, GWDIS	DONE
1	DONE	GOE, GWDIS, GSR		
2	DONE		GOE, GWDIS, GSR	
3	DONE			GOE, GWDIS, GSR
4	DONE	GOE	GWDIS, GSR	
5	DONE	GOE		GWDIS, GSR
6	DONE	GOE	GWDIS	GSR
7	DONE	GOE	GSR	GWDIS
8		DONE	GOE, GWDIS, GSR	
9		DONE		GOE, GWDIS, GSR
10		DONE	GWDIS, GSR	GOE
11		DONE	GOE	GWDIS, GSR
12			DONE	GOE, GWDIS, GSR
13		GOE, GWDIS, GSR	DONE	
14		GOE	DONE	GWDIS, GSR
15		GOE, GWDIS	DONE	GSR
16		GWDIS	DONE	GOE, GSR
17		GWDIS, GSR	DONE	GOE
18		GOE, GSR	DONE	GWDIS
19			GOE, GWDIS, GSR	DONE
20		GOE, GWDIS, GSR		DONE
21 (Default)		GOE	GWDIS, GSR	DONE
22		GOE, GWDIS	GSR	DONE
23		GWDIS	GOE, GSR	DONE
24		GWDIS, GSR	GOE	DONE
25		GOE, GSR	GWDIS	DONE

Synchronous to Internal Done Bit

If the LatticeECP/EC device is the only device in the chain, or the last device in a chain, the wake-up process should be initiated by the completion of the configuration. Once the configuration is complete the internal Done Bit will be set and the wake-up process will begin.

Synchronous to External DONE Signal

The DONE Pin can be selected to delay wake up. If DONE_EX is true the wake-up sequence will be delayed until the DONE pin is driven high externally, then the device will follow the selected wake-up sequence.

Wake-up Clock Selection

The wake-up sequence is synchronized to a clock source, the user can select the clock source for wake up. The clock sources are CCLK, TCK and User Clock. The default clock is TCK if using ispJTAG, and CCLK if using sysCONFIG. The User Clock is chosen at the time of design. The user can select any of the CLK pins of the device or a net (routing node) as the User Clock source. The WAKEUP_CLK shall default to CCLK or TCK.

Read Back

Read Sequence

To read the configuration memory data or register contents back, WRITEN is first set to low to send the read instruction into the device. The device will read in the command from the host and execute the command once read in. If the LatticeECP/EC device cannot have the data ready by the next clock cycle, it will drive the BUSY pin high. When BUSY is high, the device will continue to execute the command regardless of the state of the CSN or CS1N pins. The device will drive the BUSY pin low when the data is ready but will not drive the D[0:7] until the CSN and CS1N pins are pulled low by the host. The WRITEN pin should be pulled high after sending in the command. The CSN, CS1N and WRITEN signals are latched and the device will switch to read mode on the rising edge of CCLK. If the LatticeECP/EC device needs more than one clock cycle to switch the bus around, BUSY will be kept high until the D[0:7] is ready.

As in the Write sequence, CSN and CS1N signals can be used to temporarily pause the read sequence in case the host system is busy. The data is read at the next rising CCLK edge, after CSN and CS1N pins are set to low and the BUSY pin is low.

Transparent Read Back

Using the Slave Parallel Mode for read back, the user I/Os will remain functional. The Slave Parallel port pins must be retained in order to allow read back by setting the PERSISTENT preference to ON. CCLK becomes input only. The user must ensure that User Mode read/write operations from/to the EBR and distributed RAM do not interfere with the transparent read back.

Configuration Mode Read Back

Read back can also be done with the LatticeECP/EC device in configuration mode. Only the Slave Parallel Mode is supported for configuration read back. By driving the WRITEN pin high, the Slave Parallel port will watch for the read back request from the host device.

Software Control

In order to control the configuration of the LatticeECP/EC device beyond the default settings, software preferences can be used. Table 13-4 is a list of the preference, the default settings and the section more information about the preference can be found.

Table 13-4. LatticeECP/EC Device Preference List

Preference (Preference)	Default Setting (All Settings)
PERSISTENT	ON [off, on]
CONFIG_MODE	SLAVE_SERIAL (see Table 13-2)
DONE_OD	ON [on, off]
DONE_EX	OFF [off, on]
MCCLK_FREQ	Lowest Frequency (see device tables)
CONFIG_SECURE	OFF [off, on]
WAKE_UP	21 (DONE_EX = Off) [1:25] 4 (DONE_EX = On) [1:7]
COMPRESS_CONFIG	OFF (off, on)

Persistent

When using the sysCONFIG port to perform transparent readback the PERSISTENT preference must be set to ON, this reserves the dual-purpose pins for configuration. PERSISTENT = ON prevents the user and the software fitter from using any of the dual-purpose pins as general purpose I/O.

Configuration Mode

The device knows which physical port will be used by reading the highs and lows wired to the CFG[0:2] pins, however sometimes software needs to know the setting of the CFG pins as well. The Configuration Mode serves this purpose. The fitter will be prevented from using the I/O pins associated with the selected Configuration Mode, however the user may assign these pins (a warning will be generated by the software). If the user requires these pins as general purpose I/O they must adhere to the requirements listed above in the Configuration Pins section.

Normally, proper selection of the Configuration Mode is not strictly required. For pin reservation, for instance, the user can place prohibits in the source code to insure that the fitter doesn't use the configuration pins as general purpose I/O. However, if multiple devices are being configured from one configuration device then the Configuration Mode must match the CFG pins. This is required because the overflow option (Flow Through or Bypass) is determined by the Configuration Mode (in software) and the CFG pins (in hardware). Note that if either overflow option is selected, then the DONE_EX and WAKE_UP selections will be changed to correspond. See Table 13-5 for details on the Overflow Option defaults. For more information on the overflow options, see the Configuration Options section of this document.

Table 13-5. Overflow Option Defaults

Overflow Option (Bypass, Flow Through)	DONE_EX Preference	WAKE_UP Preference
Off	Off (default)	Default 21 (user selectable 1 through 25)
Off	On	Default 21 (user selectable 1 through 25)
On	ON (automatically set by software)	Default 4 (user selectable 1 through 7)

DONE Open Drain

The "DONE_OD" preference allows the user to configure the DONE pin as an open drain pin. The "DONE_OD" preference is only used for the DONE pin. When the DONE pin is driven low, internally or externally, this indicates that programming is not complete and the device is not ready for wake up. Once configuration is complete, with no errors, and the device is ready for wake-up, the DONE pin must be driven high. For other devices to be used to control the wake-up process an open drain configuration is needed to avoid contention on the DONE pin. The "DONE_OD" preference for the DONE pin defaults to ON. The DONE_OD preference will be automatically set to the default if the DONE_EX preference is set to on. See Table 13-6 for more information on the relationship between DONE_OD and DONE_EX.

DONE External

The LatticeECP/EC device can wake up on its own after the Done Bit is set or wait for the DONE pin to be driven externally. The DONE_EX preference will determine if the wake-up sequence is triggered by an external DONE signal. The DONE_EX preference shall take a user entered ON or OFF. ON if the user wants to delay wake-up until the DONE pin is driven high by an external signal and synchronous to the clock. The user will select OFF to synchronously wake up when the internal Done bit is set and ignore any external driving of the DONE Pin. The default for DONE_EX preference is OFF. If DONE_EX is set to ON, DONE_OD should be set to the default value of ON. If an external signal is driving the DONE pin, it should be an open drain pin. See Table 13-6 for more information on the relationship between DONE_OD and DONE_EX.

Table 13-6. Summary of DONE Pin Preferences (Preferences)

DONE_EX	Wake-up Process	DONE_OD
OFF	External DONE ignored	User selected
ON	External DONE Low delays	Set to Default (ON)

Master Clock Selection

When the user has determined that the LatticeECP/EC device will be a Master Configuration device and will provide the clocking source for configuration, the CCLK will become an output clock with the frequency set by the user. At the start of configuration the device operates with the default Master Clock Frequency of 2.5MHz. One of the first configuration bits set will be the Master Clock. Once the Master Clock configuration bits are set, the clock will start operating at the user-defined frequency.

In order to control the Master Clock frequency, the MCCLK_FREQ preference can be set. The MCCLK_FREQ preference shall set the frequency of the MASTER clock if selected by the CONFIG_MODE and the CFG[0:2] pins. See the LatticeECP/EC data sheet for the Master Clock frequencies supported by the MCLK_FREQ preference.

Security

When CONFIG_SECURE is set to ON, NO read back operation will be supported through the sysCONFIG port or ispJTAG port of the configuration SRAM. The USERCODE register is readable and not considered securable. Default is OFF. OFF indicates read back of the configuration memory is enabled through all ports.

Wake-up Sequence

The wake-up sequence controls three internal signals and the DONE pin will be driven post configuration and prior to user mode. See the Wake-up Sequence section of this document for an example of the phase controls and the device-specific section for specific info on the wake-up selections. The default setting for the WAKE_UP preference will be determined by the DONE_EX setting.

Wake-up with DONE_EX = Off (Default setting)

The WAKE_UP preference will support the user-selectable options (1-25) as shown in Table 13-3. If the user does not select a wake-up sequence, the default will be wake-up sequence 21 for DONE_EX preference set to OFF (Default).

Wake-up with DONE_EX = On

The WAKE_UP preference will take the user selectable options (1-7) as shown in Table 13-3. If the user does not select a wake-up sequence, the default will be wake-up sequence 4 for the DONE_EX preference set to ON.

Start-Up Clock Selection

Once the FPGA is configured, it enters the start-up state, which is the transition between the configuration and operational states. This sequence is synchronized to a clock source, which defaults to CCLK when sysCONFIG is used, or TCK when JTAG is used.

If desired, a user-defined clock source can be used instead of CCLK/TCK. You need to specify this clock signal, and instantiate the STRTUP library element in your design. The example shown below shows the proper syntax of instantiating the STRTUP library element.

Verilog

```
STRTUP u1 (.UCLK(<clock_name>)) /* synthesis syn_noprune=1 */;
```

VHDL

```
component STRTUP
  port(STRTUP: in STD_ULOGIC );
end component;

attribute syn_noprune: boolean ;
attribute syn_noprune of STRTUP: component is true;
begin
  u1: STRTUP port map (UCLK =><clock name>);
```

Bit Stream Compression

The LatticeECP/EC devices support bit stream compression. When the Compression preference is set to ON, the Lattice design software will generate a compressed version of the bit stream file internally along with an uncompressed bit stream file. The LatticeECP/EC devices will route the compressed bit stream through the decompression engine when the COMPRESS_CONFIG preference is set to ON. The COMPRESS_CONFIG preference defaults to OFF. It is possible for the compressed bit stream to be larger than the uncompressed bit stream.

Table 13-7. LatticeECP/EC Configuration Memory Requirements

Family	Device	Max. Config. Bits (Mb)	Required Boot Memory (Mb)	
			Without Compression	Typical Compression
LatticeECP/EC	EC1	0.6	1	25%
	EC3	1.1	2	25%
	ECP/EC6	1.8	2	25%
	ECP/EC10	3.1	4	25%
	ECP/EC15	4.3	8	25%
	ECP/EC20	5.3	8	25%
	ECP/EC33	7.9	8	25%

SPI Compatible SPI Flash Vendors

- ST Microelectronics - M25Pxx
- Winbond - W25Pxx
- Silicon Storage Technology - SST25VFxx
- Spansion - S25FLxx
- PMC pFLASH - Pm25LVxx
- Atmel - AT25Fxx

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
 +1-503-268-8001 (Outside North America)
 e-mail: techsupport@latticesemi.com
 Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
June 2004	01.0	Initial release.
July 2004	1.1	Changed DO/CSON to DOUT/CSON.
		Clarified signal names associated with data pins during SPI and other modes.
		Indicated value for INITN pull up resistor in "Master and Slave Serial Daisy Chained" diagram
		Added section detailing compatible SPI flash vendors.
October 2004	1.2	Update table 6-7 for formatting and compression %.
May 2005	2.0	Changed SPI3 to SPI
		Updated INITN description to include the power cycling instruction for SPI mode
		Updated CCLK to include toggling the CCLK continuously throughout configuration and error recovery
		Updated dual-purpose use pin
		Updated Master Parallel Mode
October 2005	2.1	Added information on how to use the sysCONFIG dual-purpose pins as GPIO
April 2006	2.2	Updated Wake-Up Options
July 2008	2.3	Updated LatticeECP/EC Device Preference List table.
		Replaced Wake-up Clock Selection text section with new Start_Up Clock Selection text section.
September 2008	02.4	Updated CCLK text section.
September 2012	02.5	Updated document with new corporate logo.