MACH f_{MAX} Theory and Calculations

February 2002

Introduction

The f_{MAX} parameter is the maximum clock rate at which a device is guaranteed to operate. f_{MAX} is commonly referred to as the maximum operating frequency and can be thought of as the longest register-to-register time in a design. Due to the inherent flexibility of programmable logic devices, the maximum operating frequency calculation can vary. There are four different ways to calculate f_{MAX} in a design. In the discussion that follows, each one of the basic f_{MAX} calculations is examined, including a general description of the f_{MAX} design type and a detailed discussion of the f_{MAX} calculation.

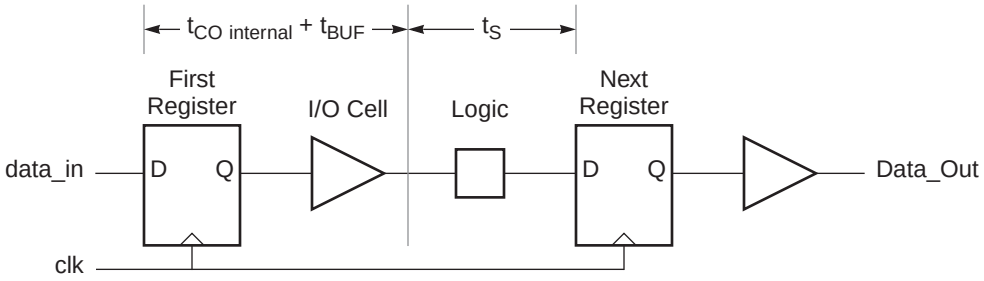
f_{MAX} Design Types

Type 1: External Feedback Timing Path

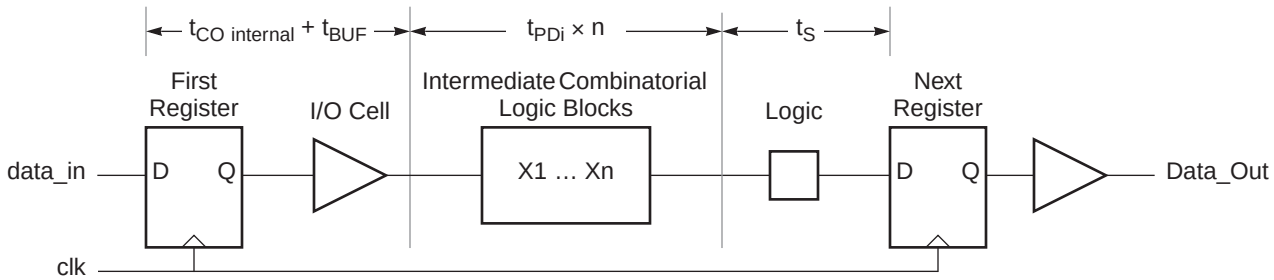
The first type of f_{MAX} design involves a signal path between two registers that is sent through the I/O cell and fed back into a register inside the part (or fed into a register on another chip). Figure 1a represents the MACH® device specification for f_{MAX} using an external data path. The period of the external feedback timing path is the sum of the setup time and the global clock to external output time. The reciprocal of this time is f_{MAX} and is calculated as:

$$f_{MAX(External)} = \frac{1}{t_{COi} + t_{BUF} + t_S}$$

where t_S is the setup time, t_{COi} is the clock-to-feedback time for the flip flop, and t_{BUF} is the time from feedback through the I/O cell.



a. MACH Device f_{MAX} using an external feedback timing path



b. f_{MAX} for a MACH design using an external feedback timing path and n number of intermediate combinatorial logic blocks

Figure 1. External Feedback Timing Path

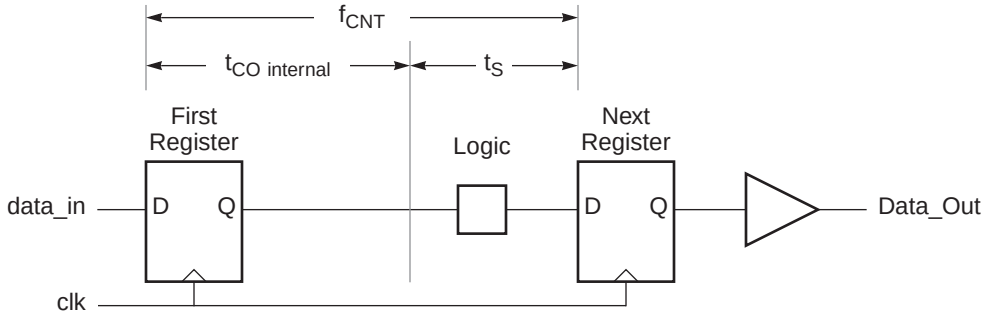
Figure 1b represents a typical design scenario involving an external feedback timing path and demonstrates how f_{MAX} is calculated in a design using intermediate combinatorial logic blocks. In Figure 1b, some intermediate combinatorial logic has been internally added between the registers. The addition of the intermediate logic causes the signal path to slow down by a factor of ($t_{PDi} \times n$), where n represents the number of combinatorial logic blocks between two registers. In this case, a combinatorial logic block is made up of all the product terms going through the logic array and macrocell only once. In the Figure 1b case, the longest timing path is the sum of the clock-to-output time of the register, delay through the I/O buffer, combinatorial propagation time, and the setup time. f_{MAX} is calculated by inverting the longest timing and becomes:

$$f_{MAX} = \frac{1}{t_{COi} + t_{BUF} + t_S + (t_{PDi} \times n)}$$

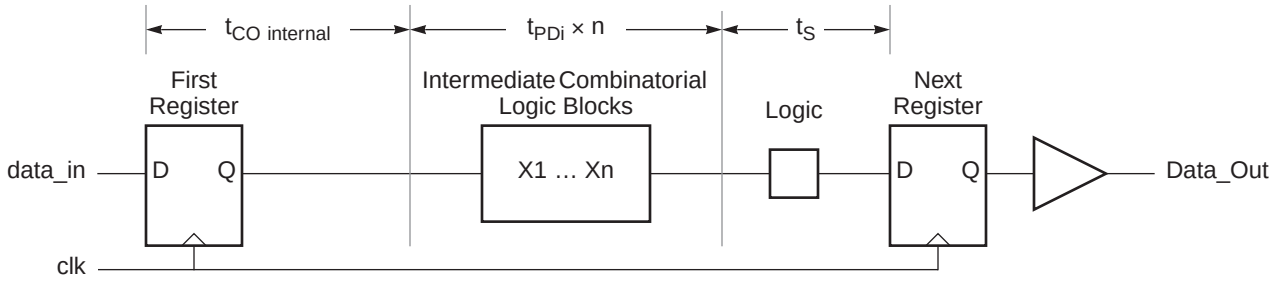
Type 2: Internal Feedback Path

In the second design, f_{MAX} is calculated for timing paths that use internal feedback. These paths do not go through the output buffer, but rather, they leave the macrocell and are sent back directly into the input or central switch matrix. In the case of internal feedback signals, f_{MAX} is calculated by using the t_{COi} timing parameter without t_{BUF}. In the circuit shown in Figure 2a, f_{MAX} is equal to f_{CNT}. The f_{CNT} parameter of Figure 2a is:

$$f_{MAX(Internal)} = \frac{1}{t_{COi} + t_S}$$



a. MACH device f_{MAX} using an internal feedback timing path



b. f_{MAX} for a MACH design using an internal feedback timing path and n number of intermediate combinatorial logic blocks

Figure 2. Internal Feedback Timing Path

The design in Figure 2b is similar to Figure 1b in that intermediate, combinatorial logic blocks have been added between registers and consequently, f_{MAX} does not equal f_{CNT}. The difference is that the feedback for the timing path is internal and does not include t_{BUF}. In Figure 2b, f_{MAX} is calculated as:

$$f_{MAX} = \frac{1}{t_{COi} + t_S + (t_{PDi} \times n)}$$

Type 3: Registered Data Path with No Feedback

The third way f_{MAX} is calculated involves circuits using no feedback data paths. Figure 3 is an example of a design involving one register and no feedback data path. In this case, the input data is presented to the flip-flop and clocked through. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). This means that the clock period must be greater than or equal to the sum of the data setup and data hold times (clock period ≥ $t_S + t_H$). In this instance, the maximum clock frequency, f_{MAX}, is determined by the duty cycle requirements for the clock (t_{WL} and t_{WH}). Therefore, the slowest time that the data path of Figure 3 can take is the clock period, and as a result, f_{MAX} is calculated as:

$$f_{MAX(\text{No Feedback})} = \frac{1}{t_{WL} + t_{WH}}$$

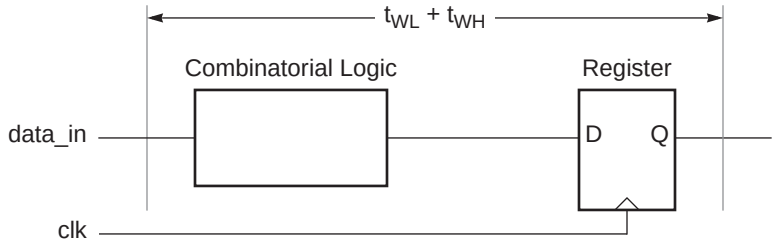


Figure 3. Registered Data Path with No Feedback

Type 4: Input Registered Data Path with No Feedback

The final f_{MAX} is calculated from a design using an input register. This is very similar to the previous type of f_{MAX} calculation. The minimum period will again be limited by the sum of the clock widths, which is $t_{WIRL} + t_{WIRH}$. In this situation, f_{MAX} is calculated as:

$$f_{MAX(IR)} = \frac{1}{t_{WIRL} + t_{WIRH}}$$

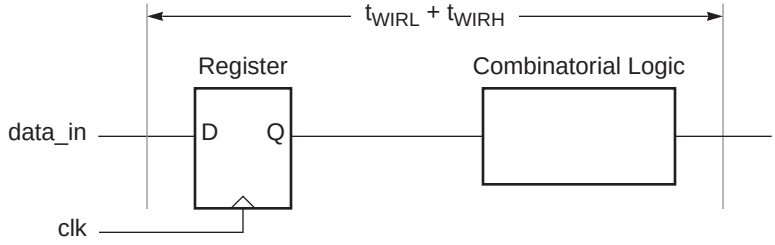


Figure 4. Input Registered Data Path with No Feedback