ispLSI® 5384VE Application: High Speed Binary Counters

Introduction

Counters are sequential logic circuits that proceed through a well-defined sequence of states. There are counters available today as standard products, such as 2-bit, 4-bit, 8-bit, 16-bit and larger. The different types of counters available are the binary, decade and gray, which are synchronously designed. Ripple and cascade counters are asynchronous. These standard products might not be able to meet the system requirements or the operating conditions set by the designer. Implementing the counter in a Lattice CPLD enables system designers to achieve different system-specific features and operating conditions such as speed.

Overview

This application note describes three 32-bit binary counters. The first design is a free running binary counter; the second a loadable counter; and the third a loadable UP/DOWN counter. These three applications take advantage of the wide inputs of the ispLSI 5000V Family architecture. The free running counter is implemented with a count enable and an asynchronous reset. The loadable counter has a data load, count enable, and an asynchronous reset. The UP/DOWN counter is designed with an asynchronous clear, synchronous clear, enable, parallel data load, synchronous preset carry-in, and carry-out.

The first two binary counters are implemented behaviorally using VHDL. The UP/DOWN counter is implemented in a schematic to show the flexibility of different design entries. This schematic implementation was done by instantiating four 8-bit UP/DOWN counters. The application is implemented in the Lattice ispLSI 5384VE-165LB388 device, which is part of the ispLSI 5000VE Family.

ispLSI 5384VE-125LB388

The ispLSI 5384VE has 18,000 gates with 384 macrocells. It has 12 Generic Logic Blocks (GLBs) connected by the Global Routing Pool (GRP) with 165 product terms (PTs). Each GLB has 32 logic macrocells with dual output functions, which can be both registered and combinatorial. The registers can be configured as a D, T or as a latch. There are 35 PTs per macrocell from the product term sharing array (PTSA), five dedicated for that macrocell and the rest from the three nearest neighbors above and below. The 5PT-bypass path can be used to bypass the PTSA. Each GLB also has 68 inputs fed from the GRP to drive the 165 PTs and each PT has all 68 inputs. There are five control signals out of the 165 PT's which are for extra control. There is a reset and a preset which can be global or PT for the GLBs. There are six global PT output enables in a macrocell. The 'tpd' of the device is 6.0ns and the maximum operating frequency is 165MHz. The open drain, slow slew, and pull up options are available in the device. It also supports JTAG programming. For more details, refer to the ispLSI 5384VE Data Sheet in the Lattice Semiconductor Data Book or CD-ROM.

Implementation

The three counters are implemented in the ispLSI 5384VE-125 device by exploiting the wide inputs of the 5000V architecture. The counters have an asynchronous reset that gets priority in all applications by resetting the output to logic '0'. To implement the clock enable as a count enable, the count enable gets priority over load. The count of the loadable UP/DOWN binary counter (refer to Figure 1) depends on the count enable, carry-in and the up/down (DNUP) signal. The asynchronous clear (CD) sets the output (Q) to '0' and the synchronous preset (PS) will set the 'Q' to '1' at the rising edge of the global clock signal (CLK). The synchronous clear (CS) will set 'Q' back to '0' at the rising edge of the 'CLK'. Data (D) is loaded when the load (LD) is set to high. After the data is loaded, and depending upon the enable (EN), carry in (CAI), and down up (DNUP) signals the counter counts UP or DOWN. When 'EN', 'CAI' and 'DNUP' are high, the counter starts counting UP at the rising edge of the 'CLK'. When 'DNUP' is low, it starts counting DOWN at the rising edge of the 'CLK'. The CAO is a combinatorial output of 'EN' and 'CAI' and 'DNUP' depending on the state of count. The free running counter and the loadable counter implementation is similar to the loadable UP/DOWN counter. The truth table for the UP/DOWN counter is shown in Table 1.

Figure 1. 1-Bit Loadable UP/DOWN Counter with Carry-In and Carry-Out

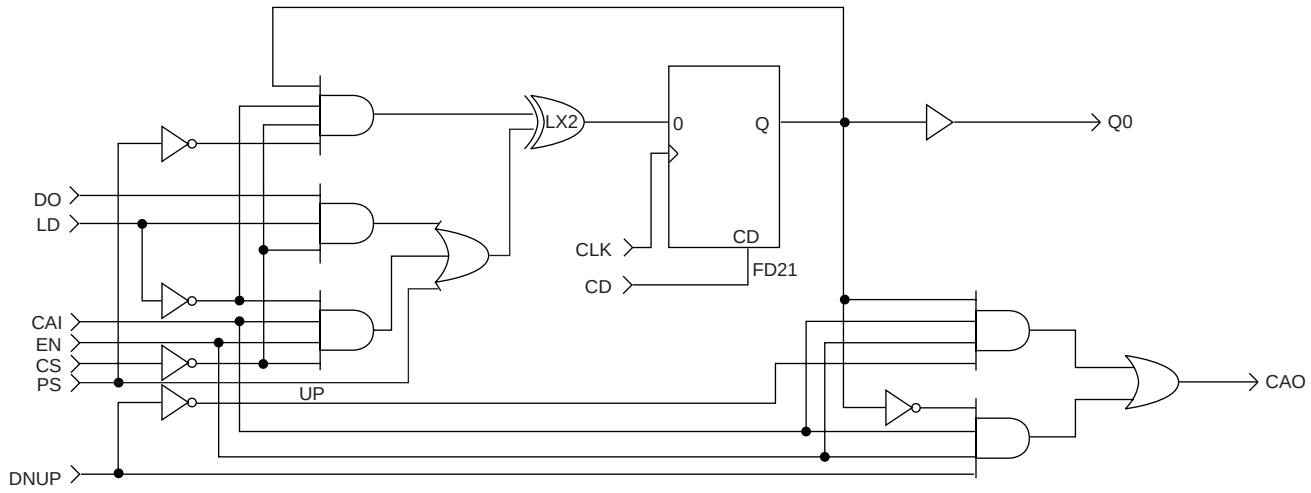

Table 1. UP/DOWN Counter Truth Table

INPUTS									OUTPUTS	
CD	**PS**	**CS**	**LD**	**D**	**EN**	**CI**	**DP**	**CK**	**Q**	**CO**
1	X	X	X	X	X	X	X	X	0	*
0	1	X	X	X	X	X	X	!	1	!*
0	0	1	X	X	X	X	X	!	0	*
0	0	0	1	d	X	X	X	!	D	C
0	0	0	0	X	0	X	X	X	Q	0
0	0	0	0	X	X	0	X	!	Q	0
0	0	0	0	X	1	1	0	!	UP	*1
0	0	0	0	X	1	1	1	!	DN	*1

X Don't Care
! Rising Edge of Clock
* CAO = CAI * EN * DNUP
C CAO = Combinatorial Output
!* CAO = CAI * EN * !DNUP
*1 CAO = 1, After Terminal Count
UP Count Up
DN Count Down

Results and Competitive Analysis

The results for all the three counters are provided in Table 2.

The same challanges associated with implementing a 32-bit Loadable counter with count enable and asynchronous clear in a Lattice ispLSI 5384VE are also true for an Altera EPM7384AEFC256-7. The Altera device has 384 logic cells and is a part of the 7000AE family. The results from the MAX+PLUS II Fitter version 9.01 are provided in Table 3.

The results in Table 3 show that the loadable 32-bit counter can be implemented more efficiently in the Lattice ispLSI 5000VE device than the Altera 7000AE device.

Conclusion

Lattice's innovative and superior ispLSI 5000V architecture with world's widest AND array can handle up to 68 input wide functions; no competitor's CPLD comes close.

The Lattice 5384VE device requires only one level of logic to implement the 32-bit loadable counter with an operating frequency of 123 MHz. The Altera 7384AE device requires more than one level of logic to implement the same function with an operating frequency of only 46.08 MHz. The Lattice ispLSI 5384VA can achieve a performance of 2.5 times over the Altera 7384AE. This result cleary indicates that the Lattice 5000V architecture is more efficient and suitable to implement wide input synchronous functions than the Altera 7000AE devices.

Technical Support Assistance

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Table 2. Post-Route Design Implementation Results

Parameter	Free Running 32-Bit Counter	Loadable 32-Bit UP/DOWN Counter	Loadable 32-Bit Counter
Number of Macrocells	32	33	32
Number of GLB Levels	1	1	1
Clock to Out (tco)	4.0 ns	4.0 ns	4.0 ns
Frequency	123 MHz	123 MHz	123 MHz

Table 3. Results for the Lattice ispLSI 5384V and Altera 7256S

Parameter	Loadable 32-Bit Counter	
	Lattice 5384VA	Altera 7384AE
Number of Macrocells/Logic Cells	32	65
Clock to Out (tco)	4.0 ns	4.5 ns
Frequency	123 MHz	46.08 MHz