ispGDX2 vs. ispGDX Architecture Comparison

July 2002 Technical Note TN1035

Introduction

The ispGDX2™ is the second generation of Lattice's successful ispGDX® platform. Architecture enhancements improve flexibility and integration when implementing a wide range of bus switching applications. Support has been added for tighter integration with common backplane transceiver, memory and other modern I/O standards. Phase-Lock Loop (PLL) capabilities have been added to allow skew adjustment of clock signals. Features including serializer/de-serializer (SERDES), clock data recovery (CDR), and FIFO buffers have also been implemented to benefit high-speed data transfer.

This application note compares the capabilities of the ispGDX2 with the ispGDXV devices and introduces its advanced features aimed at high-speed design. A basic understanding of the ispGDXV architecture is assumed.

ispGDX2 Basic Features

The ispGDX2 device family broadens the feature offerings over the previous generation to target different areas of high-speed system design. These features include changes to the core architecture, routing resources, and I/O features. Table 1 highlights some of the key differences.

Table 1. Key Differences

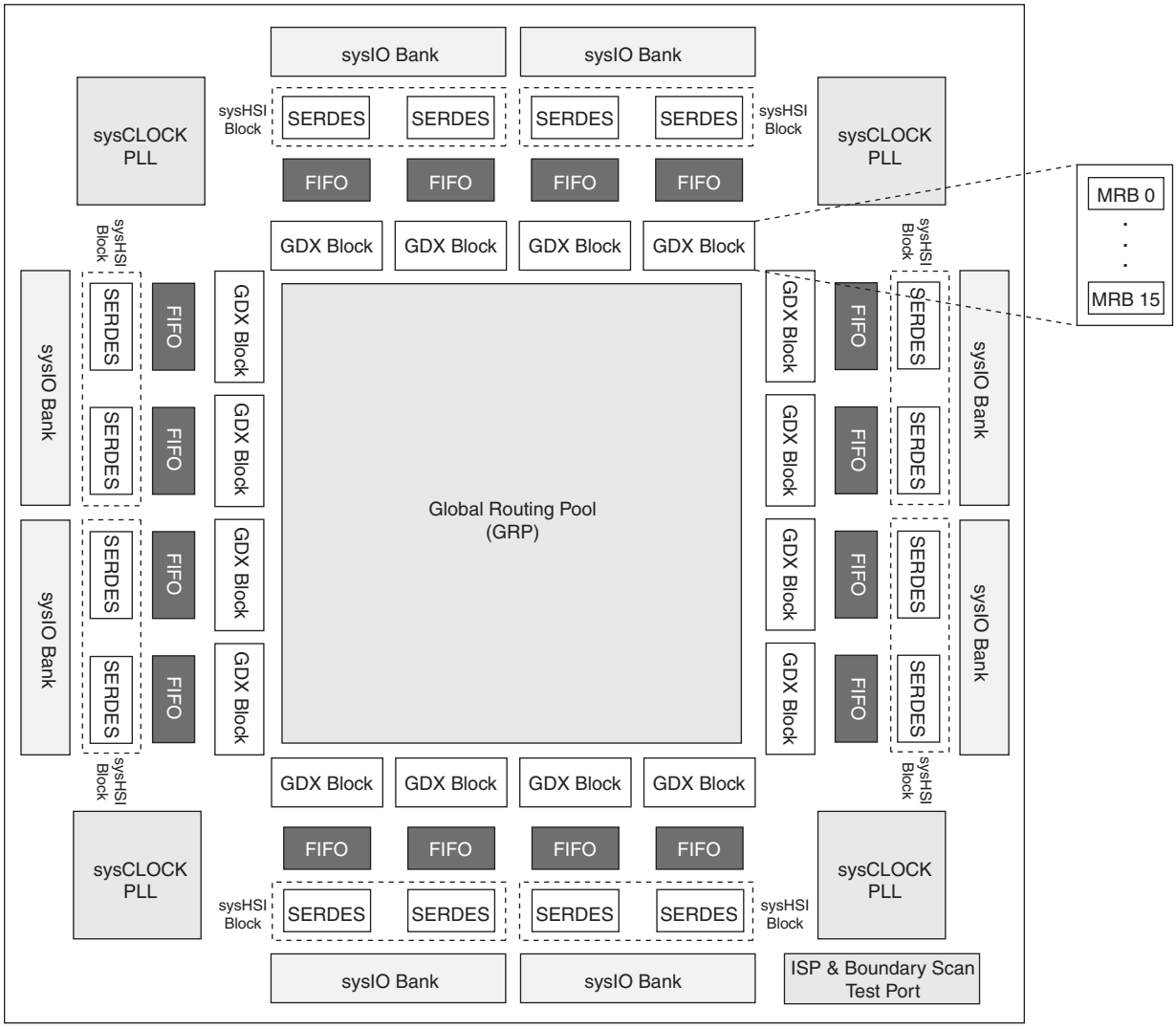
	ispGDX2	ispGDXV
I/Os	64, 128, 256	80, 160, 240
Core Voltage	1.8/2.5/3.3V	3.3V
f_{MAX}	360 MHz	250MHz
t_{PD}	2.5ns	3.5ns
I/O Support	8 sysIO Banks (See Table 2 for supported standards)	LVCMOS 3.3 and 2.5
Registers	Separate input, output and OE registers per I/O	Single register per I/O cell
Control Signals	Can be driven from any I/O pin and/or internal logic	Specific pins with no internal logic
sysHSI™ Blocks (High Speed Serial Inteface)	Up to 8	None
Embedded FIFOs	Up to 16	None
sysCLOCK PLL	2 or 4 per device	None
Programming Interface	IEEE 1532	Lattice ISP/JTAG

Architectural Enhancements

The ispGDX2 architecture is organized in a block-oriented manner which differs from the bit-oriented approach of the ispGDXV. Each ispGDX2 block provides data flow and control logic for 16 I/O buffers. The data flow is organized as four nibbles, with each nibble containing four Multiplexer Register Blocks (MRBs). Input data for the MRBs is provided from the Global Routing Pool (GRP). A block diagram of the ispGDX2 is shown in Figure 1.

By contrast, the ispGDXV family is configured in a bit-oriented structure. Each of the MUX inputs has connectivity to only a quarter of the device I/Os, which constrains the location of inputs. The block-oriented ispGDX2 structure divides the device into 16 I/O cell blocks and further divides this into four sets of 4:1 Muxes. Each block is able to receive 64 signals from any I/O location of the device.

Figure 1. ispGDX2 Block Diagram (256-I/O Device)



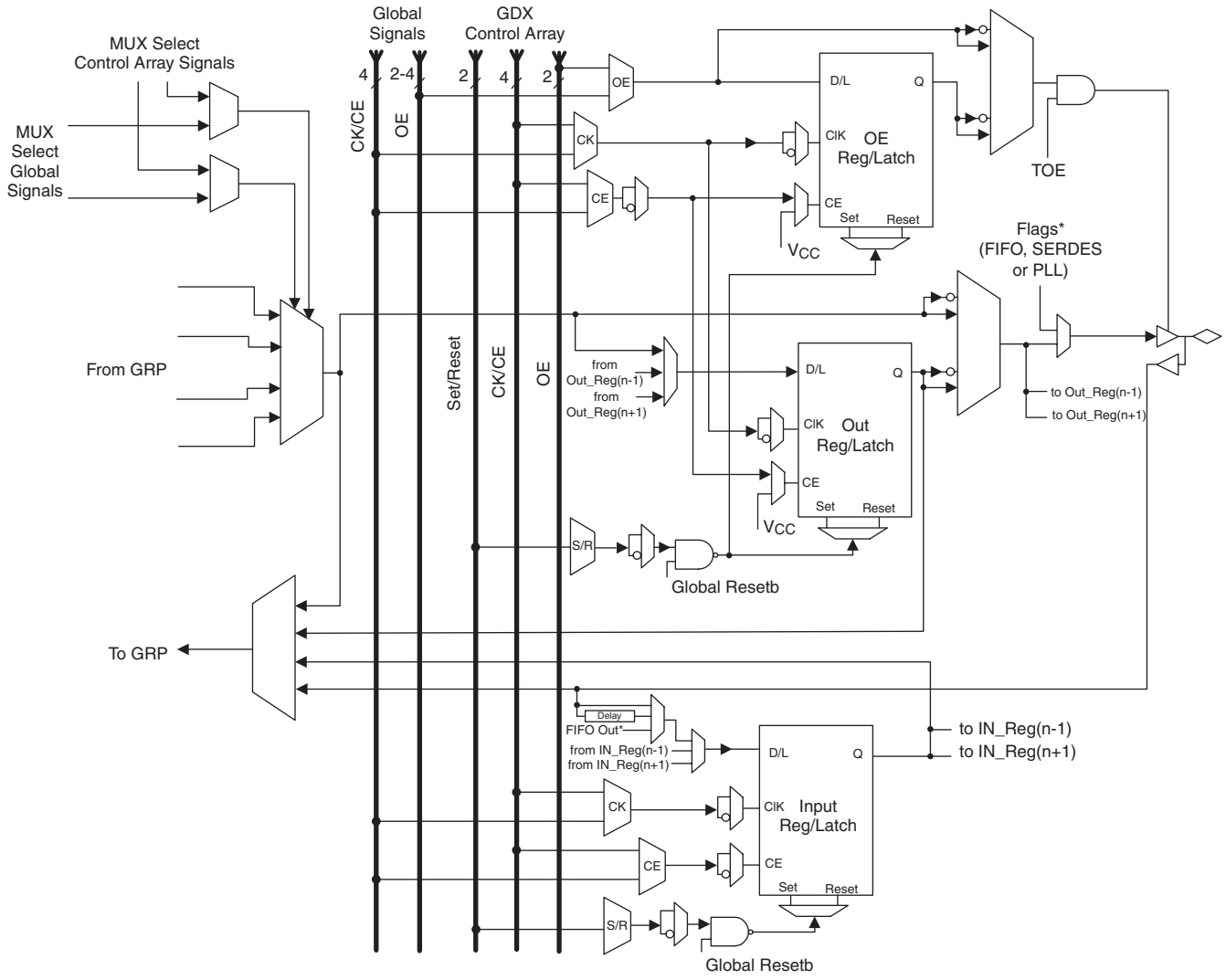
ispGDX2 MUX and Register Block (MRB)

Each MRB block has a 4:1 MUX and three registers. The output register has the same basic functionality as in the ispGDXV device. The two additional registers allow registering the input and output enable (OE) signals. These extra registers allow greater capability and efficiency for high-speed designs such as pipelining and reduced setup times.

The OE register allows synchronization of outputs, based on the same clock edge as the output register. This feature is critical in high-speed designs, since it increases the predictability of data arrival at the device pins, and provides minimal skew among outputs.

Separation of input and output registers effectively doubles the device register density. By using separate clock and clock enable signals, the input and output registers can be used independently. The built-in bi-directional shift register capability for each input and output register provides flexibility in resource usage. For example, it allows designers to build high-speed serializer/de-serializers through the GRP.

Figure 2. ispGDX2 MRB



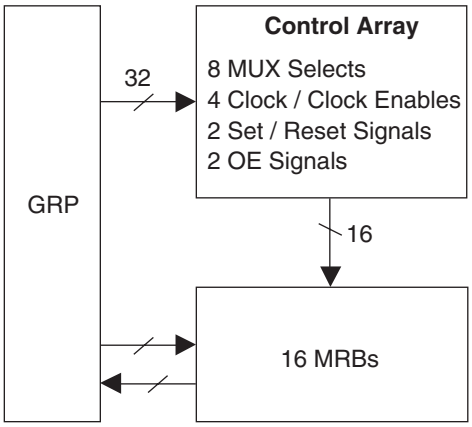
*Selected MRBs see Logic Signal Connection Table for details

Control Array

The Control Array, completely new to the ispGDX2, receives signals from the GRP and generates control signals for all 16 MRBs within a GDX Block. These control signals are derived from product term logic within the Control Array. The Control Array expands previous ispGDXV capabilities by allowing control signals to be simple logical combinations of many inputs. These signals include MUX selects, clock/clock enables, set/resets, and output enables. Figure 3 shows the connectivity between the Control Array, GRP, and MRBs.

As an example of added flexibility from the Control Array, consider register initialization. While the ispGDXV registers could be reset only using the global reset pin, the ispGDX2 allows independent set/reset signals from the Control Array.

Figure 3. Control Array



I/O Enhancements

Another significant advantage of the ispGDX2 architecture is in the supported I/O standards. While the ispGDXV device allows LVCMOS levels of 3.3V or 2.5V for each I/O, the ispGDX2 device family provides a much wider range of I/O standards. A complete list of supported I/O standards and their applications is listed in Table 2.

The inputs and outputs of each ispGDX2 device are divided into eight programmable sysIO banks, which can be configured independently to utilize any of the available I/O standards. As shown in Figure 4, each sysIO bank has its own I/O supply voltage (V_{CCO}) and reference voltage (V_{REF}), allowing each bank to be completely independent from the other. Each I/O within a bank can be configured to any of the different I/O standards consistent with the supplied V_{CCO} and V_{REF} levels.

Figure 4. ispGDX2 I/O Banks

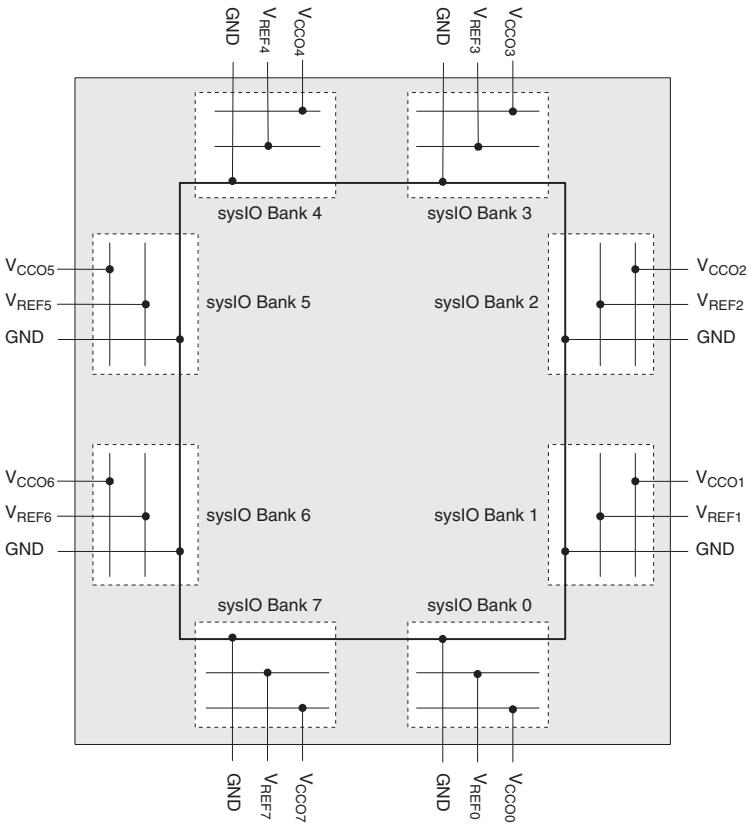


Table 2. ispGDX2 Supported I/O Standards

sysIO Standard	Nominal V_{CCO}	Nominal V_{REF}	Nominal V_{TT}	Application
LVCMOS 3.3	3.3V	-	-	Standard Interface
LVCMOS 2.5	2.5V	-	-	
LVCMOS 1.8	1.8V	-	-	
LVTTL	3.3V	-	-	
PCI 3.3V	3.3V	-	-	Bus Interface
PCI-X	3.3V	-	-	
AGP-1X	3.3V	-	-	
GTL +	1.8/2.5/3.3V	1.0V	1.5V	
SSTL3 class I & II	3.3V	1.5V	1.5V	DRAM Interface
SSTL2 class I & II	2.5V	1.25V	1.25V	
CTT 3.3	3.3V	1.5V	1.5V	
CTT 2.5	2.5V	1.25V	1.25V	
HSTL class I	1.5V	0.75V	0.75V	SRAM Interface
HSTL class III	1.5V	0.9V	0.75V	
HSTL class IV	1.5V	0.9V	1.5V	
LVDS	2.5/3.3V	-	-	High Speed Interface
BLVDS	2.5/3.3V	-	-	

Clock Implementation

Like the ispGDXV family of devices, the ispGDX2 features four dedicated clock nets that are routed to all registers/latches and available for use as a clock or clock enable. In the ispGDXV, these nets were driven directly from four global clock pins. The ispGDX2 also retains this basic functionality, but adds the capability to be driven differentially and/or via an available sysCLOCK PLL. Pairs of clock inputs are used to implement LVDS differential clocks. The ability to drive a clock from an I/O is preserved in the ispGDX2, but offers enhancement by way of the Control Array. The Control Array allows the clock and clock enable signals to be derived from a combination of signals as a product term.

ispGDX2 Advanced Features

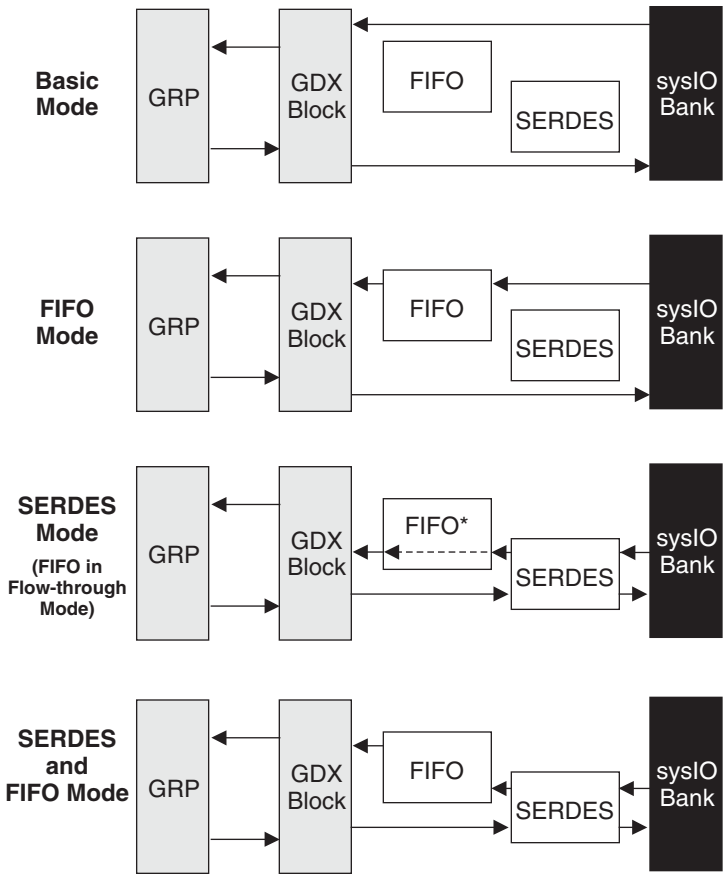
sysCLOCK PLL

High-speed designs push the limit of clock speed while shrinking the system timing budget. These changes in the system environment demand a more precise clock control in programmable devices. Up to four sysCLOCK PLLs are available in ispGDX2 devices to provide enhanced control of system clocks. Each sysCLOCK PLL is comprised of a PLL and programmable network of elements consisting of dividers, delays, and feedback. These features permit clock dividing, multiplying, skewing/de-skewing, and synchronization capabilities.

Operating Modes

All GDX blocks in the ispGDX2 family can be programmed in four modes: Basic, FIFO only, SERDES only, and FIFO and SERDES mode (Figure 5). In basic mode, the SERDES and FIFO are disabled and the MUX output of the MRB connects to the output register. Inputs are connected to the GRP via the MRB.

Figure 5. Operating Modes



*FIFO held in RESET for SERDES-only mode.

FIFO

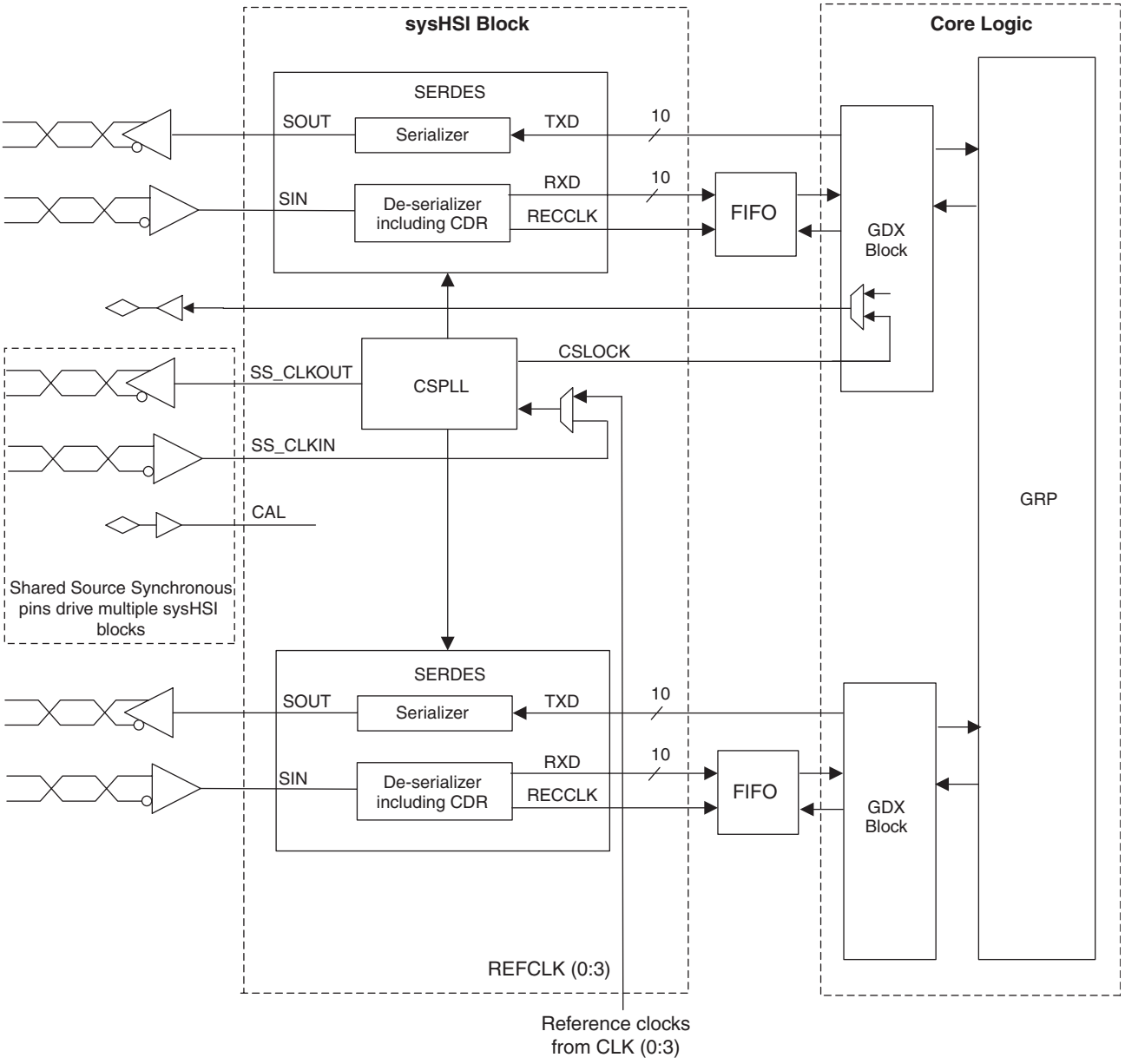
The ispGDX2 FIFO block is comprised of a 10-bit wide, 15-word deep RAM configured as a “circular queue” structure. The FIFO is intended for synchronization between SERDES and ispGDX2 internal logic, although it can be used as a generic FIFO operated either synchronously or asynchronously. In FIFO mode, 10 of the I/O from the associated GDX block are used for data and three are used for status monitoring. The three flags available for monitoring the status of each FIFO are Empty, Full, and Start Read. Up to 16 such blocks are available in the ispGDX2.

High Speed Serial Interface Block (sysHSI Block)

The ispGDX2 device family incorporates multiple High Speed Serial Interface blocks that permit up to 850Mbps transfer rates per LVDS I/O pair. Each sysHSI block utilizes two serializer/de-serializer (SERDES) elements that feature clock/data recovery (CDR) circuitry. Each SERDES can be used as a full duplex channel. The SERDES pair within a sysHSI block share a common clock signal coming from its own sysHSI PLL. Therefore, using sysHSI blocks will not consume any generic PLL resources in the device. Figure 6 illustrates the sysHSI block and its interface.

Two common data coding modes are supported in the sysHSI block: 10B/12B and 8B/10B. The 10B/12B mode is fully implemented within the ispGDX2 device, including coding and decoding. For 8B/10B, the symbol boundaries are aligned, but external encoding and decoding is required. In addition, sysHSI blocks support Source Synchronous mode with a 4, 6, or 8 channel interface.

Figure 6. sysHSI Block



Note: Some pins are shared. See Logic Signal Connections table for details

Summary

Unlike its predecessors, targeted for standard bus multiplexing, signal routing and switching, and board layout control for broad range of system designs, the ispGDX2 family offers greater flexibility and more features to facilitate high-speed data switching and routing. This is particularly true in systems that require high-speed serial data link support. A wider range of I/O standards and integrated PLL functionality permit greater capability and reduce the need for additional components. The sysHSI block, with integrated SERDES and FIFO modules, provide system designers with an integrated platform for managing multi-gigabit data transfer rates.

Additional Information

For more information, please refer to the following documents:

- *ispGDX2V/B/C Family Data Sheet*
- Technical Note TN1020, *sysHSI Block Usage Guidelines*
- Technical Note TN1000, *Lattice sysIO Design and Usage Guidelines*
- Technical Note TN1003, *sysCLOCK PLL Design and Usage Guidelines*

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