mobileFPGA™ Decoupling/Bypass Recommendations

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Introduction

This document discusses two aspects of power stabilization: decoupling and filtering. Although many use these terms interchangeably, they are distinct and sometimes contradictory conditions. Decoupling is a means of insuring energy transfer capabilities at or to a specific point. Filtering relates to the conditioning of a signal along a path - with separate start and finish locations. Although good decoupling may preclude the requirement for filtering, filtering is not the primary consideration. Likewise, good filtering may include some decoupling, but it is not optimized for this task. This document will highlight the need to plan and design for adequate power distribution.

Power/Ground Planes

SiliconBlue recommends the use of power and ground planes. The primary function of these planes is to provide a low impedance path between the power source and the device. The planes must have low resistance to ensure minimum voltage drop between the device and the power source. This can be aided by keeping via connections to a minimum. When vias cannot be avoided, use large vias for power and ground connections. The power and ground vias should connect to all of the layers associated with a particular plane.

Power traces and vias should also be thoughtfully designed. The noise generated by the device can be minimized by having the power trace pass from a via to a decoupling capacitor pad and then to the device. Using this connection sequence, the resistance and inductance of the trace and via will help isolate the component noise. Keep the trace between device and the bypass capacitor as short as possible. A short, wide trace will produce a lower inductance and resistance.

Decoupling/Bypass Capacitors

Decoupling or bypass capacitors play a large role in device performance. The main role of bypass capacitors is to act as a local DC power supply to meet the demands of fluctuating power rails. In addition, bypass capacitors block unwanted noise going into or coming from the power plane, as well as the device generated switching noise and capacitive and inductive coupling from adjacent board level planes and traces. Decoupling must consider many frequency bands. Below is a list of guidelines for proper decoupling:

- Bypass capacitor usage must take into account both a low equivalent series resistance (ESR) as well as the self-resonant frequency
- SMT (Surface Mount Technology) or chip capacitors made of ceramic will yield the best results
- Capacitor values should vary between 0.1uF and 0.01µF per device power pin to manage inductance – consult your capacitor data sheets for the impedance verses frequency plots
- Decoupling capacitors should be placed as close as possible to the device power pins, and use short, wide traces to vias when they are required
- Distribute some bulk capacitance (1uF and 10uF) throughout the layout to help eliminate low frequency coupling and maintain a low impedance power system
- Use a large electrolytic capacitor (100uF) at power source

Inadequate sizing and improper locating of power supply decoupling capacitors can result in numerous board problems. The most common problem associated with inadequate decoupling capacitance is power supply noise (i.e., high frequency noise and or droop). It is the function of the decoupling capacitor to deliver the quick burst of energy, within a specified time element, without generating a noise pulse or an apparent voltage droop. If the decoupling capacitor does not support the switching charge requirements of the device, the power supply must deliver the additional current. These additional charging and discharging cycles can cause undesirable fluctuations.

If the device is powered from a regulated power supply, the regulator noise will increase depending upon the external load current drawn from the regulator. Therefore, it is good design practice to provide RF bypassing of power and DC control lines to the device. RF chokes and good bypassing capacitors of approximately 1000 pf to 100 µF are recommended at the DC supply lines.

Note that the noise performance of the device may degrade depending upon the type of regulator used, and also upon the load current drawn from the regulator. To improve the noise performance of the device under external load conditions, place a low ESR electrolytic capacitor of about 10 µF on the voltage line.

For Noisy Environments

Since mobile applications typically do not exhibit much noise on their power planes, filtering is generally not required. However, there may be instances where the power distribution between stages cannot be sufficiently bypassed. In these specific cases, an inductive choke offers a high impedance path to any errant signals or noise between stages, while offering a very low resistance pathway to the supply. With device interfaces that have several independent device supplies that have common voltage values, these supplies often can share the common voltage rail if the board design can guarantee that the supplies are isolated. This can be accomplished with simple LC filtering schemes to prohibit device supplies from being influenced by power supply fluctuations. A Ferrite Bead inductor of about 4-10uH, with good current carrying characteristics and low resistance can be placed in series with the voltage source to choke off the high frequency noise that may be caused by other shared supplies.

In very extreme cases, it may become impossible to adequately reduce a board's exposure to voltage and current spikes. In this case, it is possible to momentarily clamp the spikes to the power supply protecting the devices on the board. For this, Transient Voltage Suppressors (TVS) can be used. These devices are similar to zener diodes, but offer a much faster turn-on time. There are several types of transient suppressor diodes available. The TVS device should be selected to allow a device that will turn on at a specific voltage, clamping a voltage spike to the supply. The device turn-on voltage should be above the board (or design) VCC, but below the level of potentially damaging noise.

Revision History

Version	Date	Description
1.0	8-MAR-2010	Initial Release.

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