Hot Socketing with ispMACH 4A and MACH 5 Devices

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Abstract

Lattice provides robust and feature-rich I/O structures in its ispMACH™ 4A and MACH 5 families of devices. To take advantage of these features, it is helpful to understand the characteristics on both a family basis and a technology basis. This application note describes the Lattice I/O characteristic in hot socketing.

Background

The Lattice ispMACH 4A and MACH 5 CPLD families have superior routability, performance, and I/O characteristics that make them ideal for today's complex system designs. The routability features include multiple switch matrices, complex macrocell architectures, wide product term allocators, and large numbers of inputs into the arrays. The performance features include fast, predictable speeds, power management capabilities and slew rate control. Detailed information about MACH routability and performance can be obtained from the MACH data sheets.

The I/O characteristics help to set the ispMACH 4A and MACH 5 devices apart from all other architectures. Some of the advanced features they offer to enhance a system design include globally programmable pull-up or Bus-Friendly latches, hot socketing, mixed supply capability and PCI compliance.

The process technology used in the manufacture of ispMACH 4A and MACH 5 devices is the 0.25µm Leff process. As device feature sizes are reduced, so must the voltage supply because of the internal electric fields that are generated across the gate oxides. The 0.25µm process is a 3.3V technology.

Hot Socketing

Hot socketing is a feature that means different things to different designers. There are two common scenarios found in hot socketing environments.

Scenario 1: A board or device is plugged into a system that is already powered up.

In this scenario, the principal cause for concern is latch-up. When inserting a board or device, it can be several milliseconds before all of the required connections have been made, and there is no particular order in which those connections are made. As a result, signal pins can be connected and driven before either V_{CC} or ground, and this can lead to latch-up in CMOS devices if they are not designed to handle this condition. When a device latches up, a low-impedance path to ground is formed within the device, and the device begins to sink large amounts of current. If the situation is not rectified quickly (i.e. by cycling the system power), the device could be thermally destroyed, necessitating its replacement.

Scenario 2: The board is powered-down and the system is still powered up and active; the powered-down board or devices continue to be connected to the active nets in the system.

In this scenario, the possibility of signal disturbance can arise. Signal disturbance takes place when an inactive device affects the functionality of active signals. This can happen when the inactive device has a leakage path to either V_{CC} or ground, or when the device is driving the signal line during power-up or power-down. All ispMACH 4A and MACH 5 devices tri-state their I/Os during power-up and power-down, and as a result, this is not a concern for bus disturbance.

Hot Socketing Specification

The most dangerous of the two hot socketing scenarios takes place when a voltage is placed on an input and the device goes into latch-up as a result. Most devices are designed to prevent latch-up from happening when VCC is at a nominal level such as 5V or 3.3V. When VCC is at 0V, however, the situation is much different in that signals driven into inputs or I/Os could potentially force the device into latch-up. The Hot Socket Latch-up Current specifica-

tion in Table 1 indicates the amount of latch-up current that MACH devices can tolerate without being damaged. This information also appears in the “Absolute Maximum Ratings” section of the device data sheets.

Table 1. I_{LUHS} Specification

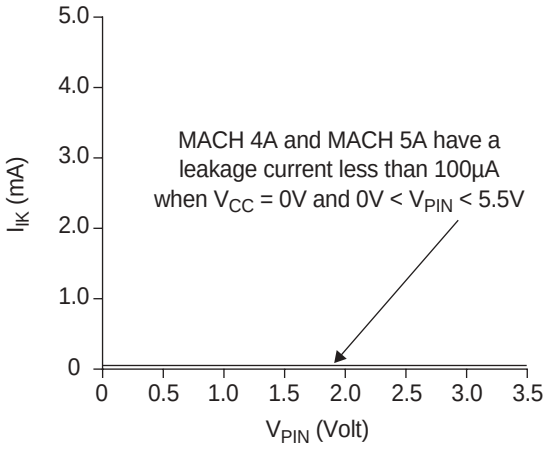
Parameter Symbol	Parameter Description	Test Description	Max	Unit
I_{LUHS}	Hot Socket Latch-up Current	V_{CC} = 0.0V, V_{IN} = 5.5V	200	mA

The second of the two scenarios is much less dangerous from both the device standpoint and the system design standpoint. When a device no longer has power applied to it, yet is still connected to active signals and buses, that device should have no affect on the active signals. If it does, precautions must be taken to ensure the system will not be adversely affected and can tolerate the strong leakage paths. If the system cannot tolerate the influence of the powered-down devices, there are design techniques that can be employed to work around the problems.

3.3V, 0.25µm I/O Buffer Hot Socketing Characteristics

The 3.3V, 0.25µm ispMACH 4A and MACH 5 devices are the most robust devices from the hot socketing standpoint. Not only do they meet the requirements for latch-up current, but they also have a minimal amount of leakage current when the devices have no power applied. During power-up, all of the ispMACH 4A and MACH 5 devices have their output drivers disabled such that the I/Os are in a high impedance state. Because of the design and the process, the 0.25µm ispMACH 4A and MACH 5 devices have a leakage current less than 100µA per pin when V_{CC} = 0V and 0V < V_{PIN} < 5.5V.

Figure 1. 3.3V, 0.25µm Typical Leakage Current Characteristics



Conclusion

ispMACH 4A and MACH 5 devices offer several advanced features including the hot socketing feature that can be invaluable in a system design. To take full advantage of these features, the designer must be aware of the effects that each feature may have on the system.

Technical Support Assistance

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