Introduction

Power/Platform Management devices are a single-chip, fully-integrated solution to supervisory and control problems encountered when implementing on-board power conversion and distribution systems. They provide several types of on-chip resources which can be used to meet the requirements of these applications. Power/Platform Management devices have analog comparators with independently adjustable references, providing the ability to detect when a voltage is greater than or less than a given threshold. They have timers to implement programmable delays and an embedded logic to support the implementation of state machines and sequencers, providing embeddable intelligence in a power supply design.

See Table 1 and Table 2 for the Power/Platform Management devices applicable to this application note.

Table 1. Applicable Power Manager Devices Summary

| Device	VMONs	Digital Inputs	HVOUTs	Open Drain Outputs	Trim DAC Outputs	Macrocells
ProcessorPM™-POWR605	6	2	None	5	None	16
ispPAC®-POWR607	6	2	2	5	None	16
ispPAC-POWR1014/A	10	4	2	12	None	24
ispPAC-POWR1220AT8	12	6	4	16	8	48

Table 2. Applicable Platform Manager™ Devices Summary

Device	VMONs	Digital Inputs	HVOUTs	Open Drain Outputs	Trim DAC Outputs	Digital I/O	CPLD Macrocells	FPGA LUTs
LPTM10-1247	12	4	4	12	6	31	48	640
LPTM10-12107	12	4	4	12	8	91	48	640
LPTM21[3]	10	—	4	10[1]	4	95[2]	—	1280
L-ASC10[3]	10	—	4	9[1]	4	—	—	—

1. Platform Manager 2 Open Drain Outputs can be configured as inputs.
2. Platform Manager 2 Digital I/O count does not include SDA_M, SCL_M, or JTAGENB pins.
3. The HIMONN_HVMON input of L-ASC10 and LPTM21 does not support extended range configuration.

This application note describes how to use the VMON input pins of the Power/Platform Management devices to monitor power supplies, both positive and negative, that exceed the normal input range. Each device incorporates an extensive set of independently programmable voltage thresholds to directly monitor a wide range of over- and under-voltage conditions. Each set of voltage thresholds (or trip points) are grouped around common power supplies of 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V, and 5 V. In addition, there is a special trip point (typically 75 mV) for monitoring power supply discharge conditions. The need, however, occasionally arises to monitor or sequence power supplies whose operating voltages fall outside the input range of the Power/Platform Management devices. In the sections that follow, we will show how to monitor both positive and negative voltages that exceed the maximum ratings, as well as near ground conditions. Also, we will discuss the design considerations that impact the performance of this solution. The suggestions in this application note are not supported by HIMONN_HVMON input of LPTM21 and ASC-10 devices.

Figure 1. Typical Application
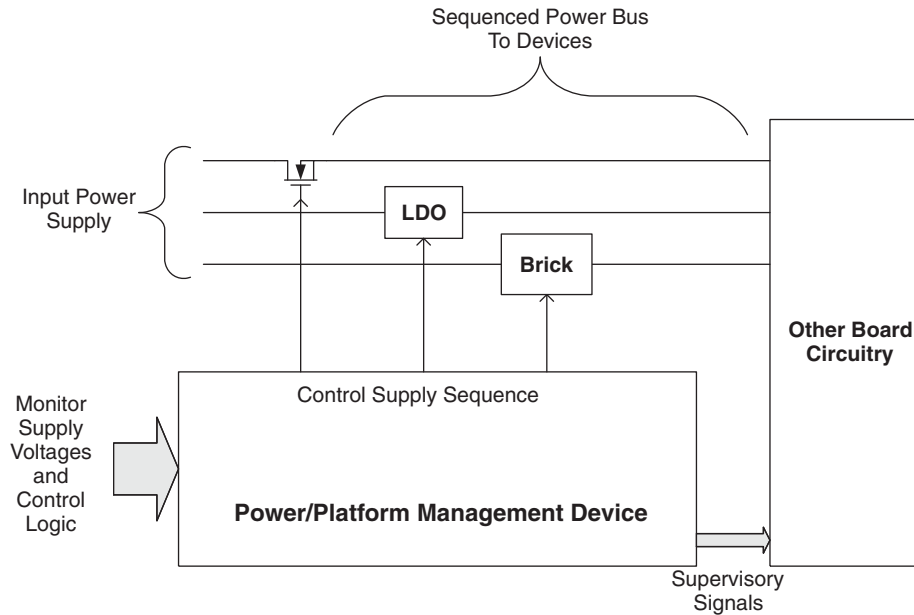
Background

Each Power/Platform Management device has a number of analog inputs for monitoring power supply voltages and digital inputs for additional logic control. The analog inputs are connected to the non-inverting inputs of the comparators (see Figure 2). Each comparator has a programmable voltage reference connected to the inverting input, which sets the trip point. The outputs of the comparators are used as inputs to the on-chip programmable logic circuits. The outputs of the logic circuits control the digital or high voltage charge pump outputs. The charge pump outputs have a constant-current output that is also programmable and designed to directly drive the gates of N-channel power FETs.

Figure 2. Typical Power Manager VMON Analog Input
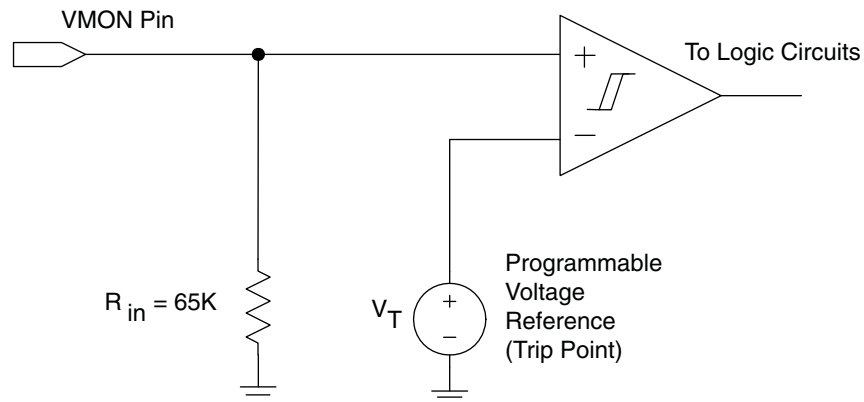
Each Power/Platform Management device can be programmed using Lattice's easy-to-use Windows-based design software, PAC-Designer®. LogiBuilder is a design environment within PAC-Designer that can be used to design, simulate, and program the programmable logic with a custom state machine based on the specific requirements of the application. This application note focuses on the comparators and VMON analog inputs that are common to each member of the Power/Platform Management device family.

Comparator Review

A comparator is an analog building block that functions similarly to an open-loop op-amp with a high-speed output. Another way to view a comparator is as a single bit analog-to-digital converter. Typically a comparator's output is designed for speed instead of linearity, so it can quickly swing from one logic state to the other. Comparator outputs are most often implemented with either totem-pole or open-drain (open-collector) circuits. The functionality of a comparator can be summarized in the following:

- Output is HIGH if $V(+) > V(-)$
- Output is LOW if $V(+) < V(-)$

Positive feedback can be incorporated into a comparator to provide hysteresis. The purpose of hysteresis is to prevent the output from stuttering or oscillating when the voltage at each of the two inputs is essentially the same.

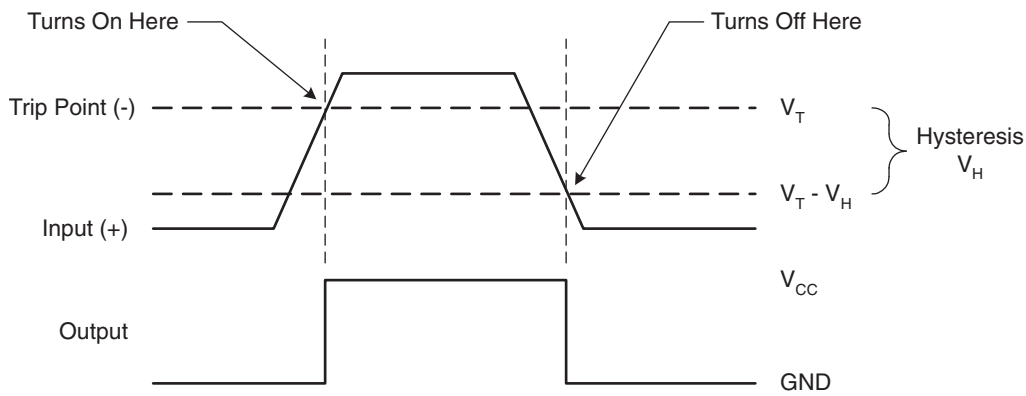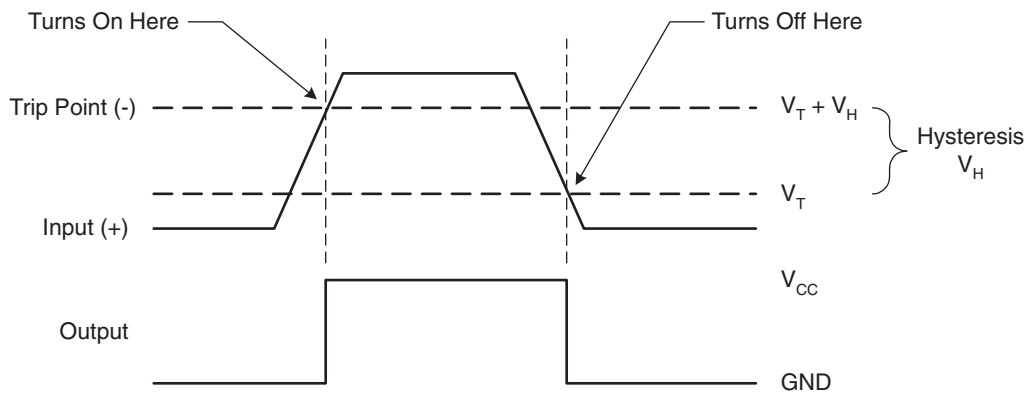*Figure 3. Over-voltage Comparator Hysteresis in the Power/Platform Management Device*

Figure 4. Under-voltage Comparator Hysteresis in the Power/Platform Management Device

The effect of hysteresis (V_H) on the actual trip point (V_T) is seen in Figure 3. Here, the output of the comparator goes HIGH when the input crosses the precision over-voltage trip point (upper dashed-line V_T). Then the hysteresis kicks in, preventing the output from going low until the input falls below the lower dashed-line ($V_T - V_H$). Each of the comparators within any Power/Platform Management device has a fixed hysteresis value.

Table 3. Hysteresis for POWR1220AT8

Trip-point Range (V)		Hysteresis (mV)
Low Limit	**High Limit**	
0.664	0.79	8
0.79	0.941	10
0.94	1.12	12
0.119	1.333	14
1.326	1.58	17
1.583	1.885	20
1.884	2.244	24
2.236	2.665	28
2.65	3.156	34
3.156	3.758	40
4.045	4.818	51
4.815	5.734	61
75 mV		0 (Disabled)

The effective hysteresis that is seen at the input pin is scaled up based upon the range of the trip point voltage and is summarized in Table 1 for the POWR1220AT8. For other devices please refer to respective data sheet. Links are provided in Related Literature section at the end of this document.

## Monitoring Voltages that Exceed the Maximum VMON Input Value

In this section we show how the Power/Platform Management device's VMON analog inputs can be used to monitor voltage levels that exceed the maximum ratings. This can be accomplished by using an external resistor divider and selecting a suitable comparator trip-point threshold. A few caveats to this approach include the following:

- The parallel input impedance of the VMON pin (nominally 65kΩ)

- The variability of the input impedance (typically ±15% or 55kΩ to 75kΩ)

Figure 5 shows an external resistor divider circuit that can be successfully used to accurately monitor positive voltages that exceed the normal input range. This divider consists of resistors R_1 and R_2. The voltage to be monitored (V_M) comes into the divider at the top or R_1. Note that R_{IN} is in parallel across resistor R_2 and will provide additional attenuation in the divider circuit. However, when the resistance of R_2 is significantly less than R_{IN}, the variations in R_{IN} will have minimal effect on the divider accuracy. Because voltages that exceed the maximum recommended values are being considered, it is a good design practice to place a Zener diode (D_1 with a Zener voltage of 5.1 V) between the input node and ground to protect the VMON input circuits from surges or spikes.

To minimize the effect and variability of the VMON input impedance on the divider, the dropping resistor R_2 should be in the 1kΩ range.

Figure 5. Monitoring Positive Voltages with External Divider
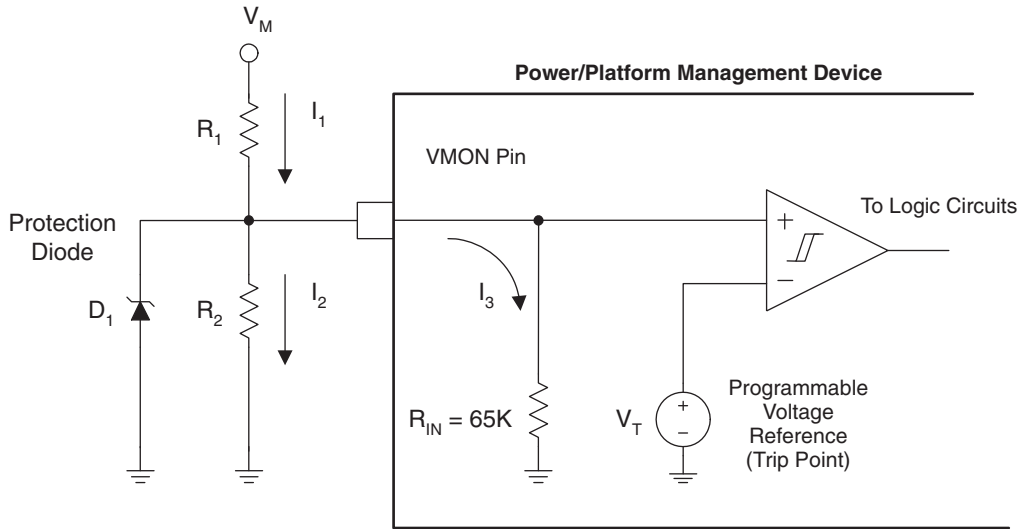
From analysis of the circuit we can see that the current (I_1) through R_1 is the algebraic sum of I_2 and I_3 as shown in Equation 1.

$$I_1 = I_2 + I_2 \tag{1}$$

This leads directly to a voltage over resistance substitution as shown in Equation 2.

$$\frac{V_M - V_T}{R_1} = \frac{V_T}{R_2} + \frac{V_T}{R_{IN}} \tag{2}$$

To simplify the selection process of possible resistor values and trip point combinations that can be used to develop the desired division, the following procedure is suggested. Select resistor R_2 to be 1kΩ and select a trip point voltage V_T in the 1.0 V to 1.2 V range. With R_2 and V_T set to these values, the effect from large variations of R_{IN} (±15%) will be reduced to less than ±0.15%, as described in Appendix A, and the monitor current I_1 will be in the range of 1mA (according to Ohm's law). Now, R_1 remains as the only unknown. Equation 2 can easily be transformed into Equation 3, so that an exact value for R_1 can be calculated.

$$R_1 = \frac{R_2\, R_{IN}}{R_2 + R_{IN}} \tag{3}$$

Substituting values for R_{IN} (65kΩ) and R_2 (1kΩ), Equation 3 is simplified to the more usable form shown in Equation 4.

$$R_1 = 948.8\left(\frac{V_M}{V_T} - 1\right) \tag{4}$$

Example 1: Monitoring +12 V with the POWR1220AT8

In this example, a POWR1220AT8 is used to monitor a 12 V power supply. The 1.205 V trip point is used with a 1kΩ resistor for R_2, which will draw just over a milliamp of current to sense the supply voltage. An exact value for R_1 is obtained using Equation 4, which in general will not result in a standard resistance value, but it does provide a target from which the closest 1% resistor (or combination of resistors) can be selected.

Given:
  V_M = 12.0 V
  V_T = 1.205 V
  R_2 = 1000Ω
  R_{IN} = 65,000Ω

Calculated:

$R_1 = 8822\Omega$

The closest 1% resistor is 8870 (selected form a standard list of 1% resistor values) and is still within 1% of the target value.

Example 2: Monitoring +36.0 V with the POWR1220AT8

In this example, a POWR1220AT8 is used to monitor a 36.0 V power-supply. The 1.006 V trip point is used with a 1kΩ resistor for R_2, which will draw right at a milliamp of current to sense the supply voltage. An exact value for R_1 is again obtained using Equation 4.

Given:

$V_M = 36.0$ V
$V_T = 1.006$ V
$R_2 = 1,000$
$R_{IN} = 65,000$

Calculated:

$R_1 = 34,256\Omega$

In this example, the closest 1% resistor value is 34.0kΩ, which is low by 256 ohms (about 1%). A 255Ω resistor could be added in series with R_1 to obtain the target resistance value. As an alternative, Equation 4 could be rewritten as shown in Equation 5 to solve for a trip-point (V_T) using the closest standard resistance value for R_1. For this example, Equation 5 suggests a V_T of 1.0133 V. The trip-point table from the POWR1220AT8 Data Sheet lists a 1.012 V setting. Therefore the 34.0kΩ standard 1% resistor can be used with that setting.

$$V_T = \frac{V_M}{\left(\dfrac{R_1}{948.8} + 1\right)} \tag{5}$$

Calculated:

$V_T = 1.0133$ V

Monitoring Voltages At or Near Ground

Many systems have a power sequencing condition that requires that certain supplies be fully off before the initial sequence or a re-sequence. Often the threshold for this "off" condition is below 1.0 V, which is below the lowest trip point setting of near-ground 75 mV trip point. In some cases, the voltage to be monitored may still be below the available pre-set trip points, either because the voltage is between 75 mV and 0.672 V (for POWR1014/A). This situation is still within the capabilities of the Power/Platform Management devices by adding two external resistors as shown in Figure 6.

Figure 6. Near Ground Voltage Monitor Circuit
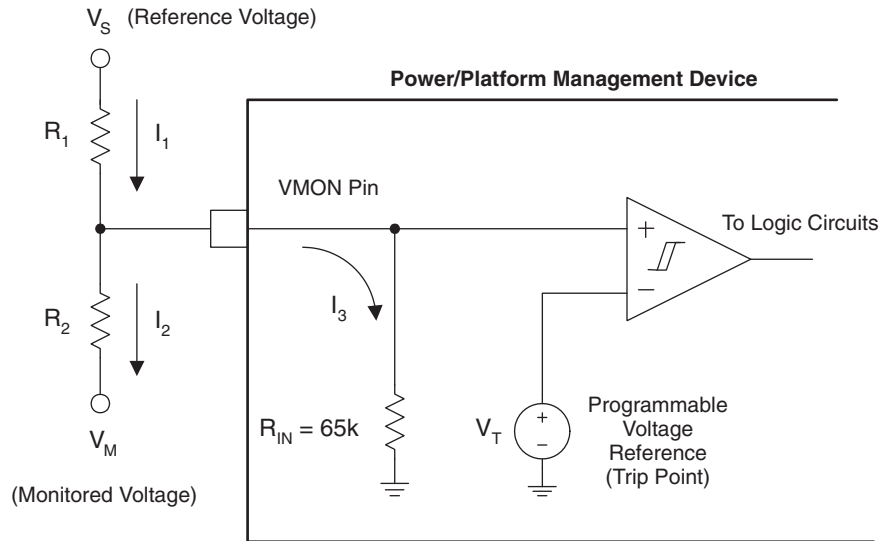
The circuit in Figure 6 is still a two-legged voltage divider, with the top of R_1 is connected to the Platform/Power Management device's supply pin (V_{DD} or other voltage reference) and the bottom of R_2 is referenced to the supply that is to be monitored. Just as in the previous case, the VMON input impedance R_{IN} is in parallel with R_2 and the currents sum as described in Equation 1. Substituting the corresponding voltages and resistors from the circuit results in Equation 6.

$$\frac{V_S - V_T}{R_1} = \frac{V_T - V_M}{R_2} + \frac{V_T}{R_{IN}} \tag{6}$$

Again, R_2 should be in the 1kΩ range to minimize the effect of R_{IN}, but the trip point value should be between the reference voltage (V_S) and ground (1.5 V to 2.5 V). Thus, Equation 7 solves for the unknown R_1 value and assumes the nominal value for R_{IN} (65kΩ).

$$R_1 = \frac{V_S - V_T}{\frac{V_T - V_M}{R_2} + \frac{V_T}{65,000}} \tag{7}$$

As was the case in Example 2, Equation 7 will result in an exact value for R_1 that will probably not be available from the standard 1% values. Thus, Equation 8 can be used to solve for a trip point voltage after the closest 1% resistor is selected for R_1. Now we will take a look at a few more examples.

$$V_T = \frac{R_2 V_S + R_1 V_M}{R_1 + R_2 + \frac{R_1 R_2}{65,000}} \tag{8}$$

Example 3: Monitoring +0.5 V with the POWR1014/A

In this example, the POWR1014/A needs to know when a supply falls below 0.5 V. The device has a supply voltage of 5 V, used for the reference, R_2 is 1kΩ, and the starting trip point is 1.502 V. Using Equation 7, a value for R_1 is calculated.

Given:
    V_M = 0.5 V
    V_T = 1.502 V
    V_S = 5 V

$R_2 = 1,000\Omega$
$R_{IN} = 65,000\Omega$

Calculated:
$R_1 = 3412\Omega$

Consulting the standard 1% resistor tables, a 3.4kΩ resistor is found. Equation 8 provides a target trip point to use with the 3.4kΩ resistor and the trip point table from the data sheet or PAC-Designer software provides a trip point of 1.511 V that is only 3 mV high.

Calculated:
$V_T = 1.508$ V

Example 4: Monitoring +0.1 V with the POWR1220AT8

In this example, the POWR1220AT8 needs to hold off the power sequencing if a certain supply is higher than 0.1 V. While the steps outlined in the previous example could be used to design an external divider, we choose to simply set the trip point to the 75 mV setting. In this case, it is not critical that the sequence starts exactly when the supply dips below 0.1 V. While this approach is a slight overkill, it saves valuable engineering time and simplifies the design.

Monitoring Near Ground Using an Op Amp

Another option for near ground sensing is to amplify the signal with an external op-amp. This option is useful for both determining when a supply is turned off, or for monitoring a sensor signal such as temperature. The circuit in Figure 7 has the added benefit that it is not dependent on a supply or reference voltage (as is the circuit in Figure 6). The gain of the op-amp circuit is configured with resistors R_1 and R_2 and should be designed to place the op-amp output voltage near one of the VMON trip points. Equation 9 can be used either to compute the trip point voltage, or rewritten to obtain the resistor ratio. Like most op-amp circuits, the resistor values for this amplifier should be in the 100Ω to 100kΩ range to minimize noise. Also the closed-loop output impedance of most op-amps is low enough to drive the VMON input impedance R_{IN} without any loss in accuracy.

Figure 7. Op Amp Gains Near Ground Voltage for VMON Trip Point
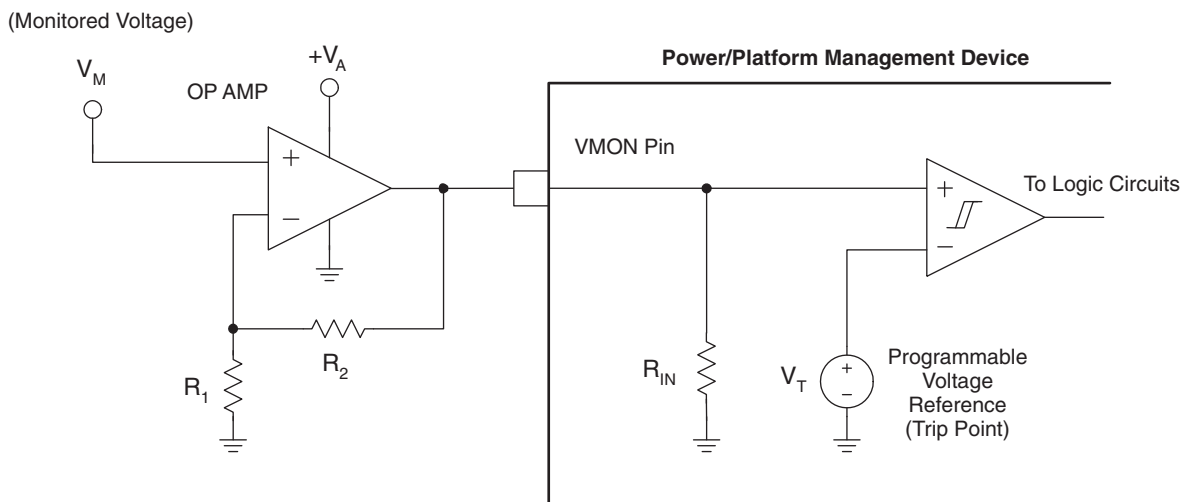
$$V_T = \left(1 + \frac{R_2}{R_1}\right)V_M \qquad (9)$$

Example 5: Monitoring Temperature Sensor with POWR1220AT8

In this example an POWR1220AT8 is used to control a cooling fan based on a temperature sensor. If the output from the temperature sensor exceeds 0.25 V, it is too hot and the fan needs to be turned on. The 0.25 V threshold falls between the 75 mV and 0.664 V trip points that are available using the POWR1220AT8. The solution is to use an op-amp to amplify the signal to a level within the trip point table. A gain of ten would result in a trip point of 2.5 V and a gain of two would result in a trip point at 0.5 V. So any gain between three and ten should suffice. It is decided to use a 3.40kΩ 1% resistor for R_2 and a 1kΩ 1% resistor for R_1 because they are used elsewhere in the design. This results in a gain of 4.4 (portion of Equation 9 within the brackets) and a trip point of 1.10 V. The POWR1220AT8 supports this trip point with 1.102.

Threshold Voltages and Hysteresis

In Example 1, the POWR1220AT8's threshold voltage was set to just one value (1.205 V) out of 368 possible values. PAC-Designer makes it easy to select the value by clicking on the analog inputs to bring up the Analog Input Settings dialog box (see Figure 8). Clicking on the "Trip Point" for the respective input will bring up the list of all 368-voltage values. Notice in Figure 8, that for the 1.205 V trip point the comparator hysteresis is 14 mV. The actual hysteresis seen at our 12 V input will be scaled up or down by the voltage divider ratio VMON / V_T. For the nominal values used in this example, the ratio is 9.98:1 (12 V to 1.205 V) and the resulting hysteresis at VMON is 139 mV. Note in Figure 8, the user defined signal is named to reflect the 12 V supply, and the trip point inside the POWR1220AT8 is set to 1.205 V.

Figure 8. VMON1 Analog Input Settings from PAC-Designer

Monitoring Voltages Below Ground

Although the Power/Platform Management devices do not require a negative supply, they can be used to monitor negative supply voltages. Figure 9 depicts a circuit similar to the previous voltage divider circuits, but with the negative supply (V_M) connected to the bottom of R_2. The functionality of this circuit is enhanced by the fact that the reference voltage (V_S) can be monitored and verified by another analog VMON input of the same Power/Platform Management device.

Figure 9. Negative Voltage Divider
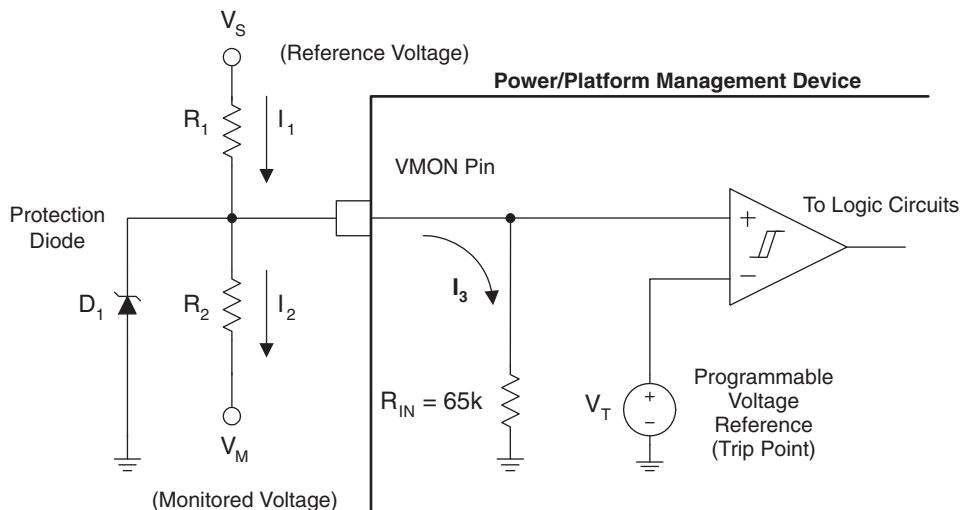
When the reference supply V_S is below the maximum VMON input value, the protection diode D_1 could actually be a signal diode (1N4148), instead of a Zener, to prevent the input node from going negative. Two caveats of this solution are the inverted logic of the comparator output and the accuracy of the V_S reference supply.

The inverted logic is a result of the following: 1) when the negative supply is at ground, the Power Manager VMON input will be above the trip point, and 2) when the negative supply is on and stable, the same VMON input will be below the trip point. However, this inversion is easily addressed in PAC-Designer using negation modifiers within LogiBuilder. Accuracy in the reference supply (V_S) is not required when simply verifying that the negative supply is functional. If greater accuracy is needed, a buffered precision reference can be used; otherwise any positive power supply can be used for the reference voltage (V_S).

The suggested approach to solving for the resistor values is slightly different for the negative supply case than was shown for positive voltage monitoring. Start by selecting a reference supply (V_S) and a trip point (V_T). Next, decide on the approximate monitor current (I_2) that both the supply and resistors can handle (target values of 1mA to 10mA). For the purposes of selecting a resistor value for the top of the divider, the current I_2 is close enough to use Ohm's law (Equation 10) to compute a value for R_1. The calculated value for R_1 is used as a target to select a standard 1% resistance value. The actual value of R_1 can be used with Equation 10 to derive the actual current I_1, as it will be used later.

$$R_1 = \frac{V_S - V_T}{I_1} \tag{10}$$

The calculation of the R_2 value also follows from Ohm's law and is obtained from the voltage drop divided by the monitor current I_2. The voltage drop is the potential difference from the trip point (V_T) to the negative supply (V_M). The monitor current I_2 from the negative supply is the algebraic difference of $I_1 - I_3$, as seen in Figure 9 and Equation 1. Equation 11 can be used to compute a value for R_2 after the Power/Platform Management device's input leakage current (I_3) is calculated using Equation 12.

$$R_2 = \frac{V_S + abs(V_M)}{I_1 - I_3} \tag{11}$$

$$I_3 = \frac{V_T}{R_{IN}} \tag{12}$$

Example 6: Monitoring -12 V with the POWR1014/A

In this example, an POWR1014/A is used to monitor a negative 12 V supply. The POWR1014/A is powered by a 3.3 V supply that will be used as the reference voltage and the 1.204 V trip point will be used. A target monitor current of 1mA is selected and Equation 10 is used both to estimate a resistor value for R_1 and to compute its actual current I_1. Equation 12 is used to compute the VMON input current, then an exact value for R_2 is calculated from Equation 11.

Given:
    V_M = -12 V
    V_S = +3.3 V
    V_T = 1.204 V
    I_1 = 1 mA
    R_{IN} = 100,000 Ω

Calculated:
    R_1 = 2096 Ω
    I_1 = 979 uA
    I_3 = 18.5 uA
    R_2 = 15,628 Ω

The closest standard 1% resistor value for R_1 is 2.10kΩ and for R_2 is 15,820Ω. The hysteresis scales by the V_M to V_T voltage ratio (12:1.2) and is 140 mV at the divider input.

Monitoring Negative Voltages Using an Op Amp

Another way to monitor negative voltages is to use an op-amp to invert the signal for the Power/Platform Management device. Figure 10 shows an op-amp in that classical configuration with a negative voltage gain that is the ratio of the feedback resistor divided by the input resistance (R_2/R_1). The output resistor R_3 in conjunction with the protection diode D_1 limits the range of voltage to the VMON input to a safe level. If the monitor voltage is ever above ground, the op-amp output will go negative; thus the protection circuit will clamp to a safe -0.7V limit. Likewise, the protection circuit will clamp the VMON input voltage to the Zener value if the output of the op-amp tries to go too positive. For example, this can happen when the positive analog supply +V_A is +12V and either the monitor signal is too negative or the wrong gain is used. The protection resistor R_3 will divide the op-amp output with the VMON input impedance (R_{IN}) and thus should be on the order of a few hundred ohms. Equation 13 is derived from the gain equation for the inverting amplifier and can be used as is to calculate a trip point (V_T) for a given monitor voltage (V_M) and gain. Or, it can be used to solve for the amplifier gain given trip and monitor voltages. If the negative voltage is less than 1 V, the gain can be greater than unity and if the negative voltage is large, the gain can be fractional.

Figure 10. Op-Amp Used to Monitor Negative Voltages
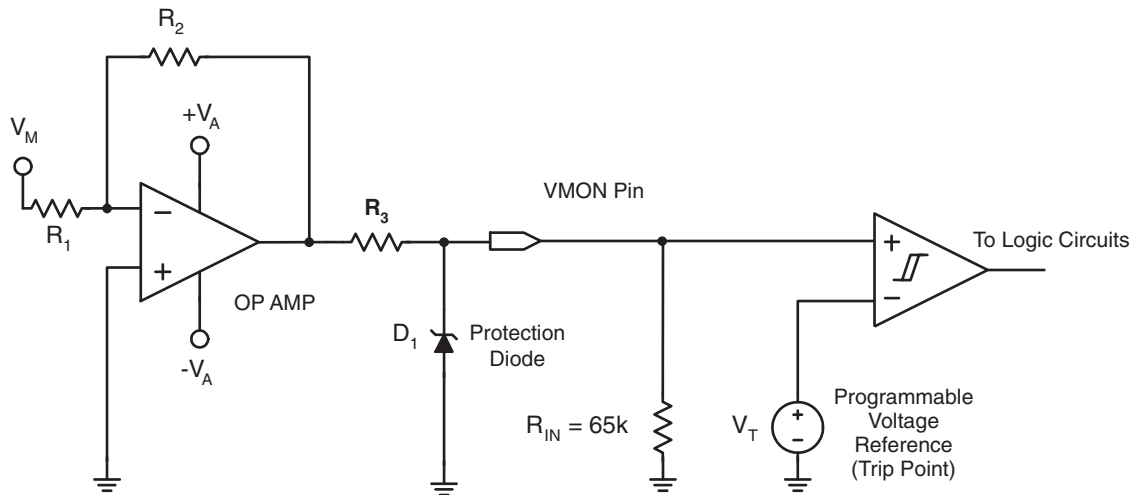
$$V_T = \frac{R_2}{R_1} V_M \tag{13}$$

Example 7: Monitoring -15 V with the POWR1014/A

In this example, an POWR1014/A is used to monitor a -15 V supply. A gain of -1/4.12 will place the op-amp output under the VMON maximum input and a 5 V Zener diode can be used for D_1. The trip point is calculated using Equation 13.

Given:
    V_M = -15
    R_1 = 4.12kΩ
    R_2 = 1kΩ

Calculated:
    V_T = 3.640 V

Using the software, we find there is a trip point at 3.639 V, which will do the job nicely.

Summary

This application note has shown how the Power/Platform Management devices can be used to accurately monitor a wide range of power supplies and voltages. Specifically, power supplies that exceed the maximum input limits and voltages near ground can be monitored using either resistor dividers or op-amps. The basic concepts of comparators and hysteresis have also been reviewed. It has been emphasized that the effective trip point voltage obtained with a low impedance divider is immune to the variations of the VMON analog input resistance. It was also shown how easy it is to select and set the Power/Platform Management device VMON trip points to a desired value using the PAC-Designer interface. With the techniques outlined in this application note, one can be confident that any Power/Platform Management device can be used to monitor and sequence power supplies on boards and in systems with practically no limit placed on the voltage level or polarity.

Related Literature

- DS1034, ProcessorPM-POWR605 Data Sheet

- DS1011, ispPAC-POWR607 Data Sheet

- DS1014, ispPAC-POWR1014/A Data Sheet

- DS1015, ispPAC-POWR1220AT8 Data Sheet

- DS1036, Platform Manager Data Sheet

- DS1043, Platform Manager 2 Data Sheet

- DS1042, L-ASC10 Data Sheet

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Date	Version	Change Summary
March 2016	2.4	Updated Introduction section. Added information on HIMONN_HVMON input.
		Updated Technical Support Assistance section.
August 2014	2.3	Updated to include Platform Manager 2 devices.
		Updated corporate logo.
November 2011	02.2	Updated to cover a broader range of Power/Platform Management devices.
March 2011	02.1	Added note to Introduction section.
—	—	Previous Lattice releases.

Appendix A. Analysis of Variation

In this appendix, we take a closer look at component variations both external and internal, and how they affect the accuracy of the voltage to be monitored. The VMON input resistance is fabricated in silicon (on the Power/Platform Management device) and is thus subject to typical process variations that result in the ±15% deviation from nominal. The variation in the external resistors is also a result of manufacturing process, but is limited to ±1% by testing and sorting. Table 4 was generated using the Equation 14 (derived from Equation 2) and the +12V monitor example from the text.

$$V_M = V_T \left[R_1 \left(\frac{R_2 + R_{IN}}{R_2 R_{IN}} \right) + 1 \right] \tag{14}$$

The bottom row of Table 4 reveals the effect of variations in resistances and the columns are arranged to highlight which resistances are varied. The "Nominal" column (center) lists the nominal resistance values that result in the nominal monitor voltage (V_M) of 12.05V. The "Depressed" and "Elevated" columns (just to the left and just to the right of the nominal column) show how little the +15% and -15% change in R_{IN} modify the monitor voltage, only -20mV and +30mV respectively.

Table 4. Effective Monitor Voltages Resulting from Resistor Variations

Parameter	Effective Trip Point at the Divider Input				
	Low	**Depressed**	**Nominal**	**Elevated**	**High**
R_1 (Ω)	8,781	8,870	8,870	8,870	8,959
R_2 (Ω)	1,010	1,000	1,000	1,000	990
R_{IN} (Ω)	75,000	75,000	65,000	55,000	55,000
V_T (V)	1.205	1.205	1.205	1.205	1.205
V_M (V)	**11.82**	**12.03**	**12.05**	**12.08**	**12.03**

The "Low" column shows what happens to the monitor voltage in one extreme worst-case and the "High" column is for the reciprocal worst-case. For the "Low" column, R_1 is 1% low, R_2 is 1% high, and R_{IN} is 15% high. This results in -230mV change from nominal. For the "High" column, R_1 is 1% high, R_2 is 1% low, and R_{IN} is 15% low. This results in a + 250mV change form the nominal.

In conclusion of this case, variations in the external 1% components have a greater influence upon the effective monitor voltage than the 15% variations of the VMON input resistance. Thus, by proper selection of external resistor values (R_2 in the 1kΩ range), the variability of R_{IN} is effectively moot.

To improve the accuracy of this circuit one could use 0.1% resistors for the external divider networks. Note that the usual statistical analysis of tolerance stack up is performed using root-mean-square (RMS) values, as the random selection of components will rarely result in a case of peak-to-peak error accumulation. We used a peak-to-peak analysis here to emphasize the possible range in values and to show that by proper selection of external resistors (R_1 and R_2) the effect of variations of R_{IN} can be minimized.