



CrossLinkPlus Hardware Checklist

Technical Note

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
DDR	Double Data Rate
ESR	Equivalent Series Resistance
FB	Ferrite Bead
FPGA	Field-Programmable Gate Array
I ² C	Inter-Integrated Circuit
LDO	Low Drop-out
LVDS	Low-Voltage Differential Signaling
PCB	Printed Circuit Board
PLL	Phase Locked Loop
Rx	Receiver
SPI	Serial Peripheral Interface

1. Introduction

When designing complex hardware using the Lattice Semiconductor CrossLinkPlus™ FPGA, you must pay special attention to critical hardware configuration requirements. This technical note guides you through these critical hardware implementation requirements related to the CrossLinkPlus device. The document does not provide detailed step-by-step instructions, but gives a high-level summary checklist to assist in the design process.

This technical note assumes that you are familiar with the CrossLinkPlus device features as described in [CrossLinkPlus Family Data Sheet \(FPGA-DS-02054\)](#).

The critical hardware areas covered in this technical note include:

- Power supplies as they relate to the CrossLinkPlus power supply rails and how to connect them to the PCB and the associated system
- Configuration mode selection for proper power-up behavior
- Device I/O interface and critical signals

The data sheet includes the functional specification and electrical characteristics for the device.

Topics covered in the data sheet include but are not limited to the following:

- High-level functional overview
- Pinouts and packaging information
- Signal descriptions
- Device-specific information about peripherals and registers
- Electrical specifications

2. Power Supplies

The V_{CC} , V_{CCAUX} , and V_{CCIO0} power supplies determine the CrossLinkPlus internal Power Good condition. These supplies need to be at a valid and stable level before the device becomes operational. All other supplies are not monitored during power-up, but need to be at valid and stable level before the device is configured and entered into User Mode. Several other supplies including V_{CCA_DPHY} and V_{CCPLL_DPHY} are used in conjunction with onboard D-PHYs on CrossLinkPlus devices.

Table 2.1 describes the power supplies and the appropriate voltage levels for each supply.

Table 2.1. CrossLinkPlus FPGA Power Supplies

Supply	Voltage (Nominal Value)	Description
V_{CC}	1.2 V	FPGA core power supply. Required for Power Good condition.
V_{CCGPLL}	1.2 V	General Purpose PLL Supply Voltage. Should be isolated from excessive noise.
V_{CCAUX}	2.5 V or 3.3 V	Auxiliary Supply Voltage for Bank 1, Bank 2, and Flash Programming. Required for Power Good condition.
$V_{CCIO[2, 1, 0]}$	1.2 V to 3.3 V	I/O Driver Supply Voltage for Bank 0, Bank 1, or Bank 2. Each bank has its own V_{CCIO} supply: V_{CCIO0} is used in conjunction with pins dedicated and shared with device configuration, and is required for Power Good condition.
$V_{CCA_DPHY[1,0]}$	1.2 V	Analog Supply Voltage for D-PHY. Should be isolated from excessive noise.
$V_{CCPLL_DPHY[1,0]}$	1.2 V	PLL Supply voltage for D-PHY. Should be isolated from excessive noise.

The CrossLinkPlus FPGA device has a power-on-reset state machine that depends on several of the power supplies. These supplies should come up monotonically. A power-on-reset counter begins to count after V_{CC} , V_{CCAUX} , and V_{CCIO0} reach the levels defined in the Power-On-Reset Voltage Levels section of [CrossLinkPlus Family Data Sheet \(FPGA-DS-02054\)](#). Initialization of the device does not proceed until the last power supply has reached its minimum operating voltage.

2.1. Power Noise

The power rail voltages of the FPGA allow for a worst-case normal operating tolerance of $\pm 5\%$ of these voltages. The 5% tolerance includes any noises.

2.2. Power Source

It is recommended that the designed voltage regulators are accurate to within 3% of the optimum voltage to allow power noise design margin.

When calculating the voltage regulator total tolerance, include:

- Regulator voltage reference tolerance
- Regulator line tolerance
- Regulator load tolerance
- Tolerances of any resistors connected to regulator feedback pin which sets regulator output voltage
- Expected voltage drops due to power filtering ferrite bead's ESR * expected current draw
- Expected voltage drops due to current measuring resistor's ESR * expected current draw

With 3% tolerance allocated to the voltage source, the design can have a remaining 2% tolerance for noise and layout related issues. The 1.2 V rail is especially sensitive to noise as every 12 mV is 1% of the rail voltage. For high-speed differential power rails, it is recommended to target a maximum 1% peak noise. For PLLs, target less than 0.5% peak noise.

CrossLinkPlus is a low current device. When possible, use LDO regulators instead of Switchers to help reduce noise and ripple.

3. CrossLinkPlus MIPI D-PHY and PLL Power Supplies

Supplies dedicated to the operation of the CrossLinkPlus MIPI® D-PHY include V_{CCA_DPHYx} and V_{CCPLL_DPHYx} . These pins are also paired with dedicated ground pins including $GNDA_DPHYx$ and $GNDPLL_DPHYx$. These supplies should be decoupled with adequate bypass capacitors between these pins, close to the device package.

The V_{CCGPLL} provides a quiet supply for the general purpose PLL while the V_{CCPLL_DPHYx} and V_{CCA_DPHYx} provide a quiet supply for the critical MIPI D-PHY blocks. For the best jitter performance, careful pin assignment can keep noisy I/O pins away from sensitive functional pins. The leading causes of PCB related MIPI D-PHY crosstalk is related to FPGA outputs located in close proximity to the sensitive MIPI D-PHY power supplies. These supplies require cautious board layout to ensure noise immunity to the switching noise generated by FPGA outputs. Guidelines are provided to build quiet filtered supplies for the analog supplies. However, robust PCB layout is required to ensure that noise does not infiltrate into these analog supplies.

3.1. Recommended Power Filtering Groups and Components

Table 3.1. Recommended Power Filtering Groups and Components

Power Input	Recommended Filter	Notes
V_{CC}	$0\ \Omega + (4.7\ \mu\text{F or } 10\ \mu\text{F}) + 100\ \text{nF per pin}$	For switching regulators or noise sensitive designs, change $0\ \Omega$ to $120\ \Omega$ FB.
V_{CCIOx}	$120\ \Omega$ or $220\ \Omega$ FB + $2.2\ \text{nF} + 100\ \text{nF per pin}$	For heavy current/capacitive loads, use $120\ \Omega$ FB with $\text{ESR} \leq 0.2\ \Omega$.
V_{CCA_DPHYx}	$120\ \Omega$ FB + $2.2\ \mu\text{F} + 100\ \text{nF per pin}$	If DPHYx is not used, it can be unpowered; or remove $2.2\ \mu\text{F}$ and change FB to $0\ \Omega$.
V_{CCPLL_DPHYx}	120 to $330\ \Omega$ FB + $2.2\ \mu\text{F} + 100\ \text{nF per pin}$	If DPHYx is not used, it can be unpowered; or remove $2.2\ \mu\text{F}$ and change FB to $0\ \Omega$.
V_{CCGPLL}	120 to $330\ \Omega$ FB + $1.0\ \mu\text{F} + 100\ \text{nF}$	If GPLL is not used, $1.0\ \mu\text{F}$ can be removed and change FB to $0\ \Omega$.
V_{CCAUX}	$0\ \Omega + 1.0\ \mu\text{F}$	For switching regulators or noise sensitive designs, change $0\ \Omega$ to $120\ \Omega$ FB.

3.1.1. Ferrite Bead Notes

- PLL rails are low current which allow ferrite beads with $\text{ESR} \leq 0.3\ \Omega$.
- Non-PLL rails should use ferrite beads with $\text{ESR} \leq 0.1\ \Omega$.
- Use $120\ \Omega$ @100 MHz ferrite beads on banks with heavy current or capacitive loads.
- Prefer 0402 size ferrite beads due to lower available ESR and lower cost compared to 0201 size.

3.1.2. Unused Bank V_{CCIOx} and V_{CCGPLL}

- Connect unused V_{CCIOs} to a power rail. Do not leave unused V_{CCIOs} open.
- Connect unused V_{CCGPLL} to V_{CC} power rail. Do not leave unused V_{CCGPLL} open.

3.1.3. Unused DPHY banks

For unused $DPHYx$, banks V_{CCA_DPHYx} and V_{CCPLL_DPHYx} can be unpowered.

3.2. Power Sequencing

Improper power sequencing does not damage the chip itself, however, larger current leakages and undefined I/O operation may cause system issues until all rails are properly powered up.

To prevent current leakages and undefined I/O operation during power up, V_{CCIO} supplies should be powered up before or together with the V_{CC} , V_{CCGPLL} , and V_{CCAUX} supplies.

4. Power Estimation

After selecting the CrossLinkPlus package and implementing the design logic, power estimation for the system environment should be determined based on the Power Calculator software provided as part of the Lattice Diamond® design tool. When estimating power, you should keep two goals in mind:

- Power supply budgeting should be based on the maximum of the power-up in-rush current, configuration current, or maximum DC and AC current for the given system environmental conditions.
- The ability for the system environment and CrossLinkPlus device packaging to be able to support the specified maximum operating junction temperature.

By determining these two criteria, the CrossLinkPlus device power requirements can be taken into account early in the design phase.

5. Configuration Considerations

The CrossLinkPlus device includes provisions to configure the FPGA from a processor via Slave I²C or Slave SPI, Master SPI from an external SPI Flash, or internally from Flash.

The use of external resistors is always needed if the configuration signals are being used to handshake to other devices. For Master SPI mode, the MCK pin must be connected to a serial 30 Ω resistor placed close to the CrossLinkPlus device package to prevent reflections or glitches during Master SPI configuration. 4.7 kΩ pull-up resistors to V_{CCIO0} should be used on the following pins (Table 5.1).

Table 5.1. Required Pull-up Resistors for Configuration Pins

Pin	PCB Connection
CRESET_B	4.7 kΩ Pull-up to V _{CCIO0}
CDONE	4.7 kΩ Pull-up to V _{CCIO0}
SDA	Strong Pull-up (Open Drain Signal)*
SCL	Strong Pull-up (Open Drain Signal)*
SPI_SS	4.7 kΩ Pull-up to V _{CCIO0} (Open Drain Signal)
MCK	30 Ω Serial Resistor close to CrossLinkPlus package

*Note: Pull-up value on I²C signals is dependent on the I²C bus characteristics and programming speed. Typical values are between 2.2 kΩ and 4.7 kΩ.

Table 5.2. Configuration Pins Needed per Programming Mode

Configuration Mode	Clock		Shared Pins	Dedicated Pins
	Pin	I/O		
SSPI	SPI_SCK	Input	MISO, MOSI, SPI_SS	CRESET_B
MSPI	MCK	Output	MISO, MOSI, CSN	CRESET_B
I2C	SCL	Input	SDA	CRESET_B

CrossLinkPlus uses the non-volatile Feature Row to select the configuration modes. You can configure CrossLinkPlus Feature Row through Diamond Spreadsheet View. See [CrosslinkPlus Programming and Configuration Usage Guide \(FPGA-TN-02103\)](#) for details.

6. Power Management Unit

The CrossLinkPlus device includes a dedicated Power Management Unit which may place the fabric and other on-chip resources into sleep mode. The CrossLinkPlus device includes a dual function pin called PMU_WKUPN. This pin is active low and may be used to wake-up the device from sleep mode. A weak pull-up resistor (10 kΩ – 100 kΩ) is recommended when the pin is assigned to the wakeup function.

7. Clock Inputs

The CrossLinkPlus device provides primary clock input pins, which are shared function pins that can also be used as general purpose I/O. When these pins are used for clocking purpose, you need to pay attention to minimize signal noise on these pins.

8. Pinout Considerations

The CrossLinkPlus device is designed to support high-speed video interface bridging. This includes various rule-based pinouts that need to be understood prior to implementation of the PCB design. The pinout selection must be completed with an understanding of the interface building blocks of the FPGA fabric. These include I/O Logic blocks such as DDR, clock resource connectivity and PLL usage. Refer to [CrossLinkPlus High-Speed I/O Interface \(FPGA-TN-02102\)](#) for rules pertaining to these interface types.

8.1. LVDS Pinout Considerations

True LVDS inputs and outputs are available on I/O pins in Banks 1 and 2. These multi-function I/O pins support LVDS, LVCMOS, subLVDS, SLVS, and MIPI D-PHY receive functions. The I/O buffers are described in [CrossLinkPlus sysI/O Usage Guide \(FPGA-TN-02108\)](#).

8.2. MIPI D-PHY Interface Considerations

Although coupling has been reduced in the CrossLinkPlus device packages to minimize crosstalk, the PCB board can cause significant noise injection from any I/O pin adjacent to MIPI D-PHY data, reference clock, and power pins as well as other critical I/O pins such as clock signals. PCB traces running in parallel for long distances need careful analysis. Simulate any suspicious traces using a PCB crosstalk simulation tool to determine if they can cause problems.

High-speed signaling requires careful PCB stackup and layout. Maintaining good transmission line characteristics and impedance controlled routing are must requirements to achieve high bandwidth performance. A solid ground reference plane shall be maintained underneath of high-speed signals. This includes tightly matched differential routing with very few discontinuities. Matching between the D-PHY clock and data pairs is especially critical. Refer to [High-Speed PCB Design Considerations \(TN1033\)](#) for suggested methods and guidance.

Implement the guidelines listed in the following table for I/O placement when MIPI Rx inputs are present on the programmable I/O banks to ensure optimal fabric performance:

Configuration	Bank 1	Bank 2
SLVS200/MIPI Rx on Bank 1	No LVCMOS Outputs	No LVCMOS Outputs
SLVS200/MIPI Rx on Bank 2	No LVCMOS Outputs	No LVCMOS Outputs
SLVS200/MIPI Rx on Bank 1 & Bank 2	No LVCMOS Outputs	No LVCMOS Outputs

9. Checklist

Table 9.1. Checklist Table

	Item	OK	NA
1	FPGA Power Supplies		
1.1	V _{CC} core voltage @ 1.2 V ±5%		
1.1.1	Use a PCB plane for V _{CC} core voltage with proper decoupling.		
1.1.2	V _{CC} core supply sized to meet power requirement calculation from software.		
1.2	V _{CCGPLL} @ 1.2 V ±5%		
1.2.1	V _{CCGPLL} isolated from excessive noise.		
1.2.2	V _{CCGPLL} pins should be ganged together and a solid PCB plane is recommended. This plane should not have adjacent non-MIPI D-PHY signals passing above or below. It should also be isolated from the V _{CC} core power plane.		
1.3	All V _{CCIO} voltages are between 1.2 V to 3.3 V		
1.3.1	V _{CCIO0} voltage matches external configuration interfaces (that is memory devices).		
1.3.2	V _{CCIO0} , V _{CCIO1} , V _{CCIO2} voltage based on user design.		
1.4	V _{CCAUX} @ 2.5 V ±5% or @ 3.3 V ±5%		
2	MIPI D-PHY Power Supplies		
2.1	V _{CCA_DPHY0} and V _{CCA_DPHY1} @ 1.2 V ±5%. Should be ganged together and a solid PCB plane is recommended. This plane should not have adjacent non-MIPI D-PHY signals passing above or below. It should also be isolated from the V _{CC} core power plane.		
2.2	V _{CCPLL_DPHYX} @ 1.2 V ±5% should be isolated.		
3	Configuration/Power Management Unit		
3.1	Pull-ups and pull-downs on configuration specific pins as given in Table 5.1 .		
3.2	V _{CCIO0} bank voltage matches sysCONFIG peripheral devices such as SPI Flash.		
3.3	When PMU_WKUPN is used to wake up CrossLinkPlus, an external weak pull-up resistor (10K – 100K) is recommended.		
4	MIPI D-PHY		
4.1	Dedicated reference clock input from clock source meets the DC and AC requirements.		
4.2	Maintain good high-speed transmission line routing.		
4.2.1	Continuous ground reference plane to serial channels.		
4.2.2	Length matched differential traces.		
4.2.3	Do not pass other signals on the PCB above or below the high-speed MIPI D-PHY signals traces without isolation.		
4.2.4	Keep non-MIPI D-PHY signal traces from passing above or below the 1.2 V V _{CCA_DPHYX} power plane without isolation.		
5	Critical Pinout Selection		
5.1	Pinout has been chosen to address FPGA resource connections to I/O logic and clock resources per CrossLinkPlus High-Speed I/O Interface (FPGA-TN-02102) .		
5.2	Ensure FPGA PLL, MIPI D-PHY PLL, and clock inputs are assigned to the proper pins. Refer to the CrossLinkPlus Family Data Sheet (FPGA-DS-02054) for details of the device.		
6	I²C		
6.1	2.2 kΩ – 4.7 kΩ Pull-up on open drain signals SCL and SDA.		

References

For more information, refer to the following documents:

- [CrossLinkPlus Family Data Sheet \(FPGA-DS-02054\)](#)
- [CrossLinkPlus High-Speed I/O Interface \(FPGA-TN-02102\)](#)
- [CrossLinkPlus Programming and Configuration Usage Guide \(FPGA-TN-02103\)](#)
- [CrossLinkPlus sysCLOCK PLL/DLL Design and Usage Guide \(FPGA-TN-02109\)](#)
- [CrossLinkPlus sysI/O Usage Guide \(FPGA-TN-02108\)](#)
- [CrossLinkPlus Memory Usage Guide \(FPGA-TN-02110\)](#)
- [Power Management and Calculation for CrossLinkPlus Device \(FPGA-TN-02111\)](#)
- [CrossLinkPlus I²C Hardened IP Usage Guide \(FPGA-TN-02112\)](#)
- [Advanced CrossLinkPlus I²C Hardened IP Reference Guide \(FPGA-TN-02135\)](#)
- [High-Speed PCB Design Considerations \(TN1033\)](#)
- [Power Decoupling and Bypass Filtering for Programmable Devices \(TN1068\)](#)

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 1.0, August 2019

Section	Change Summary
All	Production release.

