Driving High-Current LEDs with iCE65 FPGAs

SiliconBlue™

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Summary

LEDs are everywhere. The flexible I/O design of the iCE65 FPGA family is capable of directly driving many types of LEDs, including high-current LEDs. If an LED requires more drive current than a single I/O can provide, it is possible to gang multiple I/Os to achieve the required drive current. The method described in this document eliminates the need for discrete driver devices, thereby reducing total system cost.

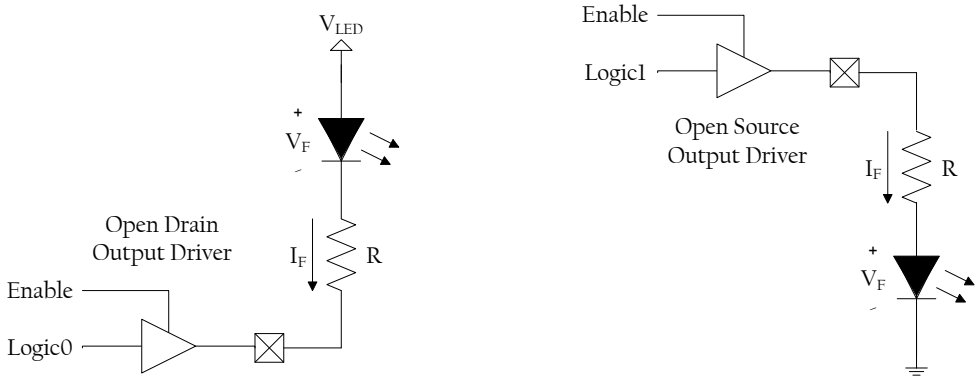
Introduction

LEDs are ubiquitous and used in a variety of applications for indication, illumination, and lighting. As an example, consider a typical cellular phone as shown in Figure 1, in which LEDs are used for all these purposes. Cellular network connectivity status is often indicated using a small, low brightness, single-color LED. Keypads are illuminated using multiple, moderate brightness, single- or multi- color LEDs. Displays are also lighted using multiple, high brightness, white LEDs.

Figure 1: **Ubiquitous Indication, Illumination and Lighting**

Although discrete LED driver devices are commercially available, they are not necessary in most applications. There are several methods to directly drive LEDs using the flexible I/O design of the iCE65 FPGA family. The most common method for directly driving an LED is the use of an open drain output driver. Open source output drivers may also be used. These are shown in Figure 2, constructed using iCE65 FPGA programmable I/O pins.

Figure 2: **Driving an LED with an Open Drain or Open Source Output Driver**



Open drain outputs are only capable of pulling the pin low. The relevant attributes for an open drain output driving an LED are its I/O Standard, the LED Supply Voltage V_{LED}, $V_{OL(MAX)}$, and $I_{OL(MIN)}$. Typically, the LED Supply Voltage is the same as the I/O Supply Voltage, V_{CCIO}. It is possible to use a different V_{LED} value as long as V_{LED} remains within the range specified in the absolute maximum parameter table for iCE65 FPGA pin voltage in the iCE65 FPGA datasheet. Table 1 lists recommended iCE65 FPGA open drain output configurations and their relevant electrical characteristics.

Table 1: **Recommended iCE65 FPGA Open Drain Output Configurations**

I/O Bank	Nominal V_{CCIO}	I/O Standard	$V_{OL(MAX)}$	$I_{OL(MIN)}$	$V_{LED(MAX)}$
0, 1, 2, and SPI	3.3V	SB_LVCMOS	0.4V	11 mA	5.5V
	2.5V	SB_LVCMOS	0.4V	8 mA	5.5V
	1.8V	SB_LVCMOS	0.4V	5 mA	5.5V
3	2.5V	SB_LVCMOS25_16	0.4V	16 mA	3.0V
	1.8V	SB_LVCMOS18_10	0.4V	10 mA	2.3V

Conversely, open source outputs are only capable of pulling the pin high. The relevant attributes for an open source output driving an LED are its I/O Standard, the I/O Supply Voltage V_{CCIO}, $V_{OH(MIN)}$, and $I_{OH(MIN)}$. Table 2 lists recommended iCE65 FPGA open source output configurations and their relevant electrical characteristics.

Table 2: **Recommended iCE65 FPGA Open Source Output Configurations**

I/O Bank	Nominal V_{CCIO}	I/O Standard	$V_{OH(MIN)}$	$I_{OH(MIN)}$
0, 1, 2, and SPI	3.3V	SB_LVCMOS	2.6V	12 mA
	2.5V	SB_LVCMOS	1.9V	9 mA
3	2.5V	SB_LVCMOS25_16	1.9V	16 mA

Historically, open drain outputs have been the preferred method because TTL output drivers can sink more current than they can source. Many recent CMOS devices, including the iCE65 FPGA family, are capable of pulling the pin high and low equally well.

Even so, an open drain approach facilitates using an LED Supply Voltage, V_{LED}, which is higher than the I/O Supply Voltage. With this in mind, Table 1 includes 1.8V I/O Standards as they can be used effectively with V_{LED} voltages higher than 1.8V. To accomplish an equivalent effect with an open source approach would require a negative, low voltage power rail that is unlikely to exist in most systems.

Other attributes of interest are the forward voltage, V_F, of the LED at the recommended current, I_F. These values are specified on the LED datasheet, and are often accompanied by a graph of the current versus voltage behavior for the LED (the IV curve of the LED).

The value of the resistor shown in Figure 2 is calculated to set the desired current through the LED.

LED Biasing Requirements

In order for the output driver to forward bias the LED, the output driver must be capable of generating V_F across the LED to achieve adequate intensity. One of the following, based on the selected circuit, must be true:

Open-Drain

Equation 1

$$V_{LED} - V_{OL(MAX)} > V_F$$

Open Source

Equation 2

$$V_{OH(MIN)} > V_F$$

If the relationship is not satisfied, consider using:

- A different LED Supply Voltage (higher V_{LED})
- A different I/O Standard (lower $V_{OL(MAX)}$ or higher $V_{OH(MIN)}$)
- A different operating point on the IV curve of the LED (lower V_F and lower I_F)
- A different LED device (a different IV curve with lower V_F and lower I_F)

LED Current Drive Requirements

In order for the output driver to forward bias the LED, the output driver must have a current capability that meets or exceeds the desired I_F through the LED. One of the following, based on the selected circuit, must be true:

Open-Drain

Equation 3

$$I_{OL(MIN)} > I_F$$

Open Source

Equation 4

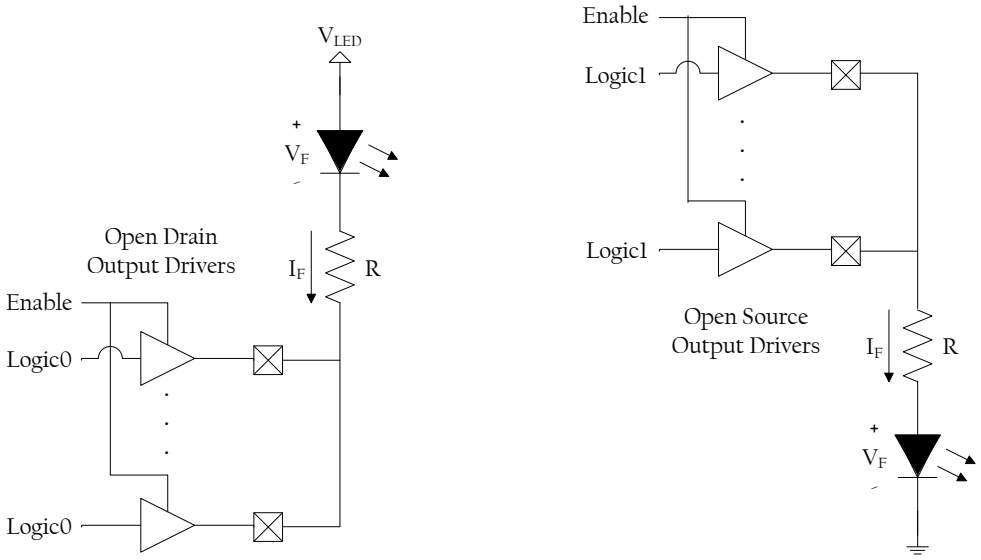
$$I_{OH(MIN)} > I_F$$

If the relationship is not satisfied, consider using:

- A different operating point on the IV curve of the LED (lower V_F and lower I_F)
- A different LED device (a different IV curve with lower V_F and lower I_F)
- Multiple I/O (effectively increasing $I_{OL(MIN)}$ or $I_{OH(MIN)}$)

The last option is especially attractive in applications where high current is required. It is possible to increase the effective $I_{OL(MIN)}$ or $I_{OH(MIN)}$, using multiple output drivers, by connecting them in parallel outside the iCE65 FPGA device. This is shown in Figure 3.

Figure 3: **Increasing the Effective Open Drain or Open Source Drive Current**



Calculate the number of output drivers required by dividing the I_F current for the LED by either the $I_{OL(MIN)}$ or $I_{OH(MIN)}$ current for the iCE65, using the next highest integer. The effective $I_{OL(MIN)}$ or $I_{OH(MIN)}$ is the sum of the individual pin contributions. It is safe to connect open-drain or open-source output drivers in parallel because a crowbar current cannot occur; the ganged output drivers never conflict.

Number of Ganged Outputs Required

Use Equation 5 or Equation 6 to determine the minimum recommended number of pins to drive the LED.

Open-Drain Outputs

Equation 5

$$Number\_of\_Pins = CEILING\left(\frac{I_F}{I_{OL(MIN)}}\right)$$

Open-Source Outputs

Equation 6

$$Number\_of\_Pins = CEILING\left(\frac{I_F}{I_{OH(MIN)}}\right)$$

Calculating the Resistor Value

Open-Drain Outputs

For open-drain implementations using one or more pins, select a standard resistor value that satisfies Equation 7.

Equation 7

$$R \geq \frac{V_{LED} - V_{OL(MAX)} - V_F}{I_F}$$

Open-Source Outputs

For open-source implementations using one or more pins, select a standard resistor value that satisfies Equation 8.

Equation 8

$$R \geq \frac{V_{OH(MIN)} - V_F}{I_F}$$

A Practical Example

As a practical example, consider the Lumex SML-LX0603IW-TR high brightness LED. This LED exhibits a typical V_F of 2.0V at an I_F of 20 mA. Use SB_LVCMOS open drain driver(s) located in Bank 1 with $V_{CCIO} = V_{LED} = 3.3V$. The following attributes are obtained from Table 1:

- $V_{OL(MAX)} = 0.4V$
- $I_{OL(MIN)} = 11$ mA

The development of a solution is discussed below. The resulting solution is evaluated on an iCE65 Evaluation Kit.

Check LED Biasing

Check Equation 1 for an open-drain output, is the LED biasing requirement met? Using the relevant values, the biasing conditions are indeed met, as shown in Equation 9.

Equation 9

$$3.3V - 0.4V > 2.0V$$

Calculate the Number of Pins Required

Using Equation 5 for an open-drain output, calculate the minimum number of pins required to drive the LED. As indicated by Equation 10, two pins are required to drive this high-current LED at its rated current.

Equation 10

$$CEILING\left(\frac{20\ mA}{11\ mA}\right) = CEILING(1.82) = 2$$

Calculate the Value for the Current-Limiting Resistor

Using Equation 7 for an open-drain output, calculate the value for the current-limiting resistor. The result appears in Equation 11. Select a standard resistor with a value greater than or equal to the calculated value.

Equation 11

$$R \geq \frac{V_{LED} - V_{OL(MAX)} - V_F}{I_F} = \frac{(3.3V - 0.4V - 2.0V)}{20\ mA} = 45.0\Omega$$

Create the Design Source Code

As indicated by Equation 10, two open-drain outputs are required to drive the LED. The output pins must be ganged together as shown in Figure 3. The following code examples illustrate how to generate the required output pins in Verilog and VHDL. The LED illuminates when signal `turn_on` is logic one.

Verilog

```
module driveled (
  input  wire       turn_on,
  output wire       open_drain_driver0,
  output wire       open_drain_driver1
  );

  assign open_drain_driver0 = turn_on ? 1'b0 : 1'bz;
  assign open_drain_driver1 = turn_on ? 1'b0 : 1'bz;

endmodule
```

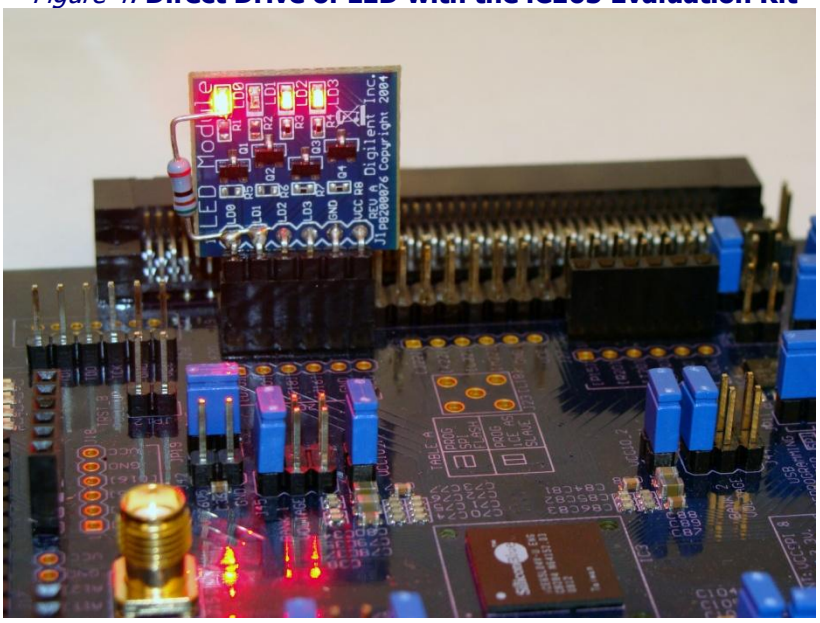
VHDL

```
library ieee;
use ieee.std_logic_1164.all;

entity driveled is port (
  turn_on: in std_logic;
  open_drain_driver0: out std_logic;
  open_drain_driver1: out std_logic);
end entity driveled;

architecture appnote of driveled is
  signal logic0 : std_logic;
begin
  logic0 <= '0';
  open_drain_driver0 <= logic0 when (turn_on = '1') else 'Z';
  open_drain_driver1 <= logic0 when (turn_on = '1') else 'Z';
end architecture appnote;
```

Evaluate the Complete Solution

Figure 4 shows an implementation of the complete solution using a modified PMOD module plugged into an iCE65 Evaluation Kit. The leftmost LED has been isolated from the discrete driver on the PMOD module and is driven by two ganged open-drain pins on the iCE65 FPGA. The resistor used is 51Ω. The measured V_F is 1.94V, confirming the validity of the calculations.

Figure 4: **Direct Drive of LED with the iCE65 Evaluation Kit**



The two rightmost LEDs, driven by discrete drivers, are illuminated for comparison purposes. The optical output is comparable. The direct drive solution reduces total system cost by a reducing the component count and board area.

Conclusion

The flexible I/O design of the iCE65 FPGA family can be used to directly drive many types of LEDs. Where high current is required, multiple open drain or open source output drivers can be safely connected in parallel. Using the techniques in this application note, discrete LED driver devices can be eliminated, reducing total system cost.

References

The following references were used in the creation of this application note:

- Lumex, Incorporated. "SML-LX0603IW-TR Surface Mount 635nm Red LED" datasheet (22-JUL-1997).
- SiliconBlue Technologies, Incorporated. "Handheld iCE: iCE65 Ultra Low-Power Programmable Logic Family" datasheet (10-OCT-2008).
- Wakerly, John. "Digital Design Principles and Practices Third Edition, Updated" New Jersey: Prentice Hall, Incorporated, 2001.

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Revision History

Version	Date	Description
1.3	23-DEC-2008	Updated corporate contact information.
1.2	17-OCT-2008	Initial public release, electrical data synchronized with product datasheet.
1.1	12-SEP-2008	First draft.

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