Boundary Scan Testability with Lattice's sysIO Capability

July 2001 Application Note AN8066

Introduction

The number of I/O interface standards used on a board or in a system has increased. In the not too distant past, virtually all of the signals running around a board were compatible with one of the JEDEC LVCMOS standards. These standards, though robust, did not always meet the requirements for high speed, low noise systems so additional standards were developed to meet those needs. Programmable logic devices have kept pace with those newer standards by offering them as programmable features on I/O and input pins. Lattice's ispMACH™ 5000VG family of devices offers the ability to interface with several different I/O interface standards through its sysIO™ capability.

With this ability to change the physical characteristics of an I/O, comes the need to provide for Boundary Scan Test at the board and system levels. This application note describes how to perform Boundary Scan Test on devices with sysIO capability.

Ratioed Interface Standard I/Os and Inputs

There are three classes of interface standards that can be implemented on devices with sysIO capability. The first is the traditional ratioed interfaced standard. This type of interface standard is single-ended and does not require any kind of reference voltage. The JEDEC LVCMOS standards and PCI are examples of ratioed interface standards. With both PCI and the JEDEC LVCMOS standards there are different voltage ranges over which each of the individual standards operates. With LVCMOS there are 1.5V, 1.8V, 2.5V, 3.3V and 5V standards, each with its own V_{IL}/V_{IH} and V_{OL}/V_{OH} levels. In some instances there is interoperability between the different levels such as between devices operating at 3.3V and others operating at 5V and in this case there is no issue when performing Boundary Scan Test on an unprogrammed device. In other instances, the output drive levels for one standard will be incompatible with the receive levels for another such as with 3.3V devices being driven by 1.8V devices. For example, if an input on an unprogrammed device is set to operate with 3.3V levels but is being driven by a 1.8V device, then the device must first be configured so that the input is set to operate with 1.8V levels before a Boundary Scan Test can be run

Referenced Interface Standard I/Os and Inputs

The second type of interface standard is a referenced standard where input levels are compared to a given reference voltage. This standard is a single-ended standard and uses a comparator as the input buffer. In a programmable logic device, there will be a single I/O pin that is converted to be the reference voltage (V_{REF}) input pin. This pin is, by nature, an analog pin and cannot be tested through traditional Boundary Scan Test methods. This behavior must be accounted for in both the Boundary Scan Description Language (BSDL) file and in the board or system level netlist used to generate connectivity test vectors.

The BSDL file describes the implementation of the IEEE 1149.1 standard in a given device including the Boundary Scan register (BSR) and how it relates to the device I/Os and inputs. The description of each of the individual registers in the boundary scan register describes the location of the register, its function, its specific configuration, which pin it is connected to, and a "safe" state that should be in the register when it is left unconnected. As an example, the following describes the Boundary Scan registers used to control a single I/O pin.

```
" 127 (BC_7, IO7A( 0), BIDIR,    X, 126, 0,Z)," &

" 126 (BC_2,        *, CONTROL,  0          )," &
```

These two cells are located at positions 127 and 126 in the Boundary Scan register and are the cells used to control pin IO7A(0). The first cell is a bi-directional cell that controls the actual data into and out of the pin while the second cell controls whether the pin is input or an output pin. The value after the cell function is the "safe" state for

that cell. In the case of the "CONTROL" cell the value is a '0' which indicates that if the pin is left unconnected the software should put a '0' into that location. Doing so will tristate the pin.

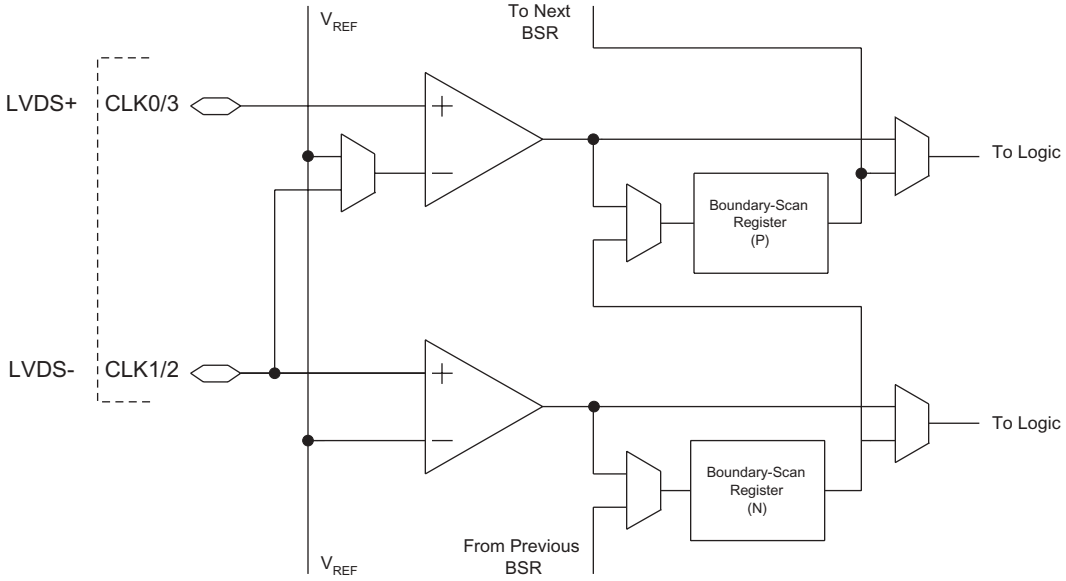
With Lattice devices, pins that can be either I/O pins or VREF pins will have the safe state for the CONTROL cell set to be a '0' in the BSDL file. When the pin is logically unconnected it cannot drive out and affect the level of VREF being driven into the VREF pin. To ensure that any Automatic Test Pattern Generation (ATPG) software does not create test vectors that will drive that pin using the Boundary Scan register it should be left completely unconnected in any netlist used for that software. It must still be physically connected for proper operation.

Differential Interface Standard I/O and Input Pins

The final interface standard type is a differential standard where two pins, a positive input or output and a negative input or output, are required for a single logical connection rather than just one. Differential I/O pins are difficult to test with traditional Boundary Scan Test methods because there is a single Boundary Scan cell capturing data for two discrete signals. This is not an ideal situation because it may not be possible to test for all possible fault conditions involving the two pins. If one of the two pins is stuck either high or low, the fault may be detected but it is virtually impossible to tell which of the two inputs is stuck.

Programmable logic devices create differential I/O pins by converting two single-ended I/Os to a single differential I/O. Figure 1 demonstrates how this is done. Each of the single-ended I/Os has its own Boundary Scan register but in practice only the Boundary Scan register attached to the positive side of the differential I/O is used. When creating test vectors for Boundary Scan Test using ATPG software, the board or system level netlist should only have the positive side of the differential I/O connected. The negative side should be left unconnected because the comparator associated with that pin is unused and data captured into the Boundary Scan register will not be indicative of what is happening at the pin. The Boundary Scan register at the positive side of the I/O will accurately capture and drive pin data.

Figure 1. Differential I/O Configuration



Quick sysIO Programming

Before performing any Boundary Scan Test on devices with sysIO capability it may be required to first configure the physical nature of the I/O pins. This will be required if:

1. Any input, output or I/O in the device is configured to interface with a referenced interface standard or a differential interface standard.
2. Any input configured to be a ratioed interface standard meets different voltage requirements than the default standard for the device. The default interface standard is shown in the device data sheet.

On all devices with sysIO features there is a method for quickly configuring those features without having to configure the entire device. This is important because the time required to configure the entire device will be much longer than the time to program just the sysIO features.

Lattice provides support for quick sysIO programming through its ispVM™ System programming software. Once a chain of devices has been created, the user selects the "Program sysIO" option to create the SVF or ATE file necessary to configure the sysIO features on a board test system. Refer to ispVM System's online help for additional information about how to use this feature.

Conclusion

Today's advanced I/O interface standards provide the ability to transport information around a board or system at higher speeds than ever before. There are issues associated with their use, however, that must be taken into account. One issue is the ability to Boundary Scan Test a system when using these I/O standards. This application note has described and addressed many of these issues. By following the suggestions presented here, it is possible to test a system with a minimal amount of additional effort.

Technical Support Assistance

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