Board Timing Guidelines for the DDR SDRAM Controller IP Core

September 2012 **Technical Note TN1071**

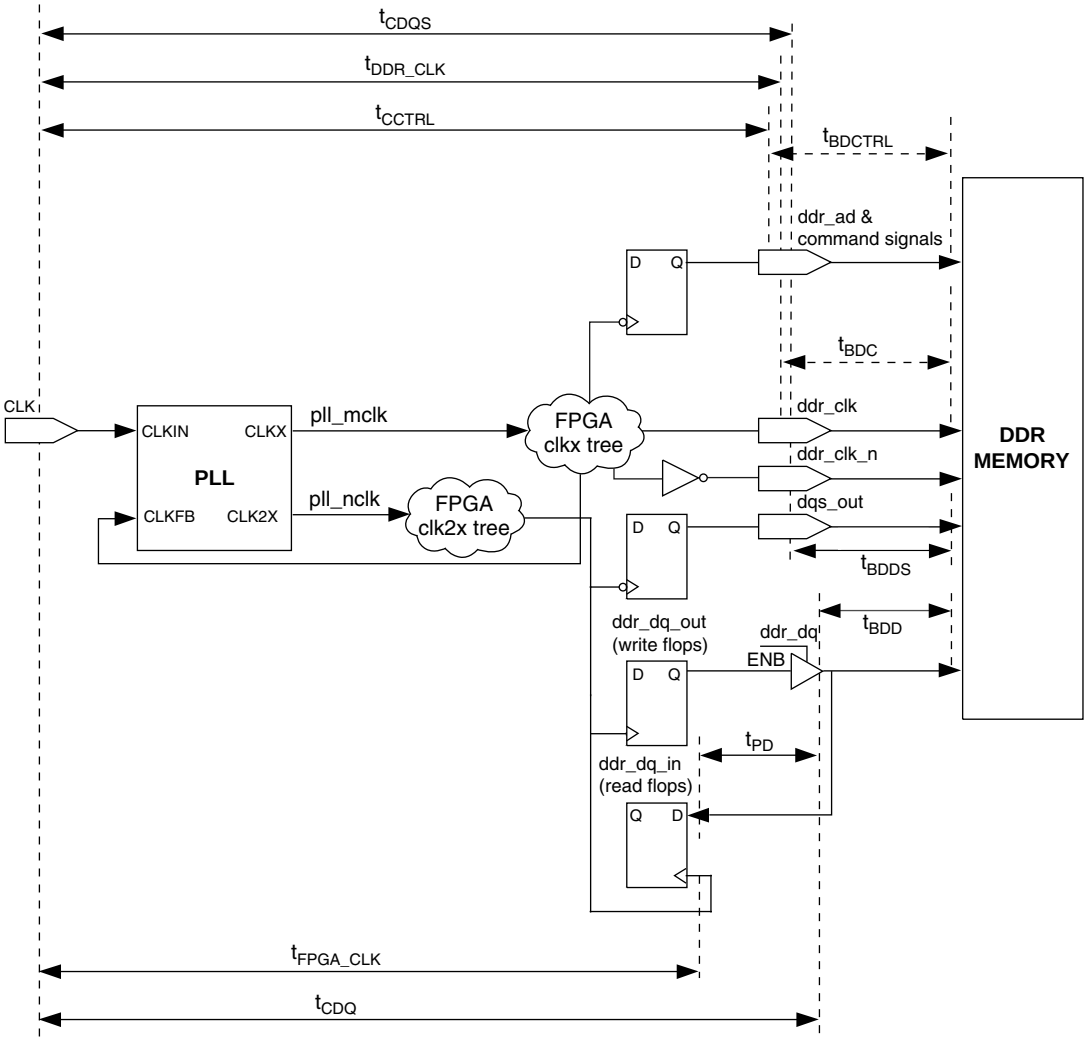
Introduction

This document describes how to meet board timing requirements for DDR signals. The Lattice DDR SDRAM Controller IP core, non-pipelined version (DDR-NP) is used as an example.

Figure 17-1 describes the timing diagram for the DDR signals. A total of five clocks are used in the DDR board design using the Lattice DDR IP core. The following is the clock description:

`clk`:	Input clock for PLL (max. frequency of 133MHz for DDR NP)
`ddr_clk`:	Output clock going to DDR (max. frequency of 133MHz for DDR NP)
`ddr_clk_n`:	Negated version of `ddr_clk`
`pll_mclk (clkx)`:	Same as `ddr_clk`, used inside the FPGA only.
`pll_nclk (clk2x)`:	A 266MHz clock for DDR NP, used inside the FPGA only.

Figure 17-1. DDR Signal Timing Diagram



As shown in Figure 17-1, input to PLL is CLK (133MHz for DDR NP). The PLL generates pll_mclk (133MHz) and pll_nclk (266MHz). The clocks ddr_clk and ddr_clk_n go to DDR memory and are delayed by I/O pad delay with respect to pll_mclk. The clocks pll_mclk and pll_nclk are internal to the FPGA. Command and address signals are clocked by a negative edge of pll_mclk. The signal dqs_out acts as a clock for DDR write and is generated by negative edge of pll_nclk. The signal ddr_dq_out is the DDR write data bus and generated by positive edge of pll_nclk. The flops ddr_dq_* latch the read data and are clocked by positive edge of pll_nclk.

Read Operation

Figure 17-2 shows the timing of the DDR read operation. Table 17-1 describes the timing arcs of the read operation.

Figure 17-2. Read Timing Diagram

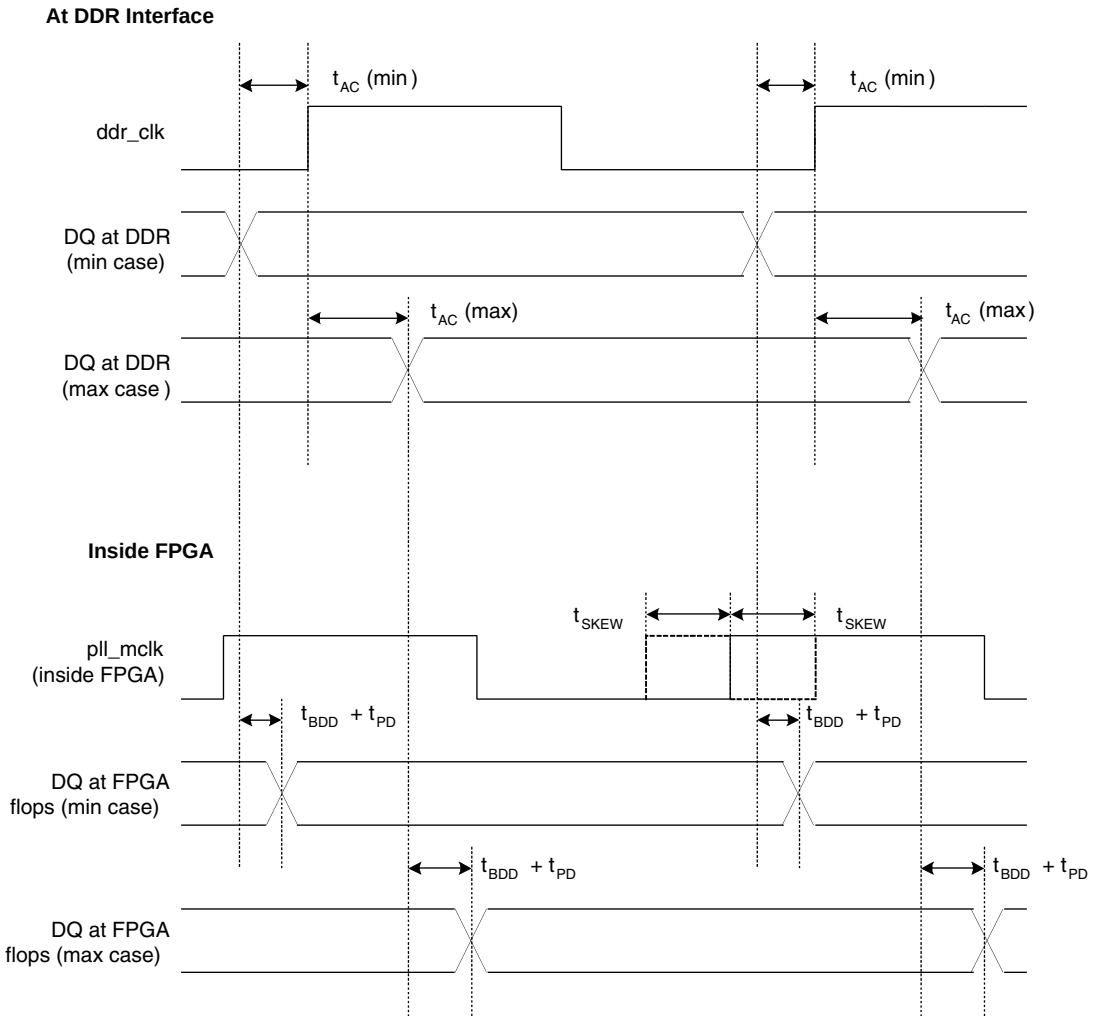


Table 17-1. Read Operation Timing Arcs

Symbol	Description	Example: DDR-NP on ORCA 4
t_{CK}	Clock period of ddr_clk	7.5ns
t_{DDR_CLK} (max)	Delay from the CLK input of the FPGA to the ddr_clk pad including Feedback compensation (Clock Path Delay - Feedback Path).	2.47[1]
t_{DDR_CLK} (min)	Delay from the CLK input of the FPGA to the ddr_clk pad including Feedback compensation (Clock Path Delay - Feedback Path).	1.138[1]
t_{BDC}	Board delay of ddr_clk from FPGA to DDR SDRAM.	—
$t_{AC(MAX)}$	Time from the rising edge of ddr_clk after which the data is available at DDR output pins (max.).	0.75ns
$t_{AC(MIN)}$	Time from the rising edge of ddr_clk after which the data is available at DDR output pins (min.).	-0.75ns
t_{BDD}	Board delay from DDR SDRAM data pad to the FPGA ddr_dq pad.	—
t_{PD}	Propagation delay from FPGA input pad to the ddr_dq_in flip-flop input pin (Data Path Delay).	0.0ns[1]
t_{FDS}	Set-up time required by the ddr_dq_in flip-flop (INREG_SET).	3.195ns[1]
t_{FDH}	Hold time required by the ddr_dq_in flip-flop (INREG_HLD).	-1.609ns[1]
t_{SKEW}	Skew of the PLL.	0.3ns
t_{FPGA_CLK} (max)	Delay from the CLK input of the FPGA to the ddr_dq_in flip-flop clock input including feedback compensation (Clock Out Path Delay - Feedback Path).	2.935ns[1]
t_{FPGA_CLK} (min)	Delay from the CLK input of the FPGA to the ddr_dq_in flip-flop clock input including feedback compensation (Clock Out Path Delay - Feedback Path).	1.239ns[1]

1. t_{FPGA_CLK}, t_{DDR_CLK}, t_{PD} and t_{FDS} can be easily obtained from the PNR time reports.

Set-up Time Calculation for the Data Input (Max. Case)

The DDR Controller IP core uses the positive edge of pll_nclk to latch in the data.

Table 17-1 timing arcs are used to calculate the following:

Max. delay of clock to ddr_dq_in flops = t_{FPGA_CLK} (max) + (t_{CK} * 1/2) - t_{SKEW} - t_{FDS}

Max. delay of DDR read data to ddr_dq_in flops = t_{DDR_CLK} (max) + t_{BDC} + t_{AC} (max) + t_{BDD} + t_{PD}

To meet set-up time at ddr_dq_in flops, Clock Delay - Data Delay > 0

Therefore:

t_{FPGA_CLK} (max) + (t_{CK} * 1/2) - t_{SKEW} - t_{FDS} - t_{DDR_CLK} (max) - t_{BDC} - t_{AC} (max) - t_{BDD} - t_{PD} > 0

Isolating the board delays, we get:

(t_{BDD} + t_{BDC}) < t_{FPGA_CLK} (max) + (t_{CK} * 1/2) - t_{SKEW} - t_{FDS} - t_{DDR_CLK} (max) - t_{AC} (max) - t_{PD}

(t_{BDD} + t_{BDC}) < 3.75 - 0.3 - 3.195 - 2.47 + 2.935 - 0.75 - 0.0

(t_{BDD} + t_{BDC}) < -0.03 ns

Hold Time Calculation for the Data Input (Min. Case)

As shown in Figure 17-2, the min data is available at DDR output pins after t_{AC} (min) time from the rising edge of ddr_clk. Since t_{AC} (min) is generally a negative number, data appears before the rising edge. This data will incur board delay (t_{BDD}) and propagation delay from FPGA input pad to the flip-flop input pin (t_{PD}).

Min. Delay of DDR read Data = t_{DDR_CLK} (min) + t_{BDC} + t_{AC} (min) + t_{BDD} + t_{PD}

Min. Delay of Clock to ddr_dq_in flops = t_{FPGA_CLK} (min) + t_{SKEW} + t_{FDH}

To meet hold time at ddr_dq_in flops, Data Delay - Clock Delay > 0

Therefore:

t_{DDR_CLK} (min) + t_{BDC} + t_{AC} (min) + t_{BDD} + t_{PD} - t_{FPGA_CLK} (min) - t_{SKEW} - t_{FDH} > 0

Isolating the board delays, we get:

(t_{BDD} + t_{BDC}) > t_{FPGA_CLK} (min) + t_{SKEW} + t_{FDH} - t_{DDR_CLK} (min) - t_{AC} (min) - t_{PD}

(t_{BDD} + t_{BDC}) > (1.239) ns + 0.3 + (-1.609ns) - (1.138) - (-0.75) - 0

(t_{BDD} + t_{BDC}) > -0.458 ns

Conclusion: To meet read set-up and hold timing, board delay for ddr_dq, ddr_clk and ddr_clk_n should be:

-0.458ns < (t_{BDD} + t_{BDC}) < -0.03ns

Write Operation

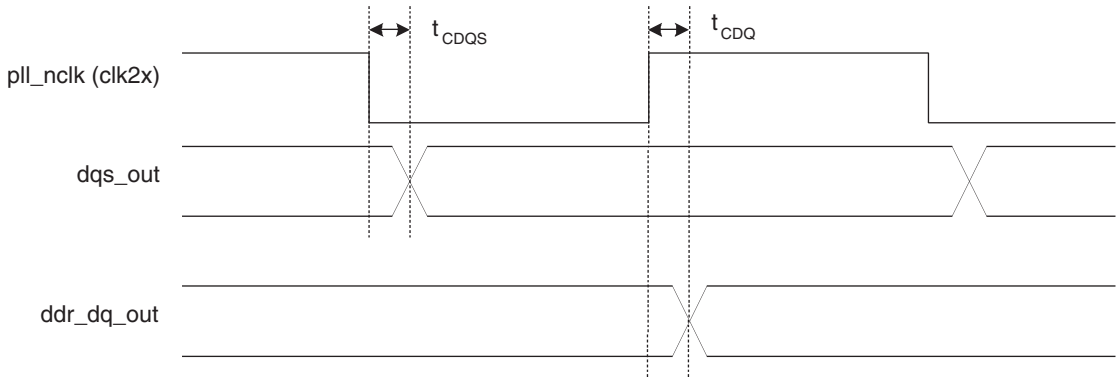
For a proper write operation, data (ddr_dq) should meet set-up (t_{DS}) and hold (t_{DH}) time requirements of DDR SDRAM with respect to ddr_dqs signal. The ddr_dqs signal is generated with respect to negative edge of pll_nclk and data ddr_dq out is generated with respect to positive edge of pll_nclk as shown in Figure 17-3. As a result, 1/2 clk2x (3.75ns/2) is provided as set-up and hold for ddr_dq_out with respect to dqs_out.

For maximum set-up and hold margin, the ddr_dqs and ddr_dq traces on the board should be matched.

Table 17-2. Write Operation Timing Arcs

Symbol	Description	ORCA 4
t_{DS}	Set-up time required by the DQ with respect to DQS for DDR SDRAM.	0.75ns
t_{DH}	Hold time required by the DQ with respect to DQS for DDR SDRAM.	0.75 ns
t_{CDQ}	Clock-to-out timing for ddr_dq with respect to pll_nclk.	—
t_{CDQS}	Clock-to-out timing for ddr_dqs with respect to pll_nclk.	—
t_{BDDS}	Board delay of ddr_dqs from FPGA to DDR SDRAM pins.	—

Figure 17-3. Write Timing Diagram



Write Set-up

Clock Delay = t_{CDQS} + 1/2 clk2x - t_{DS} + t_{BDDS}

Data Delay = t_{CDQ} + t_{BDD}

Clock Delay - Data Delay > 0

Therefore:

t_{CDQS} + 1/2 clk2x - t_{DS} + t_{BDDS} - t_{CDQ} - t_{BDD} > 0

Assumptions for write set-up and hold equations:

1. t_{BDDS} and t_{BDD} are equal (board delays are same both for dqs_out and ddr_dq_out).

2. t_{CDQ} and t_{CDQS} are equal (both are output delays from I/O flop).

Therefore:

1/2 clk2x - t_{DS} > 0

3.75/2 - 0.75 > 0

1.125 > 0

Write Hold

Data Delay = t_{CDQ} + t_{BDD}

Clock Delay = t_{CDQS} + 1/2 clk2x + t_{DH} + t_{BDDS}

Data Delay - Clock Delay > 0

Therefore:

t_{CDQS} + 1/2 clk2x - t_{DH} + t_{BDDS} - t_{CDQ} - t_{BDD} > 0

Assumptions for write set-up and hold equations:

1. t_{BDDS} and t_{BDD} are equal (board delays are same both for dqs_out and ddr_dq_out).

2. t_{CDQ} and t_{CDQS} are equal (both are output delays from I/O flop).

Therefore:

1/2 clk2x - t_{DH} > 0

3.75/2 - 0.75 > 0

1.125 > 0

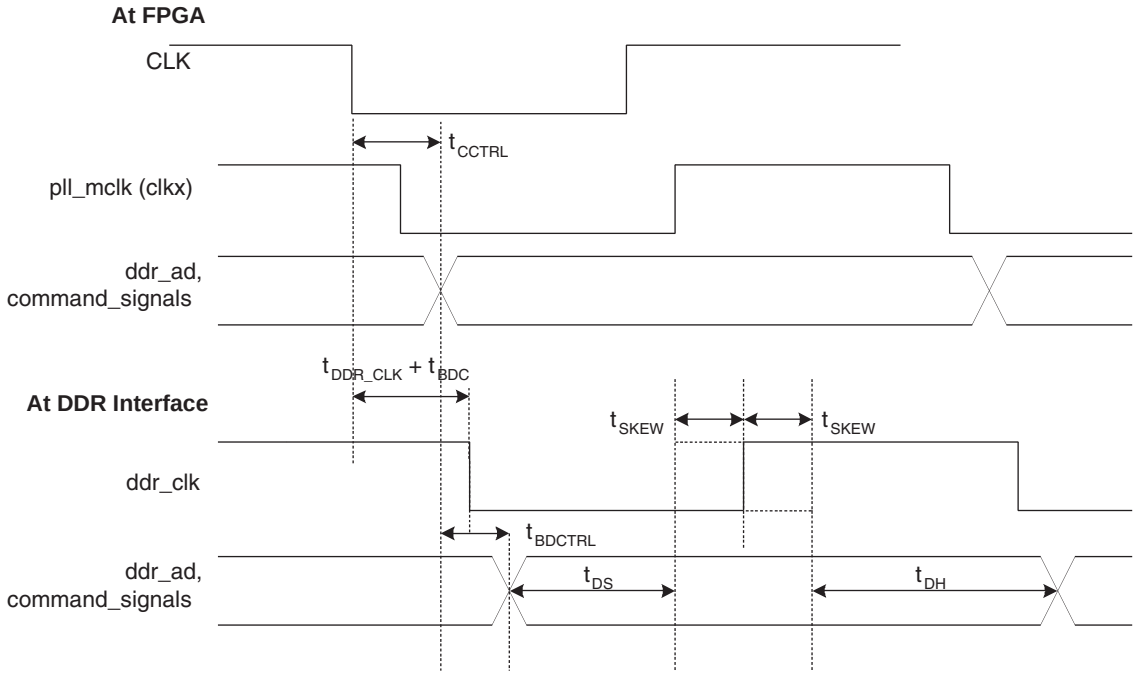
Address and Command Signals

Address (ddr_ad) and command signals (ddr_cas, ddr_ras, ddr_we) should meet set-up (t_{DS}) and hold (t_{DH}) timings at DDR interface with respect to positive edge of ddr_clk. Address and command signals are clocked using negative edge of pll_mclk inside the FPGA as shown below. The ddr_clk signal is a delayed by pad delay and board delay at DDR interface compared to pll_mclk inside the FPGA. As a result, 1/2clkx of set-up and hold is provided by design.

Table 17-3. Timing Arcs for Address and Command Signals

Symbol	Description	ORCA4
t_{CCTRL} (max)	Is the clock-to-out time for `ddr_ad` and command signals. (Clock Path Delay - Feedback Path) + Data Path Delay	4.834 ns
t_{CCTRL} (min)	Is the clock-to-out time for `ddr_ad` and command signals. (Clock Path Delay - Feedback Path) + Data Path Delay	2.147 ns
t_{BDCTRL}	Is the board delay of `ddr_ad` and command signals from FPGA pins to DDR SDRAM pins.	—

Figure 17-4. Timing Diagram for Address and Command Signals



Set-up Calculation

Max Delay of Clock to DDR = t_{DDR_CLK} (max) + t_{BDC} + t_{CK} * 1/2 - t_{SKEW} - t_{DS}

Max Delays of command signals Data to DDR = t_{CCTRL} (max) + t_{BDCTRL}

To meet set up time at DDR memory, Clock Delay - Data Delay > 0

Therefore:

t_{DDR_CLK} (max) + t_{BDC} + t_{CK} * 1/2 - t_{SKEW} - t_{DS} - t_{CCTRL} (max) - t_{BDCTRL} > 0

Isolating the board delays, we get:

t_{BDCTRL} - t_{BDC} < t_{DDR_CLK} (max) + t_{CK} * 1/2 - t_{SKEW} - t_{DS} - t_{CCTRL} (max)

t_{BDCTRL} - t_{BDC} < 2.47 + 3.75 - 0.3 - 0.75 - 4.834

t_{BDCTRL} - t_{BDC} < 0.336 ns

Hold Calculation

Min Delay of command signals Data to DDR = t_{CCTRL} (min) + t_{BDCTRL} + t_{CK} * 1/2

Min Delay of Clock to DDR = t_{DDR_CLK} (min) + t_{BDC} + t_{SKEW} + t_{DH}

To meet hold time at DDR memory, Data Delay - Clock Delay > 0

Therefore:

t_{CCTRL} (min) + t_{BDCTRL} + t_{CK} * 1/2 - t_{DDR_CLK} (min) - t_{BDC} - t_{SKEW} - t_{DH} > 0

Isolating the board delays, we get:

t_{BDCTRL} - t_{BDC} > - t_{CCTRL} (min) - t_{CK} * 1/2 + t_{DDR_CLK} (min) + t_{SKEW} + t_{DH}

t_{BDCTRL} - t_{BDC} > -2.147 - 3.75 + (1.138) + 0.3 + 0.75

t_{BDCTRL} - t_{BDC} > -3.709

t_{BDCTRL} - t_{BDC} > -3.709 ns

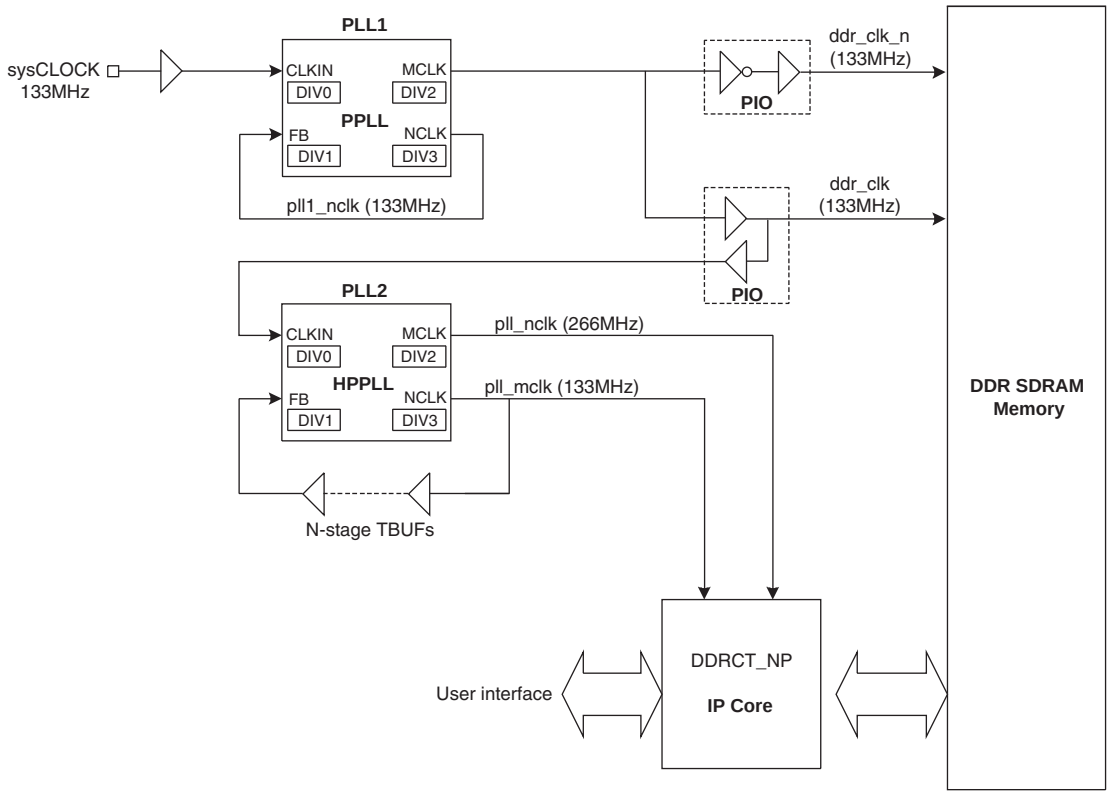
Conclusion: To meet set-up and hold timings of command signals, board delay of command signals `ddr_clk` and `ddr_clk_n` should be:

-3.709 ns < (t_{BDCTRL} - t_{BDC}) < 0.336 ns

Board Design Guidelines

- The `ddr_clk` and `ddr_clk_n` pads should be placed adjacent to each other in the FPGA to get similar internal FPGA delays.
- The `ddr_clk` and `ddr_clk_n` trace delays on the board should be matched.
- The DQ trace delays can be calculated using the following formula, for memory reads:
  t_{SKEW} + t_{FDH} - t_{AC} (min) - t_{PD} - t_{DDR_CLK} + t_{FPGA_CLK} < (t_{BDD} + t_{BDC}) < (t_{CK} * 1/2) - t_{SKEW} - t_{FDS} - t_{AC} (max) - t_{PD} - t_{DDR_CLK} + t_{FPGA_CLK}
- The DQ and DQS trace lengths should be balanced and matching to get maximum set-up/hold time during memory writes.
- The address and control signals for the DDR SDRAM are generated on the negative edge of the FPGA clock. The trace lengths for address and control lines are calculated using following equation:
  -t_{CCTRL} - t_{CK} * 1/2 + t_{DDR_CLK} + t_{SKEW} + t_{DH} < (t_{BDCTRL} - t_{BDC}) < t_{DDR_CLK} + t_{CK} * 1/2 - t_{SKEW} - t_{DS} - t_{CCTRL} + t_{BDC}
- As shown in Figure 17-1, both FPGA internal clock and `ddr_clk` are generated by a single PLL. It may be difficult to meet read data Set-up and hold timing with a single PLL. As shown in Figure 17-5, a two-PLL clocking scheme is proposed to meet read data set-up and hold timing. Adjusting feedback delay of PLL2 can control delay of `pll_mclk`. Increasing delay on `pll_mclk` can increase the read set-up margin but it also decreases the hold margin. To get better timing, skew between `ddr_clk` and `pll_mclk` has to be minimized.

Figure 17-5. Two PLL Clocking Scheme



Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
September 2012	01.1	Updated document with new corporate logo.

Appendix A. Example Extractions of Delays from Timing Reports

From the Set-up Report below, which was run for MAX conditions:

- t_{PD} = 0.0 ns
- t_{FDS} = 3.195 ns
- t_{FPGA_CLK} (max) = 6.206 - 3.271 = 2.935 ns

```
================================================================
Preference: INPUT_SETUP PORT "ddr_dq_*" 2.000000 ns CLKNET "pll_nclk" ;
            32 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------------------------
-----------------------------------
Passed:  The following path meets requirements by 1.740ns

 Logical Details:  Cell type  Pin type       Cell name  (clock net +/-)

   Source:            Port       Pad            ddr_dq_23
   Destination: O-FF In   Data in       U1_ddrct_np_o4_1_008/U3_databusif/ddr_dqoeZ0Z_23  (to
pll_nclk +)

   Data Path Delay:     0.000ns  (0.0% logic, 0.0% route), 0 logic levels.

   Clock Path Delay:    6.206ns  (29.3% logic, 70.7% route), 2 logic levels.

 Constraint Details:

      0.000ns delay ddr_dq_23 to ddr_dq_23 less
      2.000ns offset ddr_dq_23 to clk (totaling -2.000ns) meets
      6.206ns delay clk to ddr_dq_23 less
      3.271ns feedback compensation less
      3.195ns INREG_SET requirement (totaling -0.260ns) by 1.740ns

 Physical Path Details:

      Data path ddr_dq_23 to ddr_dq_23:

   Name     Fanout   Delay (ns)          Site               Resource
                  --------
                    0.000   (0.0% logic, 0.0% route), 0 logic levels.

      Clock path clk to ddr_dq_23:

   Name     Fanout   Delay (ns)          Site               Resource
IN_DEL       ---      1.431        AB4.PAD to       AB4.INCK clk
ROUTE          1      0.816      AB4.INCK to  LLHPPLL.CLKIN clk_c
NCLK_DEL     ---      0.385  LLHPPLL.CLKIN to   LLHPPLL.NCLK U2_ddr_pll_orca/ddr_pll_0_0
ROUTE        136      3.574   LLHPPLL.NCLK to         N24.SC pll_nclk
                  --------
                    6.206   (29.3% logic, 70.7% route), 2 logic levels.
```

```
      Feedback path:

   Name     Fanout    Delay (ns)          Site               Resource
NCLK_DEL     ---      0.385  LLHPPLL.CLKIN to    LLHPPLL.NCLK U2_ddr_pll_orca/ddr_pll_0_0
ROUTE        136      2.886   LLHPPLL.NCLK to     LLHPPLL.FB pll_nclk
                     --------
                       3.271   (11.8% logic, 88.2% route), 1 logic levels.

Report:    0.260ns is the minimum offset for this preference.
```

From the Hold Report below, which was run for MIN conditions:

- t_{PD} = 0.0 ns
- t_{FDH} = -1.609 ns
- t_{FPGA_CLK} (min) = 3.144 - 1.905 = 1.239 ns

```
================================================================
Preference: INPUT_SETUP PORT "ddr_dq_*" 2.000000 ns CLKNET "pll_nclk" ;
            32 items scored, 0 timing errors detected.
--------------------------------------------------------------------------------------------
---------------


Passed:  The following path meets requirements by 0.370ns

 Logical Details:  Cell type  Pin type       Cell name  (clock net +/-)

   Source:         Port       Pad            ddr_dq_31
   Destination:    IO-FF In   Data in        U1_ddrct_np_o4_1_008/U3_databusif/ddr_dqoeZ0Z_31
(to pll_nclk +)

   Data Path Delay:     0.000ns  (0.0% logic, 0.0% route), 0 logic levels.

   Clock Path Delay:    3.144ns  (25.7% logic, 74.3% route), 2 logic levels.

 Constraint Details:

      0.000ns delay ddr_dq_31 to ddr_dq_31 plus
      0.000ns hold offset ddr_dq_31 to clk (totaling 0.000ns) meets
      3.144ns delay clk to ddr_dq_31 plus
      1.905ns feedback compensation less
     -1.609ns INREG_HLD requirement (totaling -0.370ns) by 0.370ns

 Physical Path Details:

      Data path ddr_dq_31 to ddr_dq_31:

   Name     Fanout    Delay (ns)          Site               Resource
                     --------
                       0.000   (0.0% logic, 0.0% route), 0 logic levels.
```

```
      Clock path clk to ddr_dq_31:

   Name     Fanout   Delay (ns)          Site               Resource
IN_DEL       ---     0.576        AB4.PAD to       AB4.INCK clk
ROUTE          1     0.507       AB4.INCK to  LLHPPLL.CLKIN clk_c
NCLK_DEL     ---     0.231  LLHPPLL.CLKIN to   LLHPPLL.NCLK U2_ddr_pll_orca/ddr_pll_0_0
ROUTE        136     1.830   LLHPPLL.NCLK to         C25.SC pll_nclk
                   --------
                     3.144   (25.7% logic, 74.3% route), 2 logic levels.

      Feedback path:

   Name     Fanout   Delay (ns)          Site               Resource
NCLK_DEL     ---     0.231  LLHPPLL.CLKIN to   LLHPPLL.NCLK U2_ddr_pll_orca/ddr_pll_0_0
ROUTE        136     1.674   LLHPPLL.NCLK to     LLHPPLL.FB pll_nclk
                   --------
                     1.905   (12.1% logic, 87.9% route), 1 logic levels.

Report: There is no minimum offset greater than zero for this preference.
```

From the Set-up Report below, which was run for MAX conditions:

- t_{DDR_CLK} (max) = 5.741 - 3.271 = 2.47 ns

```
================================================================================
Preference: CLOCK_TO_OUT PORT "ddr_cas_n" MAX 5.500000 ns CLKPORT "clk" CLKOUT PORT "ddr_clk"
;
            1 item scored, 0 timing errors detected.
--------------------------------------------------------------------------------------------
------------------------------------


Passed:  The following path meets requirements by 3.182ns

 Logical Details:  Cell type  Pin type       Cell name  (clock net +/-)

   Source:         Unknown    Q             U1_ddrct_np_o4_1_008/U1_cmdexe/ddr_cas_nZ0  (from
ddr_clk_c -)
   Destination:    Port       Pad           ddr_cas_n

   Data Path Delay:     1.713ns  (100.0% logic, 0.0% route), 1 logic levels.

   Clock Path Delay:    6.346ns  (28.6% logic, 71.4% route), 2 logic levels.

 Constraint Details:

      6.346ns delay clk to ddr_cas_n less
      3.271ns feedback compensation
      1.713ns delay ddr_cas_n to ddr_cas_n less
      2.470ns delay clk to ddr_clk (totaling 2.318ns) meets
      5.500ns offset clk to ddr_cas_n by 3.182ns

 Physical Path Details:

      Clock path clk to ddr_cas_n:
```

```
   Name     Fanout   Delay (ns)          Site               Resource
IN_DEL       ---     1.431        AB4.PAD to       AB4.INCK clk
ROUTE          1     0.816       AB4.INCK to  LLHPPLL.CLKIN clk_c
MCLK_DEL     ---     0.385  LLHPPLL.CLKIN to   LLHPPLL.MCLK U2_ddr_pll_orca/ddr_pll_0_0
ROUTE        449     3.714   LLHPPLL.MCLK to        AE15.SC ddr_clk_c
                  --------
                    6.346   (28.6% logic, 71.4% route), 2 logic levels.

      Data path ddr_cas_n to ddr_cas_n:

   Name     Fanout   Delay (ns)          Site               Resource
OUTREG_DEL   ---     1.713        AE15.SC to       AE15.PAD ddr_cas_n (from ddr_clk_c)
                  --------
                    1.713   (100.0% logic, 0.0% route), 1 logic levels.

      Clock out path:

   Name     Fanout   Delay (ns)          Site               Resource
IN_DEL       ---     1.431        AB4.PAD to       AB4.INCK clk
ROUTE          1     0.816       AB4.INCK to  LLHPPLL.CLKIN clk_c
MCLK_DEL     ---     0.385  LLHPPLL.CLKIN to   LLHPPLL.MCLK U2_ddr_pll_orca/ddr_pll_0_0
ROUTE        449     1.191   LLHPPLL.MCLK to      AF3.OUTDD ddr_clk_c
OUTDD_DEL    ---     1.918      AF3.OUTDD to        AF3.PAD ddr_clk
                  --------
                    5.741   (65.0% logic, 35.0% route), 3 logic levels.

      Feedback path:

   Name     Fanout   Delay (ns)          Site               Resource
NCLK_DEL     ---     0.385  LLHPPLL.CLKIN to   LLHPPLL.NCLK U2_ddr_pll_orca/ddr_pll_0_0
ROUTE        136     2.886   LLHPPLL.NCLK to     LLHPPLL.FB pll_nclk
                  --------
                    3.271   (11.8% logic, 88.2% route), 1 logic levels.

Report:    2.318ns is the minimum offset for this preference.
```

From the Hold Report below, which was run for MIN conditions:

- t_{DDR_CLK} (min) = 3.043 - 1.905 = 1.138 ns

```
================================================================================
Preference: CLOCK_TO_OUT PORT "ddr_cas_n" MAX 5.500000 ns CLKPORT "clk" CLKOUT PORT "ddr_clk"
;
            1 item scored, 0 timing errors detected.
--------------------------------------------------------------------------------------------------
-----------------------------------


Passed:  The following path meets requirements by 1.056ns

 Logical Details:  Cell type  Pin type       Cell name  (clock net +/-)

   Source:         Unknown    Q             U1_ddrct_np_o4_1_008/U1_cmdexe/ddr_cas_nZ0  (from
ddr_clk_c -)
   Destination:    Port       Pad           ddr_cas_n
```

```
   Data Path Delay:     0.928ns  (100.0% logic, 0.0% route), 1 logic levels.

   Clock Path Delay:    3.171ns  (25.4% logic, 74.6% route), 2 logic levels.

 Constraint Details:

      3.171ns delay clk to ddr_cas_n less
      1.905ns feedback compensation
      0.928ns delay ddr_cas_n to ddr_cas_n less
      1.138ns delay clk to ddr_clk (totaling 1.056ns) meets
      0.000ns hold offset clk to ddr_cas_n by 1.056ns

 Physical Path Details:

      Clock path clk to ddr_cas_n:

   Name    Fanout   Delay (ns)          Site               Resource
IN_DEL      ---     0.576        AB4.PAD to       AB4.INCK clk
ROUTE         1     0.507       AB4.INCK to  LLHPPLL.CLKIN clk_c
MCLK_DEL    ---     0.231  LLHPPLL.CLKIN to   LLHPPLL.MCLK U2_ddr_pll_orca/ddr_pll_0_0
ROUTE       449     1.857   LLHPPLL.MCLK to        AE15.SC ddr_clk_c
                  --------
                    3.171   (25.4% logic, 74.6% route), 2 logic levels.

      Data path ddr_cas_n to ddr_cas_n:

   Name    Fanout   Delay (ns)          Site               Resource
OUTREG_DEL  ---     0.928        AE15.SC to       AE15.PAD ddr_cas_n (from ddr_clk_c)
                  --------
                    0.928   (100.0% logic, 0.0% route), 1 logic levels.

      Clock out path:

   Name    Fanout   Delay (ns)          Site               Resource
IN_DEL      ---     0.576        AB4.PAD to       AB4.INCK clk
ROUTE         1     0.507       AB4.INCK to  LLHPPLL.CLKIN clk_c
MCLK_DEL    ---     0.231  LLHPPLL.CLKIN to   LLHPPLL.MCLK U2_ddr_pll_orca/ddr_pll_0_0
ROUTE       449     0.778   LLHPPLL.MCLK to      AF3.OUTDD ddr_clk_c
OUTDD_DEL   ---     0.951      AF3.OUTDD to        AF3.PAD ddr_clk
                  --------
                    3.043   (57.8% logic, 42.2% route), 3 logic levels.

      Feedback path:

   Name    Fanout   Delay (ns)          Site               Resource
NCLK_DEL    ---     0.231  LLHPPLL.CLKIN to   LLHPPLL.NCLK U2_ddr_pll_orca/ddr_pll_0_0
ROUTE       136     1.674   LLHPPLL.NCLK to     LLHPPLL.FB pll_nclk
                  --------
                    1.905   (12.1% logic, 87.9% route), 1 logic levels.

Report:    1.056ns is the maximum offset for this preference.
================================================================================
```

From the Set-up Report below, which was run for MAX conditions. The report shown here is for ddr_ad.

- t_{CCTRL} (max) = (6.392-3.271) + 1.713 = 4.834 ns

Find delays similarly for ddr_ras_n, ddr_cas_n, ddr_we_n, ddr_ba, ddr_cs_n and ddr_cke signals. Then take the max of those delays as t_{CCTRL} (max).

```
================================================================================
Preference: CLOCK_TO_OUT PORT "ddr_ad_*" 5.500000 ns CLKNET "ddr_clk_c" ;
            12 items scored, 0 timing errors detected.

Passed:  The following path meets requirements by 0.666ns

 Logical Details:  Cell type  Pin type       Cell name  (clock net +/-)

   Source:         Unknown    Q             U1_ddrct_np_o4_1_008/U1_cmdexe/ddr_adZ0Z_6  (from
ddr_clk_c -)
   Destination:    Port       Pad           ddr_ad_6

   Data Path Delay:     1.713ns  (100.0% logic, 0.0% route), 1 logic levels.

   Clock Path Delay:    6.392ns  (28.4% logic, 71.6% route), 2 logic levels.

 Constraint Details:

      6.392ns delay clk to ddr_ad_6 less
      3.271ns feedback compensation
      1.713ns delay ddr_ad_6 to ddr_ad_6 (totaling 4.834ns) meets
      5.500ns offset clk to ddr_ad_6 by 0.666ns

 Physical Path Details:

      Clock path clk to ddr_ad_6:

   Name    Fanout   Delay (ns)          Site               Resource
IN_DEL      ---     1.431        AB4.PAD to       AB4.INCK clk
ROUTE         1     0.816       AB4.INCK to  LLHPPLL.CLKIN clk_c
MCLK_DEL    ---     0.385  LLHPPLL.CLKIN to   LLHPPLL.MCLK U2_ddr_pll_orca/ddr_pll_0_0
ROUTE       449     3.760   LLHPPLL.MCLK to        AE14.SC ddr_clk_c
                 --------
                   6.392   (28.4% logic, 71.6% route), 2 logic levels.

      Data path ddr_ad_6 to ddr_ad_6:

   Name    Fanout   Delay (ns)          Site               Resource
OUTREG_DEL  ---     1.713        AE14.SC to       AE14.PAD ddr_ad_6 (from ddr_clk_c)
                 --------
                   1.713   (100.0% logic, 0.0% route), 1 logic levels.

      Feedback path:

   Name    Fanout   Delay (ns)          Site               Resource
NCLK_DEL    ---     0.385  LLHPPLL.CLKIN to   LLHPPLL.NCLK U2_ddr_pll_orca/ddr_pll_0_0
ROUTE       136     2.886   LLHPPLL.NCLK to     LLHPPLL.FB pll_nclk
                 --------
                   3.271   (11.8% logic, 88.2% route), 1 logic levels.

Report:    4.834ns is the minimum offset for this preference.
```

From the Hold Report below, which was run for MIN conditions. The report shown here is for ddr_ad* only.

- t_{CCTRL} (min) = (3.124-1.905) + 0.928 = 2.147 ns

Find delays similarly for ddr_ras_n, ddr_cas_n, ddr_we_n, ddr_ba, ddr_cs_n and ddr_cke signals. Then take the min of those delays as t_{CCTRL} (min).

```
================================================================================
Preference: CLOCK_TO_OUT PORT "ddr_ad_*" 5.500000 ns CLKNET "ddr_clk_c" ;
            12 items scored, 0 timing errors detected.

Passed:  The following path meets requirements by 2.147ns

 Logical Details:  Cell type  Pin type       Cell name  (clock net +/-)

   Source:         Unknown    Q             U1_ddrct_np_o4_1_008/U1_cmdexe/ddr_adZ0Z_4  (from
ddr_clk_c -)
   Destination:    Port       Pad           ddr_ad_4

   Data Path Delay:     0.928ns  (100.0% logic, 0.0% route), 1 logic levels.

   Clock Path Delay:    3.124ns  (25.8% logic, 74.2% route), 2 logic levels.

 Constraint Details:

      3.124ns delay clk to ddr_ad_4 less
      1.905ns feedback compensation
      0.928ns delay ddr_ad_4 to ddr_ad_4 (totaling 2.147ns) meets
      0.000ns hold offset clk to ddr_ad_4 by 2.147ns

 Physical Path Details:

      Clock path clk to ddr_ad_4:

   Name    Fanout   Delay (ns)          Site               Resource
IN_DEL      ---     0.576        AB4.PAD to       AB4.INCK clk
ROUTE         1     0.507       AB4.INCK to  LLHPPLL.CLKIN clk_c
MCLK_DEL    ---     0.231  LLHPPLL.CLKIN to   LLHPPLL.MCLK U2_ddr_pll_orca/ddr_pll_0_0
ROUTE       449     1.810   LLHPPLL.MCLK to         T26.SC ddr_clk_c
                  --------
                    3.124   (25.8% logic, 74.2% route), 2 logic levels.

      Data path ddr_ad_4 to ddr_ad_4:

   Name    Fanout   Delay (ns)          Site               Resource
OUTREG_DEL  ---     0.928         T26.SC to        T26.PAD ddr_ad_4 (from ddr_clk_c)
                  --------
                    0.928   (100.0% logic, 0.0% route), 1 logic levels.

      Feedback path:

   Name    Fanout   Delay (ns)          Site               Resource
NCLK_DEL    ---     0.231  LLHPPLL.CLKIN to   LLHPPLL.NCLK U2_ddr_pll_orca/ddr_pll_0_0
ROUTE       136     1.674   LLHPPLL.NCLK to      LLHPPLL.FB pll_nclk
                  --------
                    1.905   (12.1% logic, 87.9% route), 1 logic levels.

Report:    2.220ns is the maximum offset for this preference.
```