

Lattice Radiant Software 1.1 Release Notes

Welcome to Lattice Radiant™ software, the complete design environment for Lattice Semiconductor Field Programmable Gate Arrays (FPGAs). Radiant software offers leading-edge design and implementation tools optimized for cost-sensitive and low-power Lattice FPGA architectures.

Radiant software is available for both the Windows and Linux operating systems, and provides key features to make designing for Lattice Semiconductor programmable devices easier than ever, and improves your time to market. Some of the key benefits include:

- **Design Exploration:** Explores design alternatives with Implementations and Strategies.
- **Ease-of-Use Features:** Introduces next generation and simple user interface, with intuitive message filtering, and cross-probing for effective debugging.
- **Improved Design Flow:** Utilizes standard Synopsys Design Constraints SDC format for constraint flow, integrates Timing Analysis for rapid timing closure, and provides Tcl scripting support for automation.

Lattice Semiconductor offers a rich variety of information sources, including a Help system, PDF user manuals, tutorials, and online discussions. The easiest way to access any of them is through Radiant software online Help.

You can also find extensive information about Radiant software and its capabilities, tools, and workflow on the Lattice Semiconductor website at: www.latticesemi.com.

Key Features in Radiant Software

- ▶ **Standardized Timing and Physical Constraints** utilizing the popular SDC format to help you easily apply constraints to your designs.
- ▶ **Unified Static Timing Analysis from Synthesis to Place & Route** to accelerate design timing closure.
- ▶ **Enhanced IP Security Flow and Ecosystem** to allow efficient distribution of Soft IP's and to improve 3rd Party Soft IP security.
- ▶ **New and Simplified GUI design** with option of light or dark color theme.
- ▶ **Simplified and Efficient Design Flows and Tools** to improve Ease-of-Use.

What's New in Radiant Software 1.1

▶ iCE40 UltraPlus device enhancements and bug fixes

- New HDL attribute RGB_TO_GPIO.
- Four new iCE40 UltraPlus bitstream strategy options have been added:
 - Enable Warm Boot
 - Set All Unused IO No Pullup
 - Set NVCM Security
 - SPI Flash Low Power Mode

▶ Enhanced Intellectual Property (IP) tools and flow

- **Added IP on Server capability.** Allows users to download and install the latest System IP available from Lattice Semiconductor.
- **IP Packager tool.** This new tool allows IP developers, including third party IP providers and customers, to prepare and package IP in the Radiant Software IP format.
- **IP Catalog Added Modules and Parameterized Module Instantiation (PMI).** The number of modules and PMI have increased substantially. The following table lists iCE40 UltraPlus modules and PMI that have been added in Radiant Software 1.1.

Module Name	PMI	User Guide
Adder_Subtractor	pmi_addsub	Arithmetic Modules User Guide
Comparator	N/A	Arithmetic Modules User Guide
Counter	pmi_counter	Arithmetic Modules User Guide
FIFO	pmi_fifo	Memory Modules User Guide
FIFO DC	pmi_fifo_dc	Memory Modules User Guide
LFSR	N/A	Arithmetic Modules User Guide
Mult_Add_Sub_Sum	pmi_multaddsubsum	Arithmetic Modules User Guide
ROM	pmi_rom	Memory Modules User Guide
Shift Register	N/A	Memory Modules User Guide

- Support for test bench generation.

▶ **Constraints Syntax and Flow updates**

- **Timing Constraints:** Added Object Access Command (-of_objects) support which allows flexible and efficient object accesses. Note that this option is supported in constraint files only in Radiant software 1.1. Graphical User Interface support for this option is expected in Radiant 1.2.
- **Physical Constraints:** Added -region option support in ldc_prohibit constraint. This option is also supported in ldc_set_location.
- **Timing Constraint Editor:**
 - Added set_load constraint
 - Added Disable/Enable checkbox that allows you to easily disable or enable constraints.

▶ **Tool and Other Enhancements**

- **Cross-probe timing path from timing reports.** Map and PAR timing reports now have hyperlinks that allow users to view timing paths in Netlist Analyzer, Physical View, and Floorplan View.
- **Detachable Tool Windows.** Detach and attach functionality has been added for all tools and views, allowing user to work on a tool outside of the Radiant software environment.
- **Lattice Synthesis Engine (LSE).** LSE has significant performance improvements from Radiant software 1.0 including:
 - Improvements in embedded block RAM (EBR), finite state machine (FSM), and digital signal processor (DSP) extraction.
 - Improvements in Area implementation and run time.
- **Power Estimator.** A new stand-alone Power Estimator has been added.
- **Simulation Wizard.** The Simulation Wizard has been updated to support post-synthesis simulation.
- **Source Template.** A new Source Template tab has been added to make it easier to access various templates without the need to have the Source Editor running. The selection of templates has been enhanced. Available templates, in both VHDL and Verilog, include:
 - Common Templates
 - PMI Templates
 - Primitive Templates

- Attribute Templates
 - Encryption Templates
 - Timing Constraints
 - Physical Constraints
- **Ubuntu operating system.** Support for Ubuntu operating system LTS 16.4 has been added.

Device Support

The following device family is supported in Radiant software.

Device Family	Free License
iCE40 UltraPlus	Yes

Help Resources

Available information resources for the Radiant software include the following:

▶ User Guides

▶ [Lattice Radiant Software User Guide](#)

This document provides an overview of the Radiant software features.

▶ [Lattice Radiant Software Guide for Lattice Diamond Users](#)

This document provides guidelines for Lattice Diamond users so that they can quickly grasp the concepts of the new features in the Radiant software.

▶ [Migrating iCEcube2 iCE40 UltraPlus Designs to Lattice Radiant Software](#)

This document provides guidance for iCEcube2 users to accelerate learning of the Lattice Radiant software.

▶ [Reveal Troubleshooting Guide for Lattice Radiant Software](#)

This document provides Reveal restrictions on Radiant software.

▶ Online Help

▶ [Lattice Radiant Software Online Help: Start Lattice Radiant software and select “Getting Started” icon under Information Center.](#)



▶ [Lattice Radiant Software 1.1 Help \(PDF version\)](#)

This is a PDF version for the Radiant software Online Help.

▶ Tutorial

▶ [Lattice Radiant Software Tutorial](#)

This document provides a tutorial for Radiant software.

▶ Installation

▶ [Lattice Radiant Software 1.1 Installation Guide for Windows](#)

This document provides installation instructions for Windows OS.

▶ [Lattice Radiant Software 1.1 Installation Guide for Linux/Ubuntu](#)

This document provides installation instructions for Linux OS.

▶ Lattice website

▶ General Information: General information on Radiant software can be found on the Lattice Web site:

<http://www.latticesemi.com/latticeradiant>

Help for Migrating Radiant Software 1.0 Designs to Radiant Software 1.1

If you are migrating a design from Radiant software 1.0 to Radiant software 1.1, consider the following:

1. When loading Radiant software 1.0 iCE40 UltraPlus RDF project files, Radiant software 1.1 will provide a Warning dialog to reset the project process due to Radiant software 1.1 database update.
2. If you have Radiant 1.0 designs that used Radiant 1.0 Modules/IPs, they will need to be regenerated in Radiant 1.1.
3. An incorrect fmax calculation issue in Radiant software 1.0 timing report under some specific clock conditions has been fixed in Radiant software 1.1.

In Radiant software 1.0, the summary table clock frequency could be incorrect under the following conditions:

- When the path is constrained to check both positive and negative edges of clock by using both a half cycle and a full cycle constraints.
- When there are multiple clocks in the design and inter-clock path slacks end up masking single clock path slacks.

In Radiant 1.1 software, users are recommended to use slack numbers instead of fmax because slacks are a more accurate representation of the tool performance.

Help for Lattice Diamond Users

If you are a current Lattice Diamond software user, a tool and documentation exist that will help you quickly understand Radiant software features and concepts.

- Import Diamond project – This tool allows you to quickly and easily import your Diamond software project into Radiant software. For more information, refer to Radiant software online Help **User Guides > Managing Projects > Importing Lattice Diamond Projects**.
- [Lattice Radiant Software Guide for Lattice Diamond Users](#)
This document provides information to help Lattice Diamond users quickly grasp the features and concepts of Radiant software, as well as understand the differences between Radiant and Diamond software.

Help for Migrating iCEcube2 Designs to Radiant Software

The following reference documents will help you migrate your iCEcube2 designs to Radiant software.

- [Migrating iCEcube2 ICE40 UltraPlus Designs to Lattice Radiant Software](#)
This document provides information to help iCEcube2 users migrate ICE40 UltraPlus designs into Radiant software.

System Requirements

The following shows the basic system requirements for Radiant software:

- ▶ Intel Pentium or Pentium-compatible PC
- ▶ 64-bit OS:
 - ▶ Windows 7, Windows 8 and 8.1, or Windows 10
 - ▶ Red Hat Enterprise Linux 6.6 or 7
 - ▶ Ubuntu version 16.04 LTS
- ▶ Approximately 2 GB free disk space
- ▶ Computer Memory Requirement: 2 GB Minimum, 3GB Recommended
- ▶ 1024 X 768 graphics display
- ▶ Network adapter for license and network connectivity
- ▶ A Web browser with JavaScript capability
- ▶ Microsoft Internet Explorer 8 or higher (required for Aldec Active-HDL Lattice Edition simulator)
- ▶ Acrobat Reader 5.0 or later

Support for Third-Party Synthesis and Simulator Tools

In addition to the Synopsys Synplify Pro® for Lattice and Aldec Active-HDL™ Lattice Edition tools included with Radiant software suite, the following 3rd-Party Synthesis and Simulator tools are supported by Radiant software:

▶ Synthesis Tools

- ▶ Synopsys Synplify Pro FPGA synthesis software version O-2018.09-SP1 or later

▶ Simulator Tools

- ▶ Aldec Active-HDL v10.4 or later
- ▶ Aldec Riviera-PRO™ v2016.02 or later
- ▶ Mentor Questa® Sim v10.4g or later
v10.6b or later

Known Issues for Radiant Software 1.1

The following are known Issues for the Radiant software 1.1.

Lattice Synthesis Engine (LSE) does not implement async mult

LSE does not implement async mult. LSE always uses MAC16.

Versions affected: 1.1

Devices affected: All

Bug number: DNG-3144

The *syn_useioff* attribute does not work for LSE.

This attribute controls selective register to be pack into I/O pad cell based on timing requirements. LSE "Use IO Registers" Strategy option is set to Auto to use IO registers whenever applicable. Those IO register inferences cannot be individually prevented by the user HDL attribute "syn_useioff = 0".

Versions affected: 1.0, 1.1

Devices affected: All

Bug number: DNG-3382

Workarounds (2 options):

1. Use the global option "Use IO Registers = False" in Strategy Manager if the design permits, in which LSE will not pack any register into I/O pad cell unless instantiated.
2. Use Synplify Pro for Lattice synthesis tool

No warning message issued by Synplify Pro when Synplify encryption key is missing

When the encrypted design without a valid key is not be synthesized by Synplify Pro, it should provide a warning message. Note that the encrypted design will still be protected.

Versions affected: 1.1

Devices affected: All

Bug number: DNG-5300

Hold Time calculation shows user speed grade for setup and hold calculation.

The timing engine uses the user speed grade for both setup and hold calculation. This is not the behavior users of Diamond software are expecting. Future versions of Radiant software will change this behavior to do setup calculation at the user speed grade and hold calculation at the M speed grade.

Versions affected: 1.1

Devices affected: All

Bug number: DNG-5651

If design has an error during I/O Timing Analysis, the process flow may continue as if there is no error.

An error during the I/O Timing Analysis process should cause the process flow to stop with the Process Toolbar icon appearing as a red box with an "X". But, in some cases, if there is an error during the I/O Timing Analysis process, the process flow may continue as if there is no error, and the Process Toolbar icon will appear as a green box with a checkmark.

Versions affected: 1.1

Devices affected: All

Bug number: DNG-6160

Contacting Technical Support

FAQs

The first place to look. The [Answer Database](#) on the Lattice Semiconductor Web site provides solutions to questions that many of our customers have already asked. Lattice Applications Engineers are continuously adding to the Database.

Technical Support Assistance

Submit a technical support case via www.latticesemi.com/techsupport.

For Local Support

Contact your nearest [Lattice Sales Office](#).