Designing a High Performance SDRAM Controller Using ispMACH Devices

February 2002 Reference Design RD1007

Introduction

Synchronous DRAMs have become the memory standard in many designs. They provide substantial advances in DRAM performance. They synchronously burst data at clock speeds presently up to 143MHz. They also provide hidden precharge time and the ability to randomly change column addresses on each clock cycle during a burst cycle.

This reference design provides the user with a baseline SDRAM Controller design. The user may modify the design to meet specific design requirements. This document provides information on how this design operates and shows the user where changes can be made to support other functionality.

The design was implemented in Verilog, synthesized and fitted using Lattice's ispLEVER™ Development System into an ispMACH™ 4A device. The design requires 57 macrocells and 59 I/O pins. Using an M4A-128/64-7 yields a maximum operating frequency of 111MHz. Using an M4A-128/64-55 yields a maximum operating frequency of 153MHz. Results may vary according to the synthesis tool.

This design assumes the reader has experience implementing page mode DRAM systems. Information available in documents listed in the Applicable Documents section is not repeated in this document.

Applicable Documents

- Micron Synchronous DRAM Data Sheet: MT48LC16M4A2/8M8A2/4M16A2

Theory of Operation

Overview

This SDRAM Controller is designed to interface to standard microprocessors. The controller is independent of processor type. This design, as implemented, supports two 16MB memory regions configured as 4 M x 32 bits. Each region consists of two Micron MT48LC4M16A2 devices. Changing byte enable inputs and address inputs will change the width and size of this design. For example, if a 64-bit wide data bus is desired, increase the byte enable signals from 4 to 8. If a larger memory space is required, add address inputs and reconfigure the row and column address appropriately or add more chip selects.

Before SDRAM read and write cycles can be performed, the SDRAM sub-system must be initialized. This entails performing a precharge cycle, two auto refresh cycles followed by a load mode register cycle. Commands are encoded in the SDRAM signals. Table 1 lists all SDRAM commands.

Top Level Signal Description

Table 2 provides the input/output signals of the SDRAM Controller. Signals ending with "_L" indicate an active low signal. This convention is used throughout the design. All input signals except SDRAM_EN must be synchronous to the clock. SDRAM_EN is synchronized internally.

Table 1. SDRAM Commands

Command	cs_	ras_	cas_	we_	Dqm	Add
Command Inhibit	H	X	X	X	X	X
No Operation	L	H	H	H	X	X
Activate	L	L	H	H	X	Bank/Row
Read	L	H	L	H	X	Bank_Col
Write	L	H	L	L	X	Bank/Col
Burst Terminate	L	H	H	L	X	X
Precharge	L	L	H	L	X	Code
Refresh	L	L	L	H	X	X
Load Mode Register	L	L	L	L	X	Op Code
Write Enable/Output Enable	—	—	—	—	**L**	—
Write Inhibit/Output High-Z	—	—	—	—	H	—

Table 2. SDRAM Signals

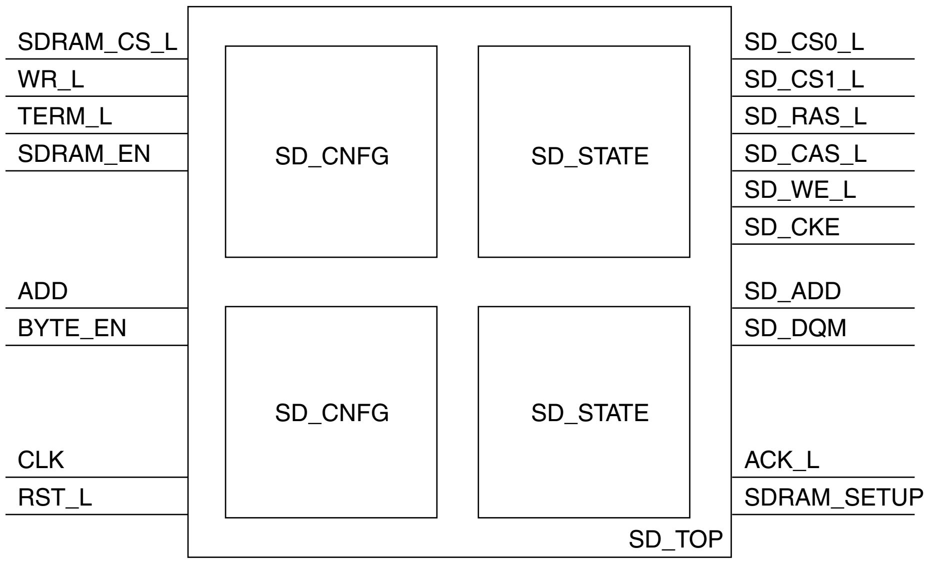
Signal	Type	Description
SDRAM_CS_L	Input	SDRAM Chip Select from processor.
WR_L	Input	Write pulse from processor
SDRAM_EN	Input	SDRAM Enable signal – may be tied high.
TERM_L	Input	Terminates burst cycles.
CLK	Input	Input clock – The SDRAM output signals will be synchronous to this clock.
RST_L	Input	Reset – Resets all signals in the controller.
BYTE_EN[3:0]	Input	Byte enable signals. These signals are directly related to sd_dqm[3:0] signals. High indicates active byte lane.
ADD[24:0]	Input	Processor Address bus. Used to address SDRAM.
SD_CKE	Output	SDRAM Clock Enable – enables all SDRAM cycles.
SD_BA[1:0]	Output	SDRAM Bank Address – selects the proper SDRAM bank.
SD_CS0_L	Output	SDRAM Chip select signal for lower 16 MB region.
SD_CS1_L	Output	SDRAM Chip Select signal for upper 16 MB region.
SD_RAS_L	Output	SDRAM Row Address Strobe.
SD_CAS_L	Output	SDRAM Column Address Strobe.
SD_WE_L	Output	SDRAM Write Enable Strobe.
SD_ADD[11:0]	Output	SDRAM Address Signals
SD_DQM[3:0]	Output	SDRAM Data Qualifier Mask. If high; on writes data is masked, on reads buffer is tristated.
ACK_L	Output	Acknowledge – Indicates when data cycles are active.
SDRAM_SETUP	Output	SDRAM Setup indicates that the SDRAM has been initialized.

Design Modules

The SDRAM Controller is comprised of a top-level module called SD_TOP as shown in Figure 1. This top-level module instantiates the following modules:

- SD_CNFG
- SD_RFRSH
- SD_STATE
- SD_SIG

Figure 1. Block Diagram



Each module is discussed below.

SD_CNFG Module

The SD_CNFG module performs the configuration and initialization of the SDRAMs. When the reset signal becomes inactive, and if the SDRAM_EN signal is active, this module sends requests to the state machine module to initialize the SDRAM. The SDRAM_EN signal could be removed from the design or can be tied high if this feature is not needed. If tied high, the controller will initialize the SDRAM sub-system when the reset signal becomes false.

The parameters for the mode register are stored in this module. These can be modified to suit the user's specific needs. Some of the bits are reserved and must be kept as '0'. The parameters CAS LATENCY, BURST MODE, BURST LENGTH and BURST TYPE can be changed in this module.

Table 3 describes the input and output signals of this module.

Table 3. SD_CNFG Signals

Signal	Type	Description
SDRAM_EN	Input	SDRAM Enable signal – allows SDRAM initialization.
CLK	Input	Clock signal – runs all synchronous logic
RST_L	Input	Reset signal – resets all synchronous logic.
SDRAM_CYCLE[3:0]	Input	State machine bits – indicates the type of cycle: 00 = idle, 01 = command, 10 = data, 11 = refresh
STATE_CNTR[3:0]	Input	State machine bits – indicates state of cycle.
SDRAM_MODE_REG[11:0]	Output	Mode Register Value.
SDRAM_CMND[1:0]	Output	SDRAM command desired : 00 = nop, 01 = precharge, 10 = autorefresh, 11 = load mode register
CMND_CYCLE_REQ	Output	Command Cycle Request to state machine
SDRAM_SETUP	Output	Indicates SDRAM setup is complete

SD_RFRSH Module

The SD_RFRSH module provides a refresh request signal to the state machine module. The refresh module has a 12 bit counter that is clocked by the system clock. The output of the counter is set so that a request occurs every 15.6µsec. The parameter value “count” can be changed depending on the clock frequency. The counter doesn't start counting until after the SDRAM has been initialized. Table 4 describes the input and output signals of this module.

Table 4. SD_RFRSH Signals

Signal	Type	Description
CLK	Input	Clock signal – runs all synchronous logic
RST_L	Input	Reset signal – resets all synchronous logic.
SDRAM_SETUP	Input	Indicates SDRAM setup is complete
SDRAM_CYCLE[3:0]	Input	State machine bits – indicates the type of cycle: 00 = idle, 01 = command, 10 = data, 11 = refresh
RFRSH_REQ	Output	Refresh cycle request to state machine.

SD_STATE Module

The SD_STATE module takes requests from:

- the processor to perform data cycles
- the SD_CNFG module to perform command cycles
- the SD_RFRSH module to perform refresh cycles

It outputs a state type vector as well as a state bit vector. The type vector indicates what type of cycle is being performed. The bit vector indicates the state cycle. Table 5 describes the input/output signals for this module.

Table 5. SD_STATE Signals

Signal	Type	Description
SDRAM_CS_L	Input	Chip select signal from processor. This signal must be synchronous to the clock.
CMND_CYCL_REQ	Input	Command cycle request from SD_CNFG module.
RFRSH_REQ	Input	Refresh request from SD_RFRSH module.
CLK	Input	Clock signal – runs all synchronous logic
RST_L	Input	Reset signal – resets all synchronous logic.
SDRAM_CYCLE[3:0]	Output	State machine bits – indicates the type of cycle: 00 = idle, 01 = command, 10 = data, 11 = refresh
STATE_CNTR[3:0]	Output	State machine bits – indicates state of cycle.

SD_SIG Module

The SD_SIG module outputs the appropriate SDRAM signals depending on what type of cycle is occurring and where the state machine is at in the cycle. Table 6 describes the input and output signals for this module.

Table 6. SD_SIG Signals

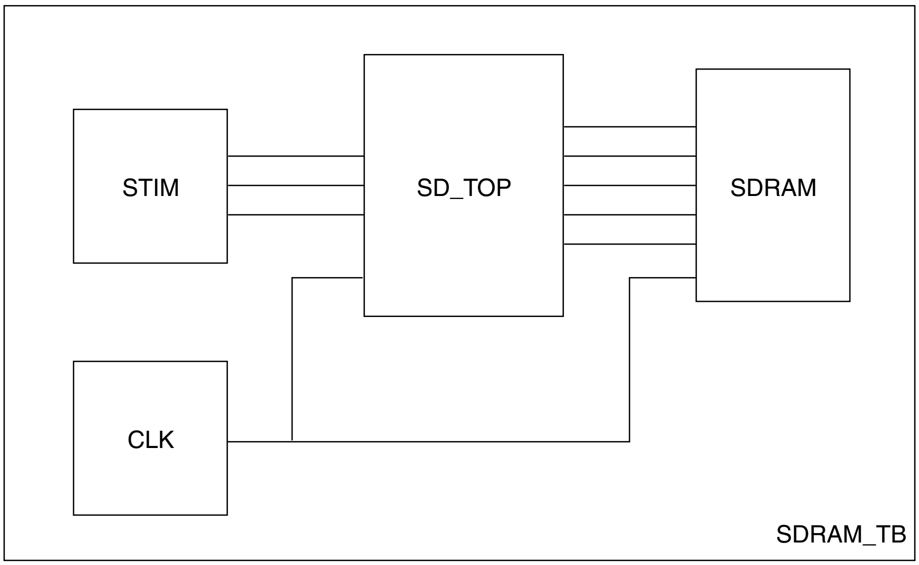
Signal	Type	Description
ADD[24:0]	Input	Address bus from processor.
WR_L	Input	Write strobe from processor.
BYTE_EN[3:0]	Input	Byte enable signals from processor.
TERM_L	Input	Terminate signal from processor.
SDRAM_CYCLE[3:0]	Input	State machine bits – indicates the type of cycle: 00 = idle, 01 = command, 10 = data, 11 = refresh
STATE_CNTR[3:0]	Input	State machine bits - indicates state of cycle.
SDRAM_MODE_REG[11:0]	Input	Mode Register Value.
SDRAM_CMND[1:0]	Input	SDRAM command desired: 00 = nop, 01 = precharge, 10 = autorefresh, 11 = load mode register
CLK	Input	Clock signal – runs all synchronous logic
RST_L	Input	Reset signal – resets all synchronous logic.
SD_CKE	Output	SDRAM Clock Enable – enables all SDRAM cycles.
SD_BA[1:0]	Output	SDRAM Bank Address – selects the proper SDRAM bank.
SD_CS0_L	Output	SDRAM Chip Select signal for lower 16 MB region.
SD_CS1_L	Output	SDRAM Chip Select signal for upper 16 MB region.
SD_RAS_L	Output	SDRAM Row Address Strobe.
SD_CAS_L	Output	SDRAM Column Address Strobe.
SD_WE_L	Output	SDRAM Write Enable Strobe.
SD_ADD[11:0]	Output	SDRAM Address Signals
SD_DQM[3:0]	Output	SDRAM Data Qualifier Mask. If high; on writes data is masked, on reads buffer is tristated.
ACK_L	Output	Acknowledge – indicates when data cycles are active.

Test Bench Description

The test bench for this design, shown below in Figure 2, includes four Verilog modules in addition to the design modules. The top module of the test bench, SDRAM_TB, instantiates the following modules:

- CLK
- STIM
- SDRAM
- SD_TOP (the SDRAM Controller)

Figure 2. Test Bench Diagram



CLK Module

The clock module provides the clock and reset signals to the test bench. Editing the CLK_PERIOD parameter can change the clock frequency. Editing the RESET_TIME parameter can change the duration of reset.

STIM Module

The STIM module provides stimulus to the SDRAM Controller as a microprocessor would. The module consists of an initial block and three tasks. After the reset cycle ends the SDRAM_EN signal is turned on. Then the module waits for the SDRAM_SETUP signal to be active.

After receiving the SDRAM_SETUP signal, write and read tasks are called. These tasks are called three times. The first time tests the first SDRAM memory region, the second time tests the second memory region. Both of these cycles are allowed to finish. The last time the write and read tasks are called, a simulated terminate command is initiated.

SDRAM Module

The SDRAM Module provides a decoder for SDRAM cycles. It echoes to the simulator output screen when SDRAM cycles are decoded. Memory models are available from SDRAM vendors' websites. These provide an actual gate level simulation of the SDRAM.

Other Configurations

Full Page Mode

This design ends all fixed-length burst cycles using the auto-precharge command. Using this mode prevents a full page burst. If full page bursts are desired, the auto-precharge command must be disabled. This is accomplished by leaving Address bit 10 low during the write and read commands. The precharge command must then be used to de-activate the SDRAM row.

CAS Latency

Depending on the clock speed, the CAS latency may have to be increased to three. The designer should look at the requirements for the parts selected and the desired clock frequency to determine what CAS latency is required. If a CAS latency of three is required, move the CAS time, the write enable time and the ACK time out one clock tick in the SD_SIG module.

Row Comparison

If desired, the activated row for each bank of the SDRAM could be stored in registers. This captured value could then be compared to the presently accessed row to see if it is a match. If it is a match, read or write commands could be initiated without activating the row.

If the new row address did not match, a precharge command would have to be issued to de-activate the active row. Then, an activate command would be sent for the new row.

Clock Suspend/Power Down Modes

Clock suspension and power-down modes are not implemented in this design. If desired, the logic would have to be built and connected to the SD_CKE signal.

Design Flow

Simulation

The design was simulated using Model Technology's ModelSim simulator. In this design, the sdram_tb.v file is the top-level file. The test bench files and design files include:

- sdram_tb.v – top level test bench file
- sd_top.v – top level design file
- sd_cnfg.v – configuration design file
- sd_state.v – state machine design file
- sd_rfrsh.v – refresh design file
- sd_sig.v – signal output design file
- clk.v – clock test bench file
- stim.v – stimulus test bench file and
- sdram.v – SDRAM test bench file.

Synthesis

This design was synthesized using Exemplar's Spectrum and Synplify's Synplicity. The output file from either tool will be an EDIF file.

Fitting

The EDIF file is imported into the ispLEVER Development System software and targeted to an ispMACH 4A device. Running the Timing Analyzer shows the expected performance of 153.8 MHz when a 5.5ns device is targeted. Generate timing simulation files for post route simulation.

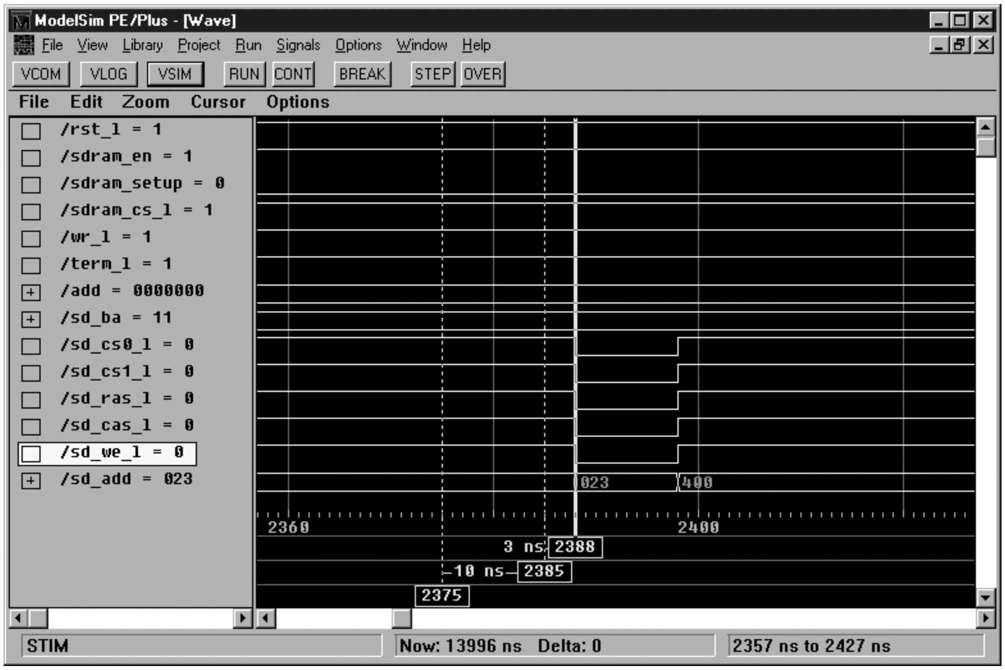
Post Simulation

After the design has been fitted, post route simulations should be run. In newer versions of the synthesis tools, the EDIF file splits buses apart. This requires a different top-level test bench file to be used for post route simulation. The difference in the files is the instantiation of the controller module. This file is called sd_tb1.v.

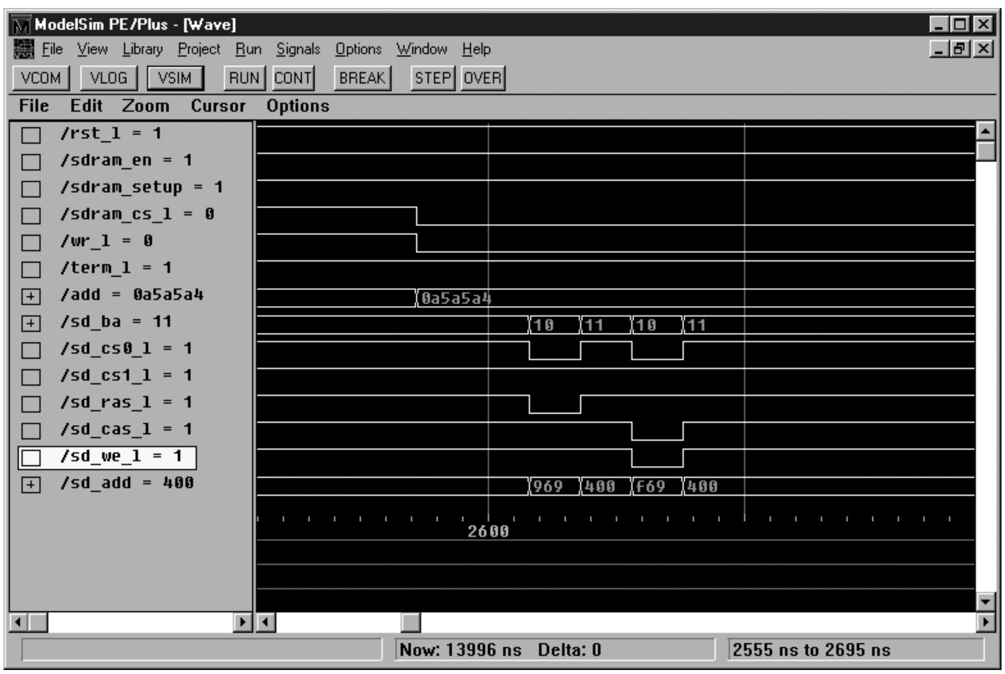
Timing Diagrams

The following timing diagrams were created from Model Technology's ModelSim version 4.7 Simulator. The clock parameter was changed to 10 ns, which yields a 100 MHz solution.

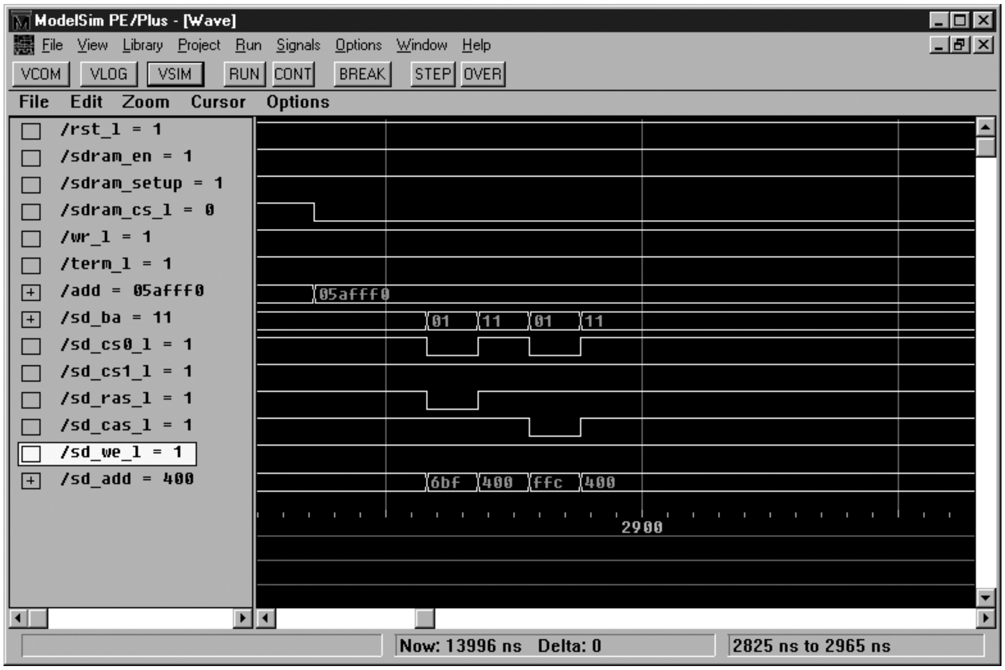
Load Mode Register



Write Cycle



Read Cycle



Lattice also offers a different version of an SDRAM Controller as a Reference Design. The other version, *SDR SDRAM Controller* (RD1010), has the following differences:

- Verilog source code
- Works in the ispMACH 5000VG devices, uses the on-chip programmable PLL to generate SDRAM clock signal from slower system clock
- Calculates min system clocks for timing delay between SDRAM commands , reducing access time
- Dedicated input pin for asynchronous SDRAM refresh request requires no internal counter, saves space

Technical Support Assistance

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