# OSC Module - Lattice Radiant Software

# User Guide

FPGA-IPUG-02065-1.1

February 2020

## Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS and with all faults, and all risk associated with such information is entirely with Buyer. Buyer shall not rely on any data and performance specifications or parameters provided herein. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. No Lattice products should be used in conjunction with mission- or safety-critical or any other application in which the failure of Lattice's product could create a situation where personal injury, death, severe property or environmental damage may occur. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

# Contents

# Figures



# Tables

# 1. Introduction

The Lattice Semiconductor CrossLink-NX™ Oscillator (OSC) Module is designed to produce two clock signals that drive the FPGA clock tree for user-specific applications. The trimmed low frequency oscillator and trimmed high frequency oscillator are also used by the IP sub-system of the FPGA. The low frequency oscillator always run, even at sleep mode.

## 1.1. Quick Facts

Table 1.1 shows a summary of the OSC Module.

**Table 1.1. OSC Module Quick Facts**

| | | |
|---|---|---|
| **IP Requirements** | Supported FPGA Family | CrossLink-NX |
| **Resource Utilization** | Targeted Devices | LIFCL-40, LIFCL-17 |
| | Supported User Interfaces | Native interfaces; please refer to the Signal Descriptions section. |
| **Design Tool Support** | Lattice Implementation | Lattice Radiant® Software 2.0 |
| | Synthesis | Lattice Synthesis Engine (LSE) |
| | | Synopsys® Synplify Pro® for Lattice |
| | Simulation | For the list of supported simulators, see the Lattice Radiant Software 2.0 User Guide. |

## 1.2. Features

The key features of this module are:

- Independent output enable
- Built-in divider with static control
- Dynamic on/off glitchless enable/disable
- Low DC leakage in both Stand-by Mode and in Sleep Mode
- Low frequency oscillator output is 32 kHz +/–10%
- High frequency oscillator output is 450 MHz +/–10% and is controlled by a user-configurable frequency divider.
- Maximum oscillator frequency for user application is 225 MHz
- Active current consumption of 6 uA for LF OSC and 0.3 mA for HF OSC

## 1.3. Conventions

### 1.3.1. Nomenclature

The nomenclature used in this document is based on Verilog HDL.

### 1.3.2. Signal Names

Signal names that end with:

- _*n* are active low
- _*i* are input signals
- _*o* are output signals

### 1.3.3. Attribute Names

Attribute names in this document are formatted in title case and italicized (*Attribute Name*).

# 2. Functional Description

OSC Module includes two accuracy oscillators, which can be individually enabled. One oscillator generates an internal 128 kHz clock used by the IP sub-system. This clock is divided by 4 for user-specific application. The other oscillator provides a clock whose maximum frequency is 450 MHz and hardened dividers allowing optional division from 2 to 256 to scale the output frequency down. The maximum frequency for user application is 450 MHz divided by 2, which is 225 MHz.

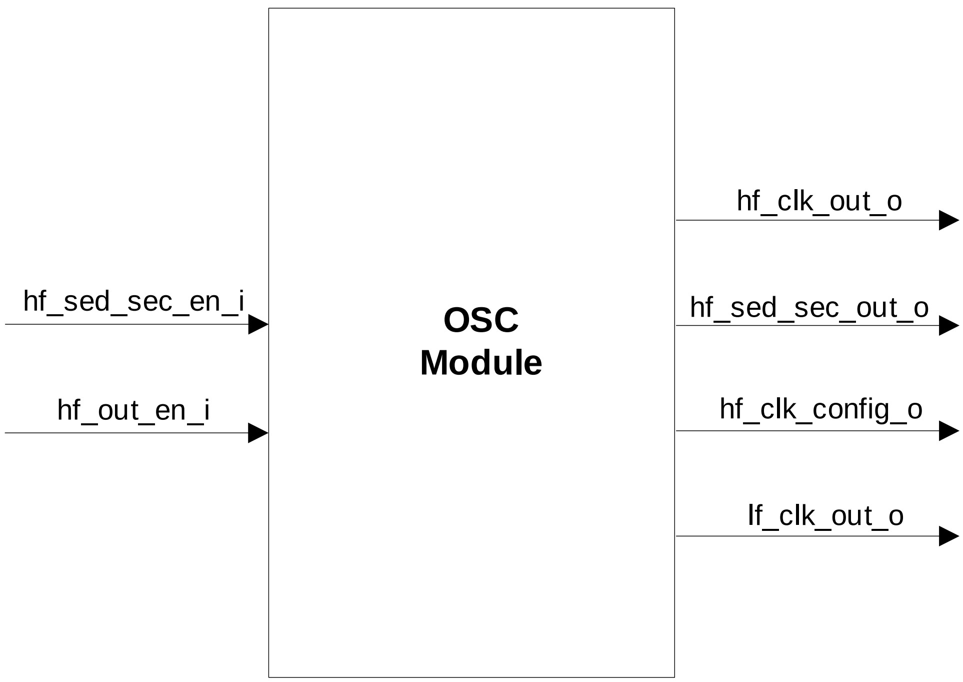


**Figure 2.1. OSC Block Diagram**

## 2.1. Signal Descriptions

**Table 2.1. OSC Module Signal Description**

| Port Name | I/O | Width | Description |
|---|---|---|---|
| **Clock** | | | |
| hf_clk_out_o | Out | 1 | High frequency clock output, enabled by *HFCLK Enable* and controlled by *HFCLK Divider*. |
| lf_clk_out_o | Out | 1 | Low frequency clock output after div4:32 kHz, controlled by *LFCLK Enable*. |
| hf_clk_config_o | Out | 1 | High frequency clock output, enabled by *SEDCLK Enable* and controlled by *SEDCLK Divider*. |
| **Enable Port** | | | |
| hf_out_en_i | In | 1 | Enable port for hf_clock_out_o |
| hf_sed_sec_en_i | In | 1 | Available if *SEDCLK Enable* == ENABLED BY SIGNAL |
| hf_sed_sec_out_o | Out | 1 | Available if *SEDCLK Enable* == ALWAYS ENABLED or *SEDCLK Enable* == ENABLED BY SIGNAL |

## 2.2. Attribute Summary

The configurable attributes of the OSC Module are shown in Table 2.2 and are described in Table 2.3. The attributes can be configured through the IP Catalog's Module/IP wizard of the Lattice Radiant Software.

**Table 2.2. Attributes Table**

| Attribute | Selectable Values | Default | Dependency on Other Attributes |
|---|---|---|---|
| **General** | | | |
| HFCLK Enable | ENABLED<br>DISABLED | ENABLED | — |
| HFCLK Divider | 2-256 | 2 | Active if *HFLCK Enable* == ENABLED |
| HFCLK Frequency(MHz) | N/A | 225 | — |
| LFCLK Enable | DISABLED<br>ENABLED | DISABLED | — |
| LFCLK Frequency (kHz) | N/A | 32 | — |
| SEDCLK Enable | DISABLED<br>ALWAYS ENABLED<br>ENABLED BY SIGNAL | DISABLED | — |
| SEDCLK Divider | 2-256 | 2 | Active if:<br>*SEDCLK Enable* == ALWAYS ENABLED or<br>*SEDCLK Enable* == ENABLED BY SIGNAL |
| SEDCLK Frequency (MHz) | N/A | 225 | — |

**Table 2.3. Attributes Descriptions**

| Attribute | Description |
|---|---|
| **General** | |
| HFCLK Enable | Enables the presence of hf_clk_out_o signal on the generated IP.<br>ENABLED – Signal is available.<br>DISABLED – Signal is unavailable. |
| HFCLK Divider | Specifies the divider of the High Frequency Oscillator. |
| HFCLK Frequency(MHz) | Specifies the HFCLK Frequency, wherein,<br>*HFCLK Frequency* == (450MHz/*HFCLK Divider*).<br>The 450 MHz oscillator is used internally by the IP sub-system. Maximum oscillator frequency for user application is 225 MHz (450 MHz divided by 2) |
| LFCLK Enable | Enables the presence of lf_clk_out_o signal on the generated IP.<br>ENABLED – Signal is available.<br>DISABLED – Signal is unavailable. |
| LFCLK Frequency (kHz) | Specifies the LFCLK Frequency after div4 which means that the internal LFCLK (128kHz) is divided by 4. Fixed attribute value is 32 kHz. |
| SEDCLK Enable | Enables the presence of hf_sed_sec_en_i and hf_sed_sec_out_o signal on the generated IP.<br>ALWAYS ENABLED – hf_sed_sec_en_i signal is unavailable and is tied to 1'b0, hf_sed_sec_out_o signal available.<br>ENABLED BY SIGNAL: hf_sed_sec_en_i and hf_sed_sec_out_o signals are available.<br>DISABLED – hf_sed_sec_en_i and hf_sed_sec_out_o signals are unavailable; input signal is tied to 1'b0 and output signal is dangling. |
| SEDCLK Divider | Specifies the frequency divider of the SEDCLK. |
| SEDCLK Frequency (MHz) | Specifies the SEDCLK Frequency wherein:<br>*SEDCLK Frequency* == (450 MHz/*SEDCLK Divider*). |

# 3. IP Generation, Synthesis, and Validation

This section provides information on how to generate and synthesize this module using the Lattice Radiant Software. For more on Lattice Radiant Software, please refer to the Lattice Radiant Software 2.0 User Guide and relevant tutorials.

## 3.1. Licensing the IP

No license is required for this module.

## 3.2. Generating and Synthesizing the IP

The Lattice Radiant Software allows you to customize and generate modules and IPs and integrate them into the device's architecture. The procedure for generating the OSC Module in Lattice Radiant Software is described below.

To generate the OSC Module:

1. Create a new Lattice Radiant Software project or open an existing project.
2. In the **IP Catalog** tab, double-click on **OSC** under **Module, Architecture_Modules** category. The **Module/IP Block Wizard** opens as shown in Figure 3.1. Enter values in the **Instance name** and the **Create in** fields and click **Next**.

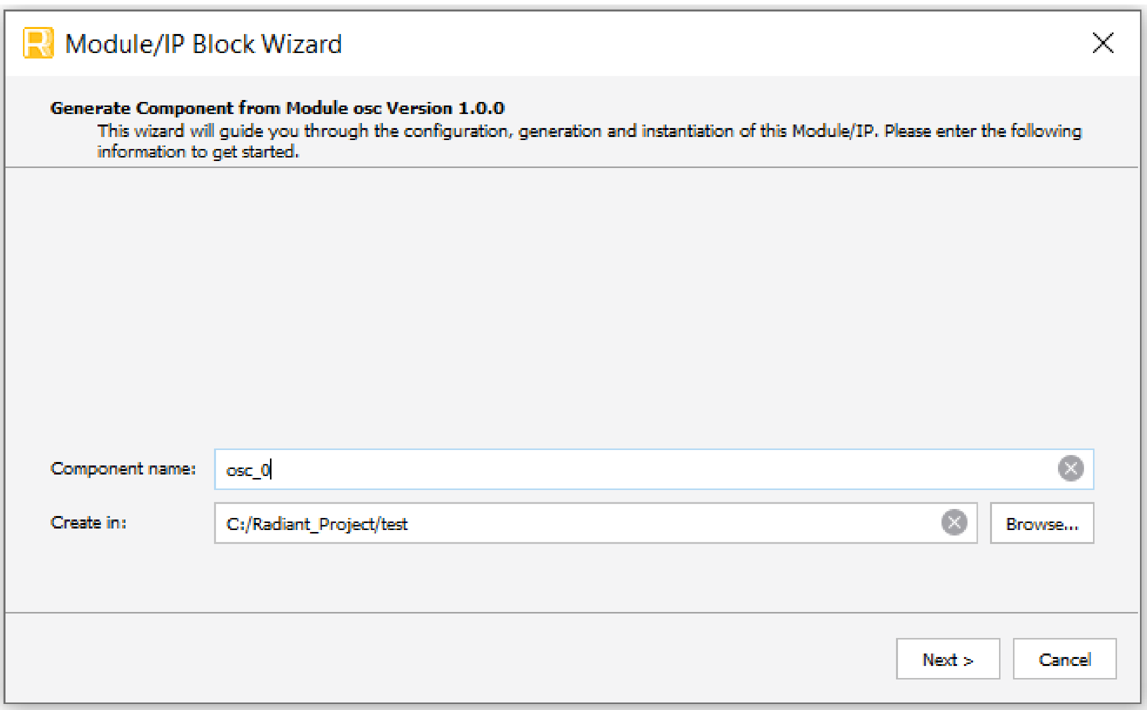


**Figure 3.1. Module/IP Block Wizard**

3. In the module's dialog box of the **Module/IP Block Wizard** window, customize the selected OSC Module using drop-down menus and check boxes. As a sample configuration, see Figure 3.2. For configuration options, see the Attribute Summary section.

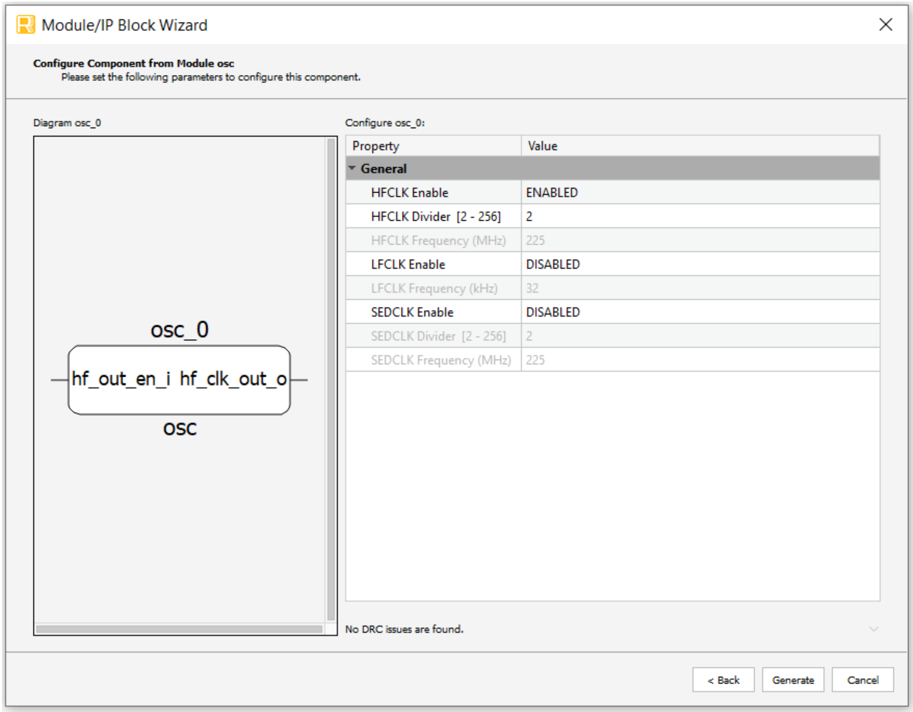


**Figure 3.2. Configure User Interface of OSC Module**

4. Click **Generate**. The **Check Generating Result** dialog box opens, showing design block messages and results as shown in Figure 3.3.

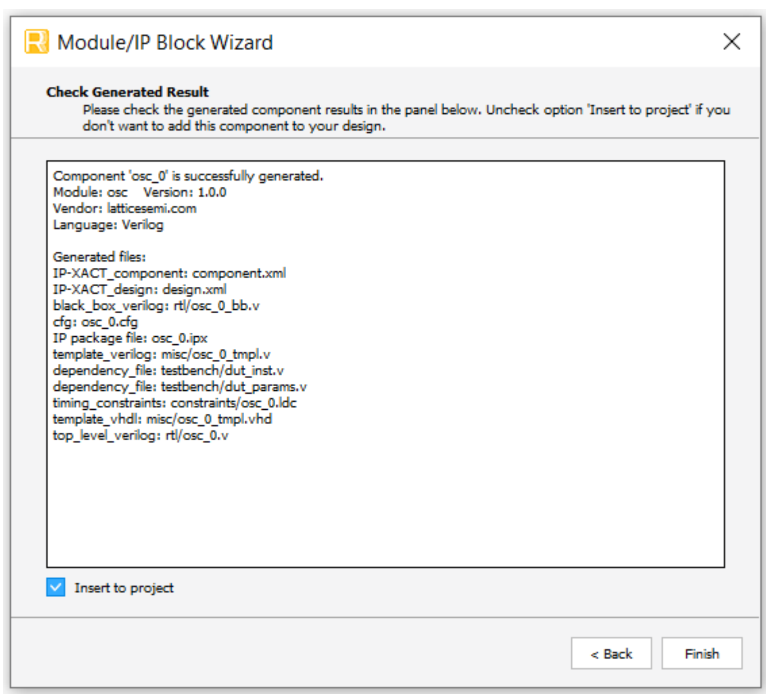


**Figure 3.3. Check Generating Result**

5. Click the **Finish** button. All the generated files are placed under the directory paths in the **Create in** and the **Instance name** fields shown in Figure 3.1.

The generated OSC Module package includes the black box (<Instance Name>_bb.v) and instance templates (<Instance Name>_tmpl.v/vhd) that can be used to instantiate the module in a top-level design. An example RTL top-level reference source file (<Instance Name>.v) that can be used as an instantiation template for the module is also provided. You may also use this top-level reference as the starting template for the top-level for their complete design. The generated files are listed in Table 3.1.

**Table 3.1. Generated File List**

| Attribute | Description |
|---|---|
| <Instance Name>.ipx | This file contains the information on the files associated to the generated IP. |
| <Instance Name>.cfg | This file contains the attribute values used in IP configuration. |
| component.xml | Contains the ipxact:component information of the IP. |
| design.xml | Documents the configuration attributes of the IP in IP-XACT 2014 format. |
| rtl/<Instance Name>.v | This file provides an example RTL top file that instantiates the module. |
| rtl/<Instance Name>_bb.v | This file provides the synthesis black box. |
| misc/<Instance Name>_tmpl.v<br>misc /<Instance Name>_tmpl.vhd | These files provide instance templates for the module. |

## 3.3. Running the Functional Simulation

Running functional simulation can be performed after the IP is generated.

To run Verilog simulation:

1. Click the  button located on the Toolbar to initiate the Simulation Wizard shown in Figure 3.4.

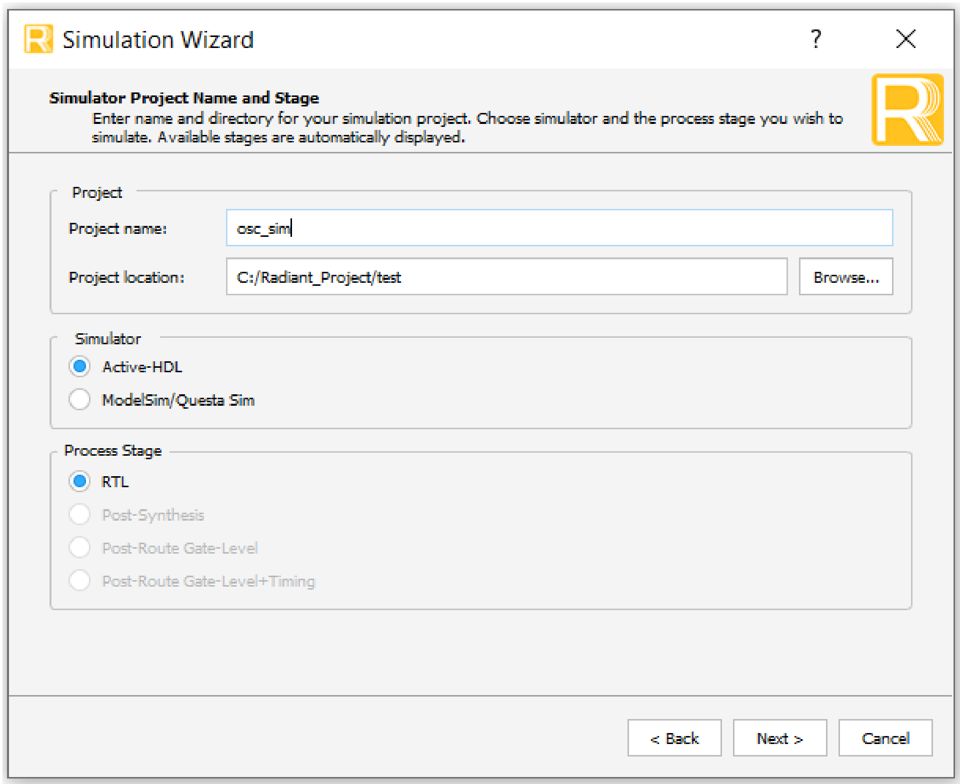


**Figure 3.4. Simulation Wizard**

2. Click **Next** to open the **Add and Reorder Source** window as shown in Figure 3.5.

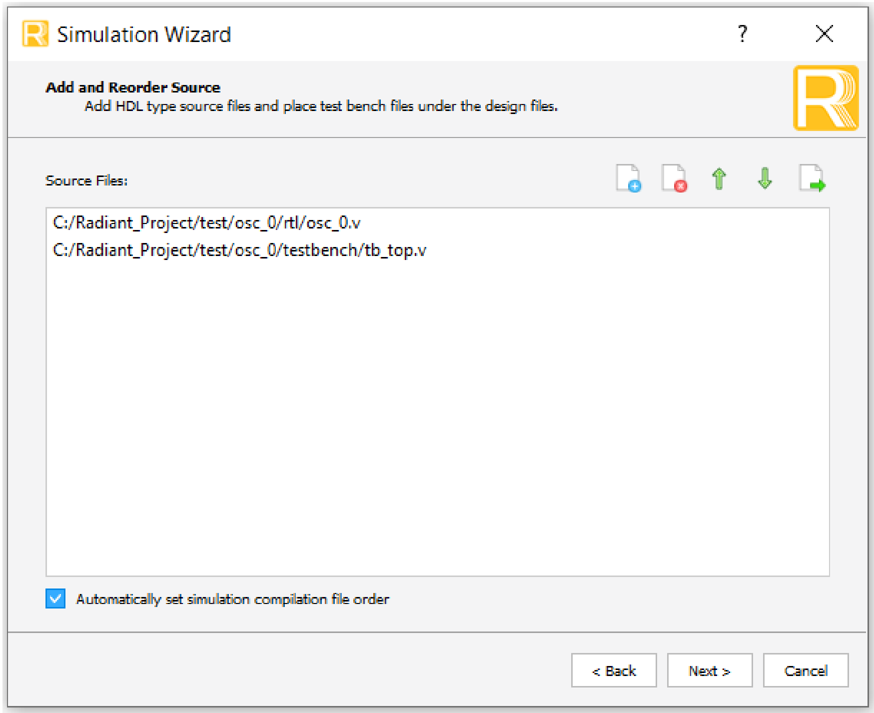


**Figure 3.5. Adding and Reordering Source**

3. Click **Next**. The **Summary** window is shown. Click **Finish** to run the simulation.

   **Note:** It is necessary to follow the procedure above until it is fully automated in the Lattice Radiant Software Suite.

   The results of the simulation in our example are provided in Figure 3.6.

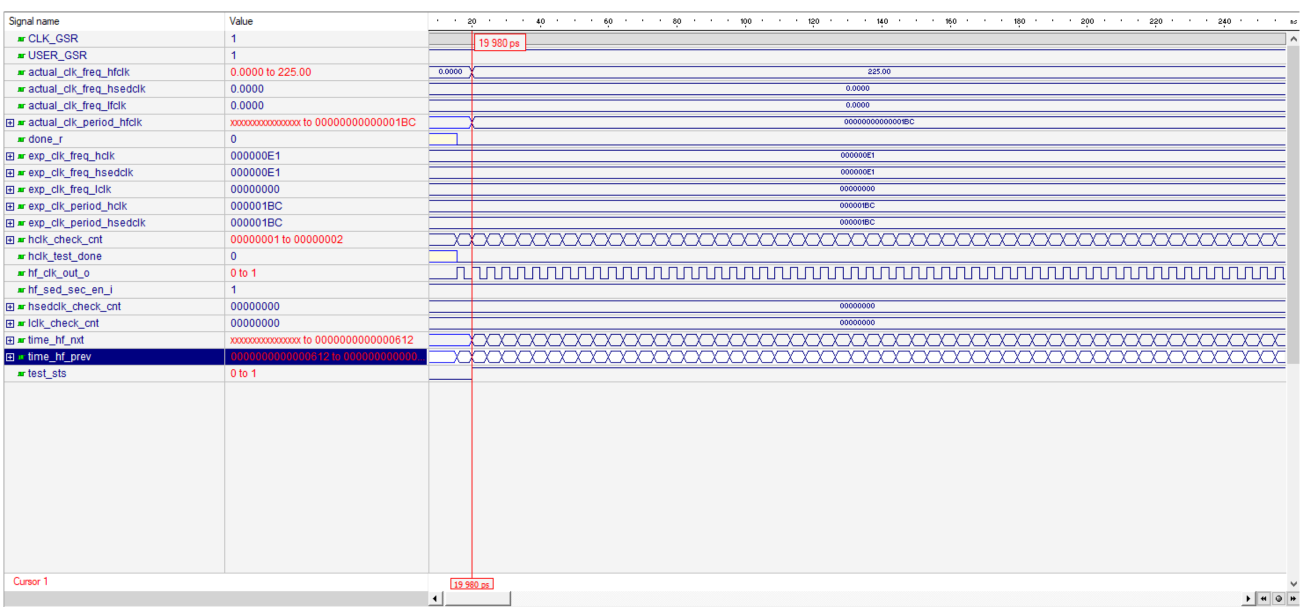


**Figure 3.6. Simulation Waveform**

# References

For complete information on Lattice Radiant Project-Based Environment, Design Flow, Implementation Flow and Tasks, as well as on the Simulation Flow, see the Lattice Radiant Software 2.0 User Guide.

# Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

# Revision History

**Document Revision 1.1, Lattice Radiant SW version 2.0, February 2020**

| Section | Change Summary |
|---|---|
| Introduction | Updated Table 1.1 to add LIFCL-17 as targeted device. |
| Functional Description | • Updated Figure 2.1. OSC Block Diagram.<br>• Updated Table 2.1. OSC Module Signal Description. |
| IP Generation, Synthesis, and Validation | Updated Figure 3.2. Configure User Interface of OSC Module. |

**Document Revision 1.0, Lattice Radiant SW version 2.0, November 2019**

| Section | Change Summary |
|---|---|
| All | Changed document status from Preliminary to final. |
| Introduction | Added *Maximum oscillator frequency for user application is 225MHz*in Features section. |
| IP Generation, Synthesis, and Validation | Updated Figure 3.6. Simulation Waveform. |

**Document Revision 0.80, Lattice Radiant SW version 2.0, October 2019**

| Section | Change Summary |
|---|---|
| All | Preliminary release. |

www.latticesemi.com