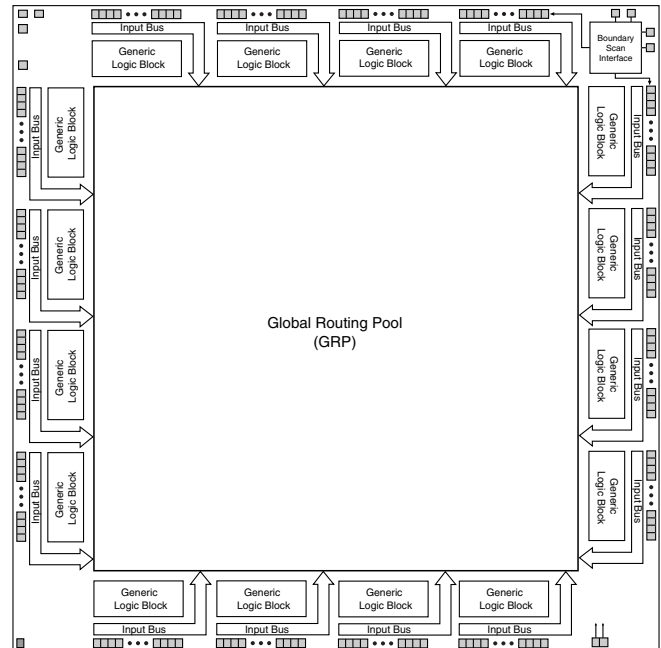


## Features

- **SuperWIDE HIGH DENSITY IN-SYSTEM PROGRAMMABLE LOGIC**
  - 3.3V Power Supply
  - User Selectable 3.3V/2.5V I/O
  - 24,000 PLD Gates / 512 Macrocells
  - Up to 288 I/O Pins
  - 512 Registers
  - High-Speed Global Interconnect
  - SuperWIDE 32 Generic Logic Block (GLB) Size for Optimum Performance
  - SuperWIDE Input Gating (68 Inputs) for Fast Counters, State Machines, Address Decoders, etc.
  - PCB Efficient Ball Grid Array (BGA) Package Options
- **HIGH PERFORMANCE E<sup>2</sup>CMOS<sup>®</sup> TECHNOLOGY**
  - $f_{max} = 110$  MHz Maximum Operating Frequency
  - $t_{pd} = 8.5$  ns Propagation Delay
  - TTL/3.3V/2.5V Compatible Input Thresholds and Output Levels
  - Electrically Erasable and Reprogrammable
  - Non-Volatile
  - Programmable Speed/Power Logic Path Optimization
- **IN-SYSTEM PROGRAMMABLE**
  - Increased Manufacturing Yields, Reduced Time-to-Market, and Improved Product Quality
  - Reprogram Soldered Devices for Faster Debugging
- **100% IEEE 1149.1 BOUNDARY SCAN TESTABLE AND 3.3V IN-SYSTEM PROGRAMMABLE**
- **ARCHITECTURE FEATURES**
  - Enhanced Pin-Locking Architecture with Single-Level Global Routing Pool and SuperWIDE GLBs
  - Wrap Around Product Term Sharing Array Supports up to 35 Product Terms Per Macrocell
  - Macrocells Support Concurrent Combinatorial and Registered Functions
  - Macrocell Registers Feature Multiple Control Options Including Set, Reset and Clock Enable
  - Four Dedicated Clock Input Pins Plus Macrocell Product Term Clocks
  - Slew and Skew Programmable I/O (SASPI/O) Supports Programmable Bus Hold, Pull-up, Open Drain and Slew and Skew Rate Options
  - Six Global Output Enable Terms, Two Global OE Pins and One Product Term OE per Macrocell
- **ispDesignEXPERT™ – LOGIC COMPILER AND COMPLETE ISP DEVICE DESIGN SYSTEMS FROM HDL SYNTHESIS THROUGH IN-SYSTEM PROGRAMMING**
  - Superior Quality of Results
  - Tightly Integrated with Leading CAE Vendor Tools
  - Productivity Enhancing Timing Analyzer, Explore Tools, Timing Simulator and ispANALYZER
  - PC and UNIX Platforms

## Functional Block Diagram



## ispLSI 5000V Description

The ispLSI 5000V Family of In-System Programmable High Density Logic Devices is based on Generic Logic Blocks (GLBs) of 32 registered macrocells and a single Global Routing Pool (GRP) structure interconnecting the GLBs.

Outputs from the GLBs drive the Global Routing Pool (GRP) between the GLBs. Switching resources are provided to allow signals in the Global Routing Pool to drive any or all the GLBs in the device. This mechanism allows fast, efficient connections across the entire device.

Each GLB contains 32 macrocells and a fully populated, programmable AND-array with 160 logic product terms and 5 extra control product terms. The GLB has 68 inputs from the Global Routing Pool which are available in both true and complement form for every product term. The 160 product terms are grouped in 32 sets of five and sent into a Product Term Sharing Array (PTSA) which allows sharing up to a maximum of 35 product terms for a single function. Alternatively, the PTSA can be bypassed for functions of five product terms or less. The five extra product terms are used for shared GLB controls, set, reset, clock, clock enable and output enable.

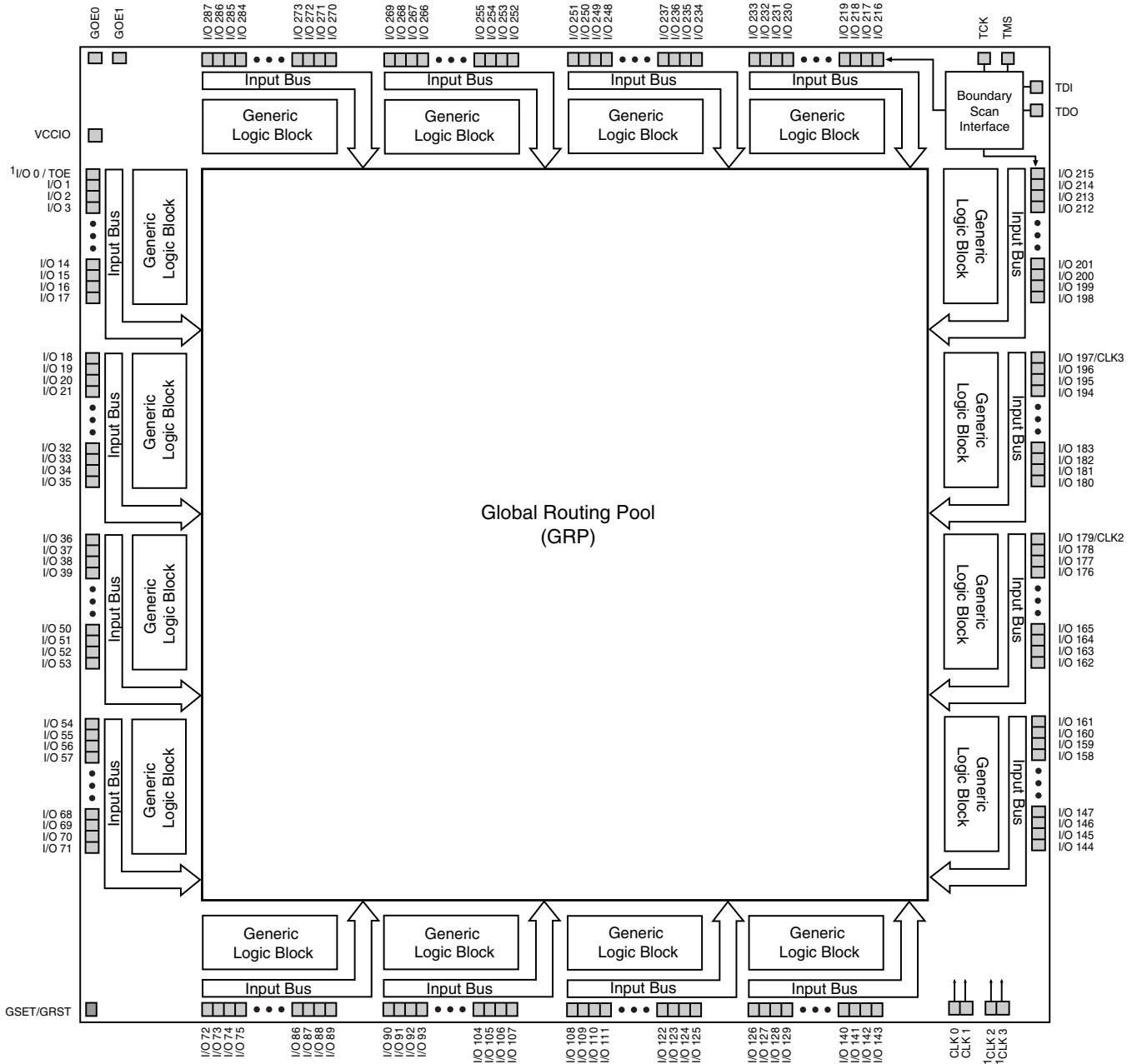
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LATTICE SEMICONDUCTOR CORP., 5555 Northeast Moore Ct., Hillsboro, Oregon 97124, U.S.A.  
Tel. (503) 268-8000; 1-800-LATTICE; FAX (503) 268-8556; <http://www.latticesemi.com>

May 1999

**Functional Block Diagram**

**Figure 1. ispLSI 5512V Functional Block Diagram (388 BGA Option)**



1. CLK2, CLK3 and TOE signals are multiplexed with I/O signals. Which I/O is multiplexed is determined by the package type used – see table below.

Package Type	Multiplexed Signals		
388 BGA	I/O 179 / CLK2	I/O 197 / CLK3	I/O 0 / TOE

## ispLSI 5000V Description (Continued)

The 32 registered macrocells in the GLB are driven by the 32 outputs from the PTSA or the PTSA bypass. Each macrocell contains a programmable XOR gate, a programmable register/latch/toggle flip-flop and the necessary clocks and control logic to allow combinatorial or registered operation. The macrocells each have two outputs, which can be fed back through the Global Routing Pool. This dual output capability from the macrocell allows efficient use of the hardware resources. One output can be a registered function for example, while the other output can be an unrelated combinatorial function. A direct register input from the I/O pad facilitates efficient use of this feature to construct high-speed input registers.

Macrocell registers can be clocked from one of several global or product term clocks available on the device. A global and product term clock enable is also provided, eliminating the need to gate the clock to the macrocell registers. Reset and preset for the macrocell register is provided from both global and product term signals. The macrocell register can be programmed to operate as a D-type register, a D-type latch or a T-type flip flop.

The 32 outputs from the GLB can drive both the Global Routing Pool and the device I/O cells. The Global Routing Pool contains one line from each macrocell output and one line from each I/O pin.

The input buffer threshold has programmable TTL/3.3V/2.5V compatible levels. The output driver can source 4mA and sink 8mA in 3.3V mode. The output drivers have a separate VCCIO reference input which is independent of the main VCC supply for the device. This feature allows the output drivers to drive either 3.3V or 2.5V output levels while the device logic and the output current drive is always powered from 3.3V. The output drivers also provide individually programmable edge rates and open drain capability. A programmable pullup

resistor is provided to tie off unused inputs and a programmable bus-hold latch is available to hold tristate outputs in their last valid state until the bus is driven again by some device.

The ispLSI 5000V Family features 3.3V, non-volatile in-system programmability for both the logic and the interconnect structures, providing the means to develop truly reconfigurable systems. Programming is achieved through the industry standard IEEE 1149.1-compliant Boundary Scan interface. Boundary Scan test is also supported through the same interface.

An enhanced, multiple cell security scheme is provided that prevents reading of the JEDEC programming file when secured. After the device has been secured using this mechanism, the only way to clear the security is to execute a bulk-erase instruction.

## ispLSI 5000V Family Members

The ispLSI 5000V family ranges from 256 macrocells to 512 macrocells and operates from a 3.3V power supply. All family members will be available with multiple package options. The ispLSI 5000V family device matrix showing the various bondout options is shown in the table below.

The interconnect structure (GRP) is very similar to Lattice's existing 1000, 2000 and 3000 families, but with an enhanced interconnect structure for optimal pin locking and logic routing. The ispLSI 5000V family does not, however, use registered I/O cells or an Output Routing Pool.

**Table 1. ispLSI 5000V Family**

Device	GLBs	Macrocells	Package Type			
			208 BGA*	208 PQFP	272 BGA	388 BGA
ispLSI 5256V	8	256	144 I/O	144 I/O	192 I/O	—
ispLSI 5384V	12	384	144 I/O	144 I/O	192 I/O	288 I/O
ispLSI 5512V	16	512	—	—	—	288 I/O

\*1.0mm ball pitch Fine Pitch BGA

Figure 2. ispLSI 5512V Block Diagram (288 I/O Version)

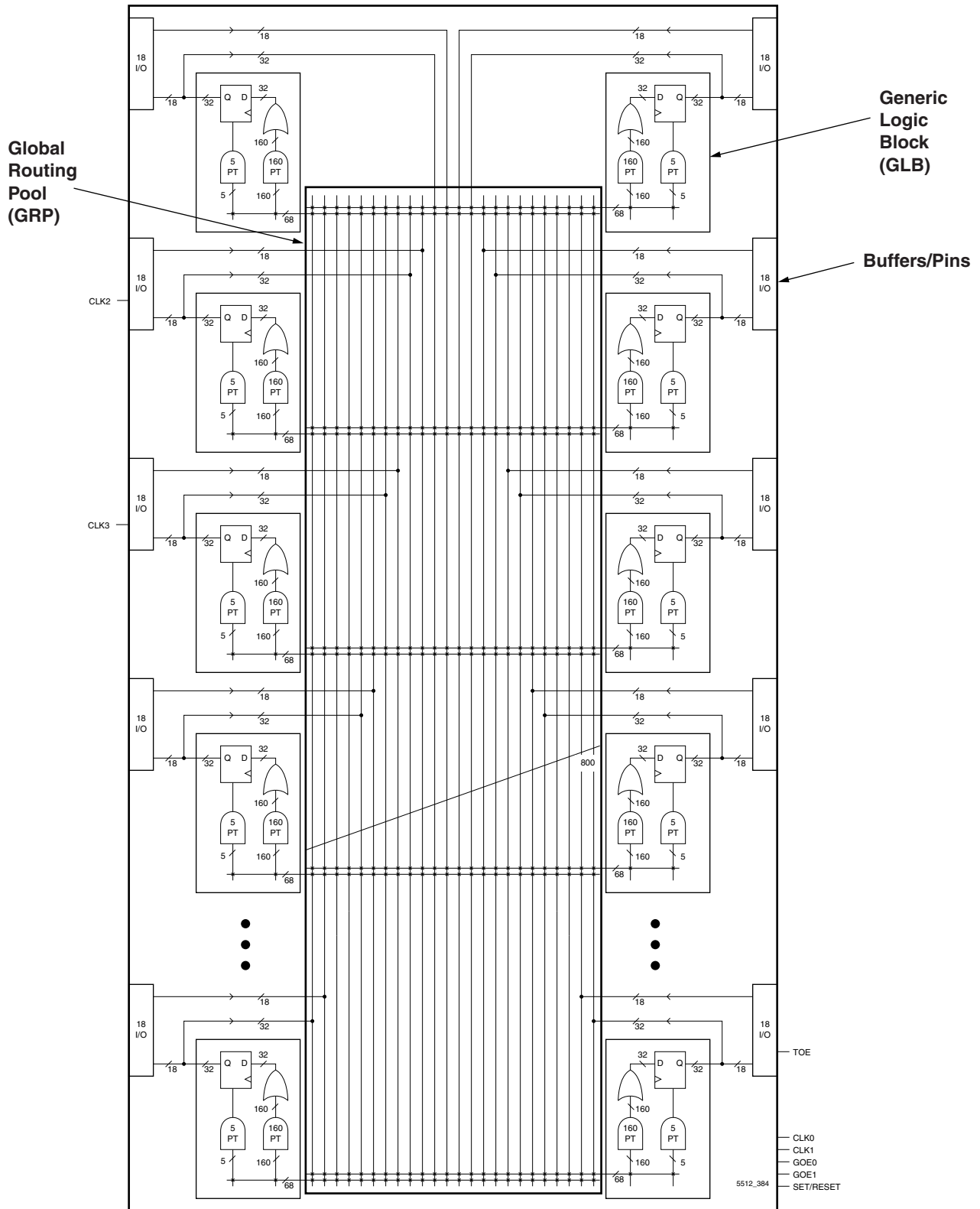


Figure 3. ispLSI 5000V Generic Logic Block (GLB)

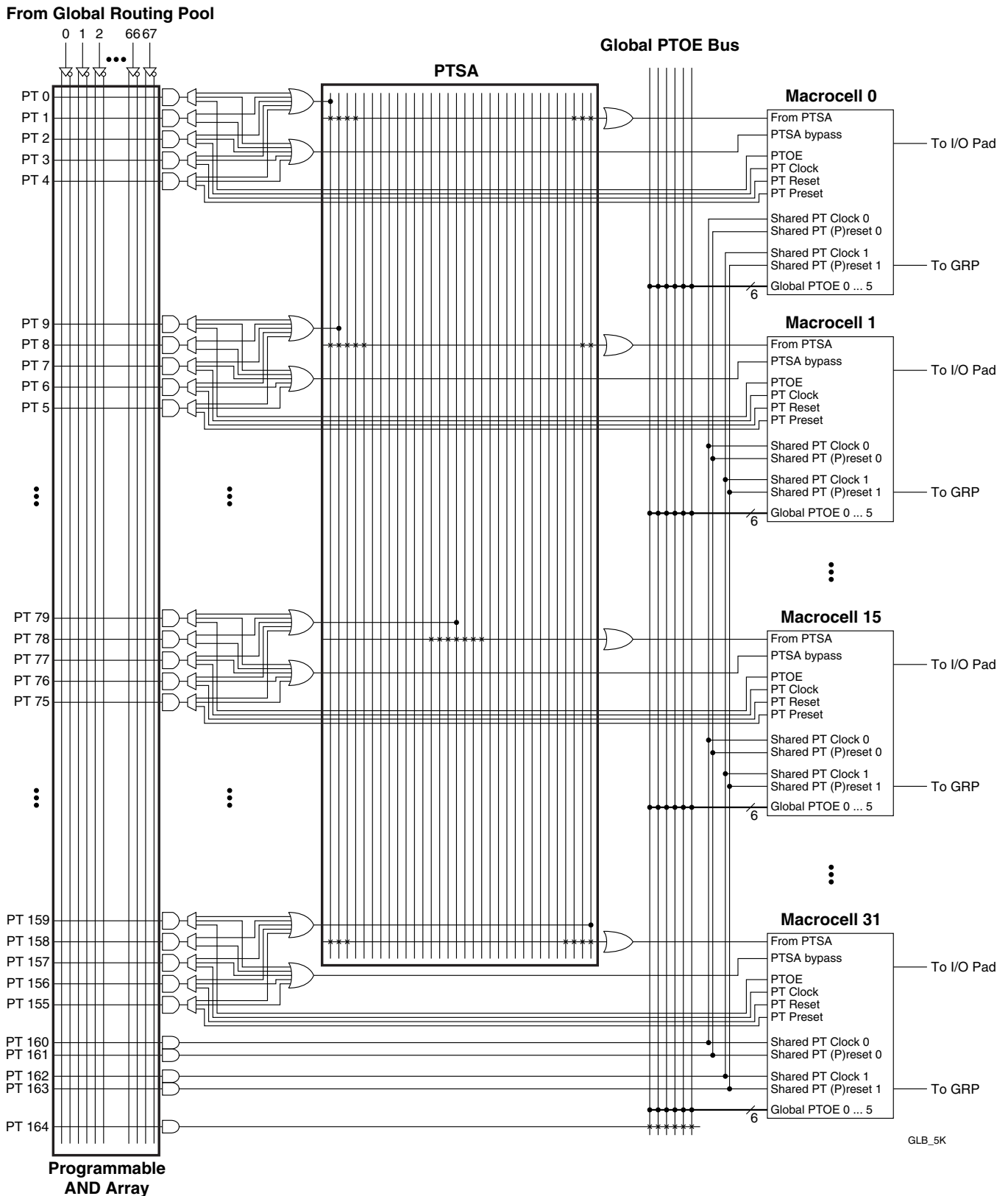
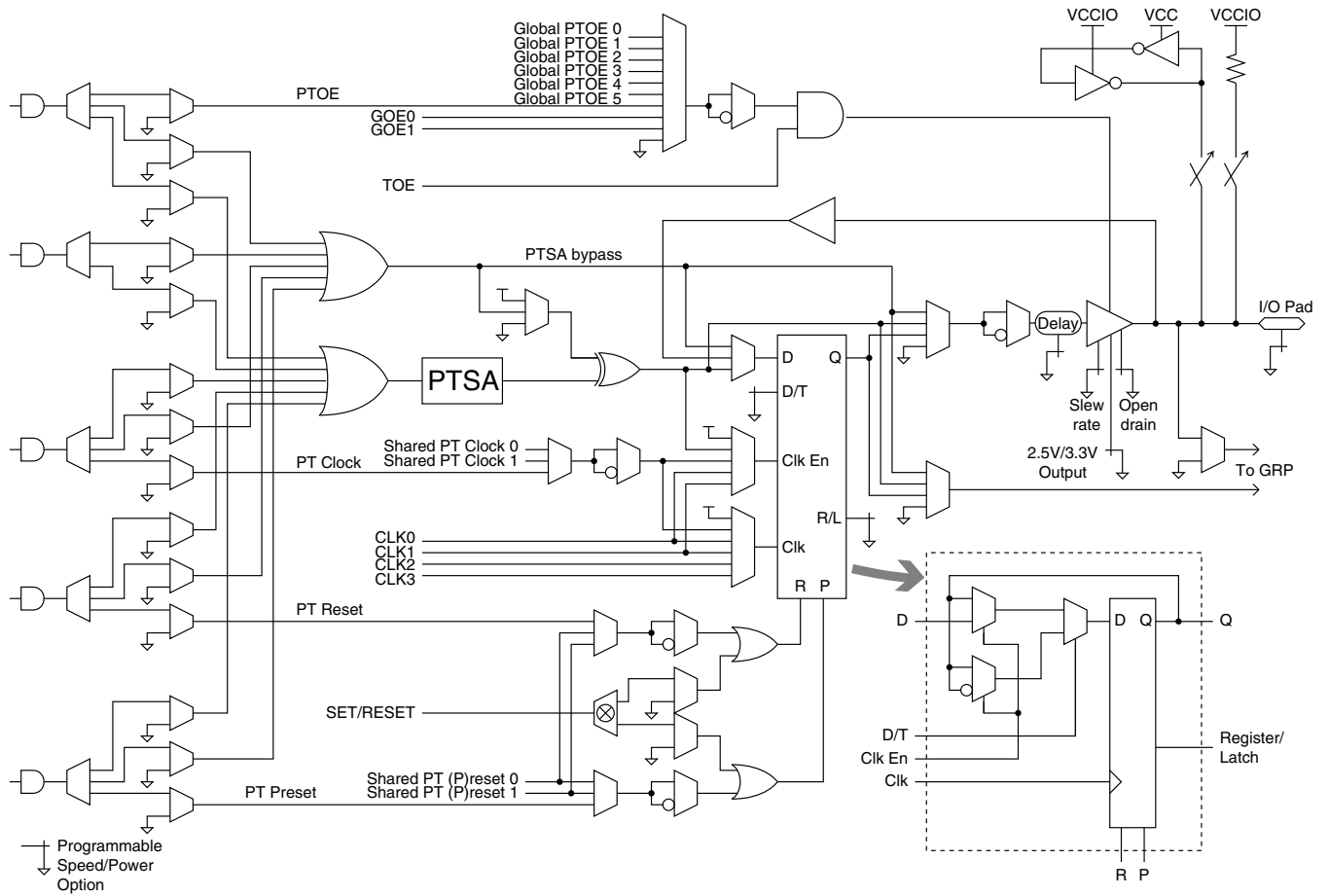


Figure 4. ispLSI 5000V Macrocell



**Global Clock Distribution**

The ispLSI 5000V family has four dedicated clock input pins - CLK0 - CLK3. CLK0 input is used as the dedicated master clock that has the lowest internal clock skew with no clock inversion to maintain the fastest internal clock

speed. The clock inversion is available on the remaining CLK1 - CLK3 signals. By sharing the pins with the I/O pins, CLK2 and CLK3 can not only be inverted but also is available for logic implementation through GRP signal routing. Figure 5 shows these different clock distribution options.

**Figure 5. ispLSI 5000V Global Clock Structure**

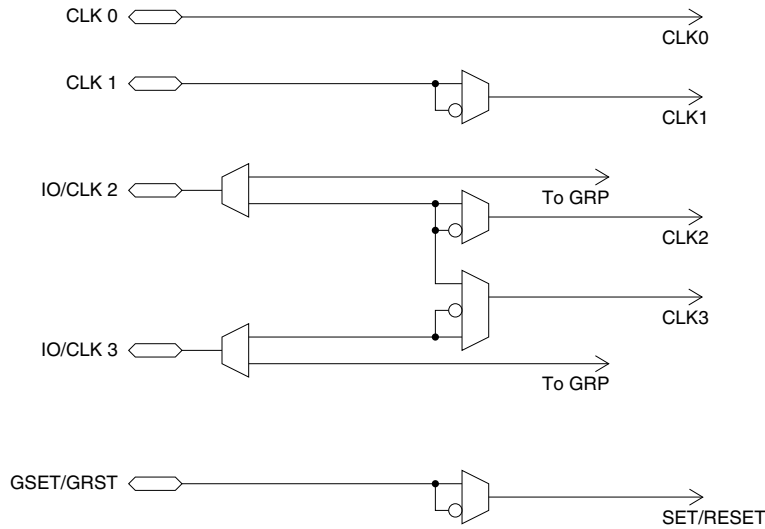


Figure 6. Boundary Scan Register Circuit for I/O Pins

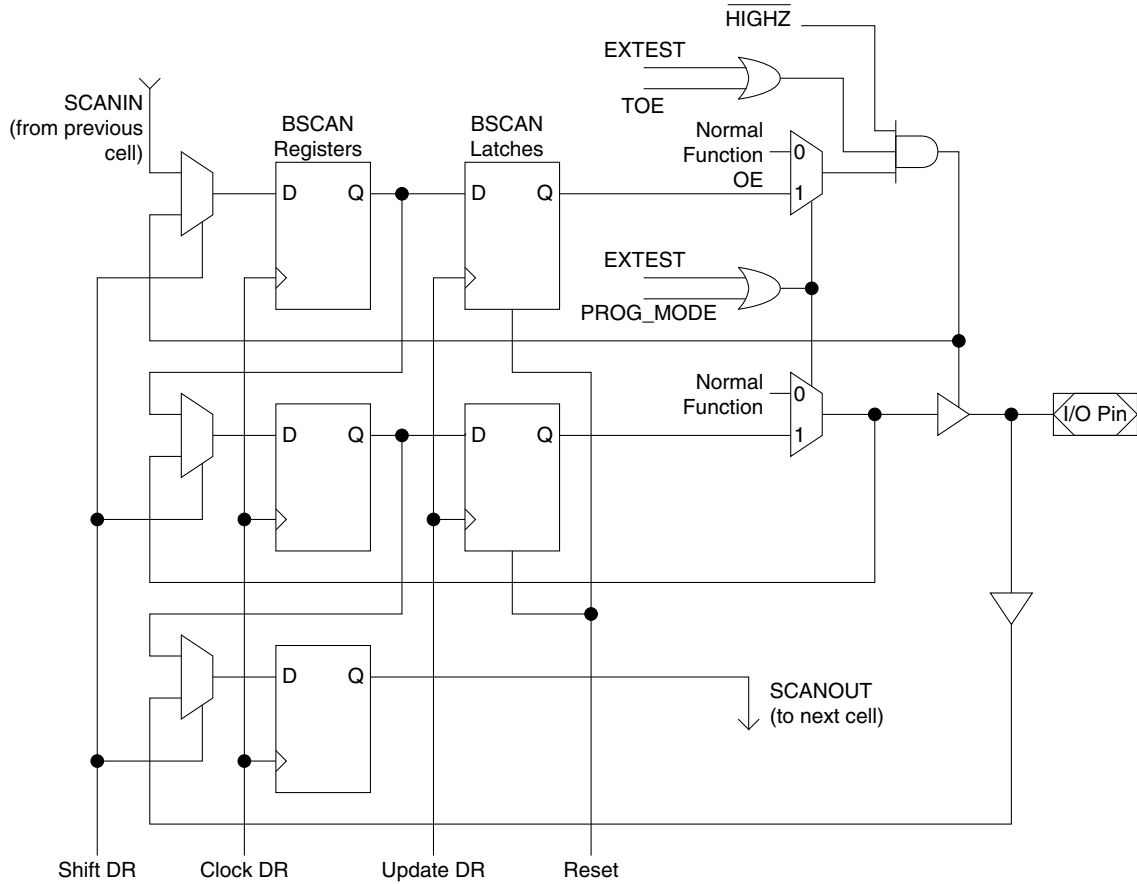
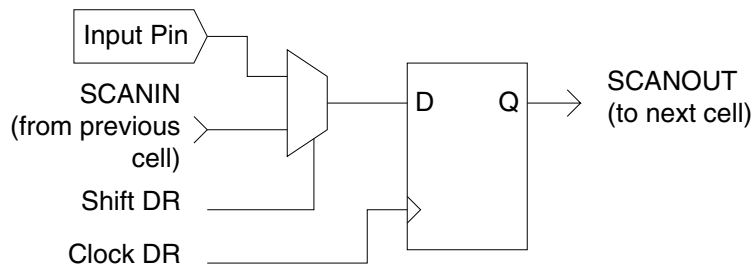
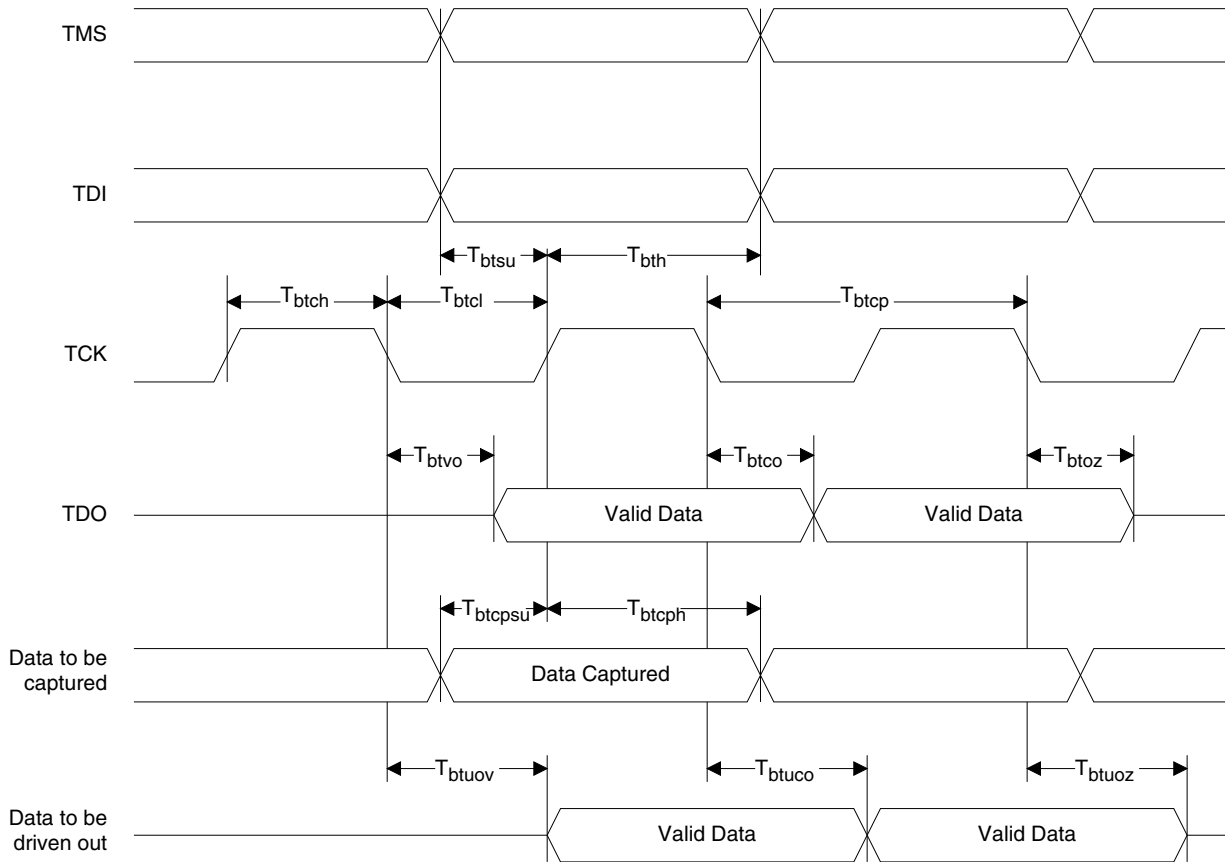


Figure 7. Boundary Scan Register Circuit for Input-Only Pins





**Figure 8. Boundary Scan Waveforms and Timing Specifications**



SYMBOL	PARAMETER	MIN	MAX	UNITS
$t_{btcp}$	TCK [BSCAN test] clock pulse width	125	–	ns
$t_{btch}$	TCK [BSCAN test] pulse width high	62.5	–	ns
$t_{btcl}$	TCK [BSCAN test] pulse width low	62.5	–	ns
$t_{btsu}$	TCK [BSCAN test] setup time	20	–	ns
$t_{bth}$	TCK [BSCAN test] hold time	25	–	ns
$t_{rf}$	TCK [BSCAN test] rise and fall time	50	–	mV/ns
$t_{btco}$	TAP controller falling edge of clock to valid output	–	25	ns
$t_{btoz}$	TAP controller falling edge of clock to data output disable	–	25	ns
$t_{btvo}$	TAP controller falling edge of clock to data output enable	–	25	ns
$t_{btcpu}$	BSCAN test Capture register setup time	20	–	ns
$t_{btcpu}$	BSCAN test Capture register hold time	25	–	ns
$t_{btuco}$	BSCAN test Update reg, falling edge of clock to valid output	–	50	ns
$t_{btuoz}$	BSCAN test Update reg, falling edge of clock to output disable	–	50	ns
$t_{btuov}$	BSCAN test Update reg, falling edge of clock to output enable	–	50	ns

## Absolute Maximum Ratings 1, 2

Supply Voltage  $V_{CC}$  ..... -0.5 to +5.4V  
 Input Voltage Applied ..... -0.5 to +5.6V  
 Tri-Stated Output Voltage Applied ..... -0.5 to +5.6V  
 Storage Temperature ..... -65 to 150°C  
 Case Temp. with Power Applied ..... -55 to 125°C  
 Max. Junction Temp. ( $T_J$ ) with Power Applied ... 150°C

1. Stresses above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).
2. Compliance with the Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM is a requirement.

## DC Recommended Operating Condition

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	
$V_{CC}$	Supply Voltage	Commercial $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$	3.00	3.60	V
		Industrial $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	3.00	3.60	V
$V_{CCIO}$	I/O Reference Voltage	2.3	3.60	V	

Table 2 - 0005/5000

## Capacitance ( $T_A=25^\circ\text{C}, f=1.0\text{ MHz}$ )

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
$C_1$	I/O Capacitance	10	pf	$V_{CC} = 3.3\text{V}, V_{I/O} = 2.0\text{V}$
$C_2$	Clock Capacitance	10	pf	$V_{CC} = 3.3\text{V}, V_{CK} = 2.0\text{V}$
$C_3$	Global Input Capacitance	10	pf	$V_{CC} = 3.3\text{V}, V_G = 2.0\text{V}$

Table 2 - 0006/5384

## Erase Reprogram Specification

PARAMETER	MINIMUM	MAXIMUM	UNITS
ispLSI Erase/Reprogram Cycles	10000	–	Cycles

Table 2-0008/3320

**Switching Test Conditions**

Input Pulse Levels	GND to $V_{CCIO_{min}}$
Input Rise and Fall Time	$\leq 1.5ns$ 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See figure

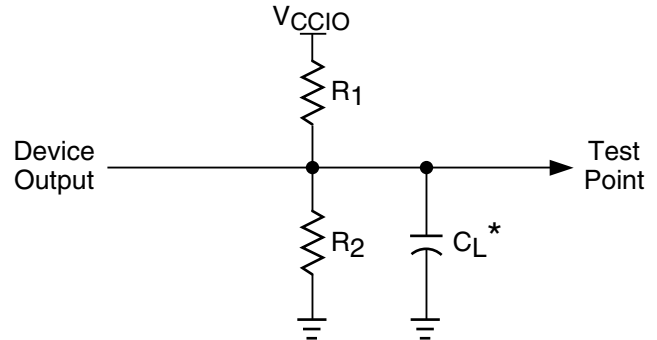
3-state levels are measured 0.5V from steady-state active level. Table 2 - 0003/5384

**Output Load Conditions (See figure 8)**

		3.3V		2.5V		
TEST CONDITION		R1	R2	R1	R2	CL
A		316Ω	348Ω	511Ω	475Ω	35pF
B	Active High	∞	348Ω	∞	475Ω	35pF
	Active Low	316Ω	∞	511Ω	∞	35pF
C	Active High to Z at $V_{OH}-0.5V$	∞	348Ω	∞	475Ω	5pF
	Active Low to Z at $V_{OL}+0.5V$	316Ω	∞	511Ω	∞	5pF
D	Slow Slew	∞	∞	∞	∞	35pF

Table 2 - 0004A/5384

**Figure 9. Test Load**



\*  $C_L$  includes Test Fixture and Probe Capacitance.

0213D

**DC Electrical Characteristics for 3.3V Range**

**Over Recommended Operating Conditions**

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. <sup>1</sup>	MAX.	UNITS
$V_{CCIO}$	I/O Reference Voltage		3.0	–	3.6	V
$V_{IL}$	Input Low Voltage	$V_{OH} \leq V_{OUT}$ or $V_{OUT} \leq V_{OL(max)}$	-0.3	–	0.8	V
$V_{IH}$	Input High Voltage	$V_{OH} \leq V_{OUT}$ or $V_{OUT} \leq V_{OL(max)}$	2.0	–	5.25	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 8\text{ mA}$	–	–	0.4	V
$V_{OH}$	Output High Voltage	$I_{OH} = -4\text{ mA}$	2.4	–	–	V

Table 2 - 0007/5512

1. Typical values are at  $V_{CC} = 3.3V$  and  $T_A = 25^\circ C$ .

**DC Electrical Characteristics for 2.5V Range**
**Over Recommended Operating Conditions**

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V <sub>CCIO</sub>	I/O Reference Voltage		2.3	–	2.7	V
V <sub>IL</sub>	Input Low Voltage	$V_{OH(min)} \leq V_{OUT}$ or $V_{OUT} \leq V_{OL(max)}$	-0.3	–	0.7	V
V <sub>IH</sub>	Input High Voltage	$V_{OH(min)} \leq V_{OUT}$ or $V_{OUT} \leq V_{OL(max)}$	1.7	–	5.25	V
V <sub>OL</sub>	Output Low Voltage	$V_{CCIO=min}, V_{IN}=V_{IH}$ or $V_{IL}, I_{OL}=100\mu A$	–	–	0.2	V
		$V_{CCIO=min}, V_{IN}=V_{IH}$ or $V_{IL}, I_{OL}=2mA$	–	–	0.7	V
V <sub>OH</sub>	Output High Voltage	$V_{CCIO=min}, V_{IN}=V_{IH}$ or $V_{IL}, I_{OH}=-100\mu A$	2.1	–	–	V
		$V_{CCIO=min}, V_{IN}=V_{IH}$ or $V_{IL}, I_{OH}=-2mA$	1.7	–	–	V

2.5V/5512

**DC Electrical Characteristics**
**Over Recommended Operating Conditions**

SYMBOL	PARAMETER	CONDITION	MIN.	TYP. <sup>1</sup>	MAX.	UNITS
I <sub>IL</sub>	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL(Max.)}$	–	–	-10	μA
I <sub>IH</sub>	Input or I/O High Leakage Current	$(V_{CCIO}-0.2)V \leq V_{IN} \leq V_{CCIO}$	–	–	10	μA
		$V_{CCIO} \leq V_{IN} \leq 5.25V$	–	–	50	μA
I <sub>PU</sub> <sup>2</sup>	I/O Active Pullup Current	$0V \leq V_{IN} \leq V_{IL}$	–	–	-150	μA
I <sub>BHL</sub>	Bus Hold Low Sustaining Current	$V_{IN} \geq V_{IL(max)}$	40	–	–	μA
I <sub>BHH</sub>	Bus Hold High Sustaining Current	$V_{IN} \leq V_{IH(min)}$	-40	–	–	μA
I <sub>BHLO</sub>	Bus Hold Low Overdrive Current	$0V \leq V_{IN} \leq V_{CCIO}$	–	–	550	μA
I <sub>BHLH</sub>	Bus Hold High Overdrive Current	$0V \leq V_{IN} \leq V_{CCIO}$	–	–	-550	μA
I <sub>BHT</sub>	Bus Hold Trip Points		V <sub>IL</sub>	–	V <sub>IH</sub>	V
I <sub>VCCIO</sub>	Current Needed for V <sub>CCIO</sub> Pin	All I/Os Pulled-up, (Total I/Os * I <sub>PUmax</sub> )	–	–	45	mA

DC Char\_5000V

 1. Typical values are at V<sub>CC</sub> = 3.3V and T<sub>A</sub> = 25°C.

 2. Pullup is capable of pulling to a minimum voltage of V<sub>OH</sub> under no-load conditions.

**External Switching Characteristics**

**Over Recommended Operating Conditions**

PARAM.	TEST <sup>3</sup> COND.	#	DESCRIPTION <sup>4,5</sup>	-110		-100		-70		UNITS
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t <sub>pd1</sub>	A	1	Data Prop. Delay, 5PT Bypass	—	8.5	—	10	—	15	ns
t <sub>pd2</sub>	A	2	Data Propagation Delay	—	10	—	13	—	19	ns
f <sub>max</sub>	A	3	Clock Frequency with Internal Feedback <sup>1</sup>	110	—	100	—	70	—	MHz
f <sub>max</sub> (Ext.)	—	4	Clock Freq. with Ext. Feedback, 1/(tsu2 + tco1)	80	—	64.5	—	43.5	—	MHz
f <sub>max</sub> (Tog.)	—	5	Clock Frequency, Max Toggle <sup>2</sup>	143	—	125	—	84	—	MHz
t <sub>su1</sub>	—	6	GLB Reg. Setup Time before Clk, 5PT bypass	6.5	—	8	—	12	—	ns
t <sub>co1</sub>	A	7	GLB Reg. Clock to Output Delay	—	5	—	5.5	—	8	ns
t <sub>h1</sub>	—	8	GLB Reg. Hold Time after Clock, 5PT bypass	0	—	0	—	0	—	ns
t <sub>su2</sub>	—	9	GLB Reg. Setup Time before Clock	7.5	—	10	—	15	—	ns
t <sub>h2</sub>	—	10	GLB Reg. Hold Time after Clock	0	—	0	—	0	—	ns
t <sub>su3</sub>	—	11	GLB Reg. Setup Time before Clk, Input Reg. Path	6	—	8	—	12	—	ns
t <sub>h3</sub>	—	12	GLB Reg. Hold Time after Clock, Input Reg. Path	0	—	0	—	0	—	ns
t <sub>r1</sub>	A	13	Ext. Reset Pin to Output Delay	—	17	—	20	—	30	ns
t <sub>rw1</sub>	—	14	Ext. Reset Pulse Duration	7.5	—	9	—	14	—	ns
t <sub>ptoe/dis</sub>	B/C	15	Local Product Term Output Enable/Disable	—	10	—	12	—	18	ns
t <sub>gptoe/dis</sub>	B/C	16	Global Product Term Output Enable/Disable	—	20	—	24	—	30	ns
t <sub>goe/dis</sub>	B/C	17	Global OE Input to Output Enable/Disable	—	6.5	—	8	—	12	ns
t <sub>wh</sub>	—	18	Ext. Sync. Clock Pulse Duration, High	3.5	—	4	—	6	—	ns
t <sub>wl</sub>	—	19	Ext. Sync. Clock Pulse Duration, Low	3.5	—	4	—	6	—	ns

1. Standard 32-bit counter using GRP feedback.
2. f<sub>max</sub> (Toggle) may be less than 1/(t<sub>wh</sub> + t<sub>wl</sub>). This is to allow for a clock duty cycle of other than 50%.
3. Reference Switching Test Conditions section.
4. Unless noted otherwise, all timing numbers are taken with worst case PTSA fanout.
5. Timing parameters measured using normal active output driver.

Timing Ext.5512.eps

## Internal Timing Parameters<sup>1</sup>

### Over Recommended Operating Conditions

PARAM	#	DESCRIPTION	-110		-100		-70		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
<b>I/O Buffer</b>									
t <sub>idcom</sub>	20	Input Pad and Buffer, Combinatorial Input	–	0.7	–	0.9	–	1.4	ns
t <sub>idreg</sub>	21	Input Pad and Buffer, Registered Input	–	7.1	–	8.8	–	12.4	ns
t <sub>odcom</sub>	22	Output Pad and Buffer, Combinatorial Output	–	1.3	–	2	–	2.6	ns
t <sub>odreg</sub>	23	Output Pad and Buffer, Registered Output	–	1.6	–	2.8	–	4.9	ns
t <sub>odz</sub>	24	Output Buffer Enable/Disable	–	1.3	–	1.7	–	2.6	ns
t <sub>slf</sub>	25	Slew Rate Adder, Fast Slew	–	0	–	0	–	0	ns
t <sub>sls</sub>	26	Slew Rate Adder, Slow Slew	–	8.5	–	10	–	15	ns
t <sub>slfd</sub>	27	Programmable Delay Adder, Fast Slew	–	0.5	–	0.7	–	1	ns
t <sub>slsd</sub>	28	Programmable Delay Adder, Slow Slew	–	9	–	10.7	–	16	ns
<b>GLB/Macrocell Delay Register</b>									
t <sub>mbp</sub>	29	Macrocell Register/Latch Bypass	–	0	–	0	–	0	ns
t <sub>mlat</sub>	30	Macrocell Latch Delay	–	1	–	1.4	–	2	ns
t <sub>mco</sub>	31	Macrocell Register/Latch Clock to Output	–	1	–	1	–	1	ns
t <sub>msu</sub>	32	Macrocell Register/Latch Setup Time	0.5	–	0.9	–	1.7	–	ns
t <sub>mh</sub>	33	Macrocell Register/Latch Hold Time	4.5	–	5.3	–	8	–	ns
t <sub>msuce</sub>	34	Macrocell Register/Latch CLKEN Setup Time	1	–	1.4	–	2	–	ns
t <sub>mhce</sub>	35	Macrocell Register/Latch CLKEN Hold Time	1	–	1.4	–	2	–	ns
t <sub>mrst</sub>	36	Macrocell Register/Latch Set/Reset Time	–	1	–	1.4	–	2	ns
t <sub>ftog</sub>	37	Toggle Flip-Flop Feedback	–	1	–	1.3	–	2	ns
<b>AND Array</b>									
t <sub>andhs</sub>	38	AND Array, High Speed Mode	–	3.6	–	4	–	6	ns
t <sub>andlp</sub>	39	AND Array, Low Power Mode	–	5.1	–	6.6	–	10	ns
<b>PTSA</b>									
t <sub>5ptcom</sub>	40	5 Product Term Bypass, Combinatorial	–	1.2	–	1.4	–	2	ns
t <sub>5ptreg</sub>	41	5 Product Term Bypass, Registered	–	2.4	–	1.6	–	2	ns
t <sub>5ptxcom</sub>	42	5 Product Term XOR, Combinatorial	–	2.1	–	2.8	–	4	ns
t <sub>5ptxreg</sub>	43	5 Product Term XOR, Registered	–	2.8	–	2.3	–	3	ns
t <sub>ptsacom</sub>	44	Product Term Sharing Array, Combinatorial	–	2.7	–	4.1	–	6	ns
t <sub>ptsareg</sub>	45	Product Term Sharing Array, Registered	–	3.4	–	3.6	–	5	ns
<b>PTSA Controls</b>									
t <sub>pk</sub>	46	Product Term Clock Delay	–	0.5	–	0.7	–	1	ns
t <sub>pkcn</sub>	47	Product Term CLKEN Delay	–	1	–	1.4	–	2	ns
t <sub>scken</sub>	48	Shared Product Term CLKEN Delay	–	1	–	1.4	–	2	ns
t <sub>sck</sub>	49	Shared Product Term Clock Delay	–	0.5	–	0.7	–	1	ns
t <sub>ptsacken</sub>	50	Product Term Sharing Array CLKEN Delay	–	2.2	–	3.4	–	5	ns
t <sub>srst</sub>	51	Shared Product Term Set/Reset Delay	–	2.5	–	3.4	–	5	ns
t <sub>prst</sub>	52	Product Term Set/Reset Delay	–	1.5	–	2	–	3	ns
t <sub>poe</sub>	53	Product Term Output Enable/Disable	–	2.7	–	3.4	–	5	ns
t <sub>gpoe</sub>	54	Global PT Output Enable/Disable	–	12.7	–	15.4	–	17	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

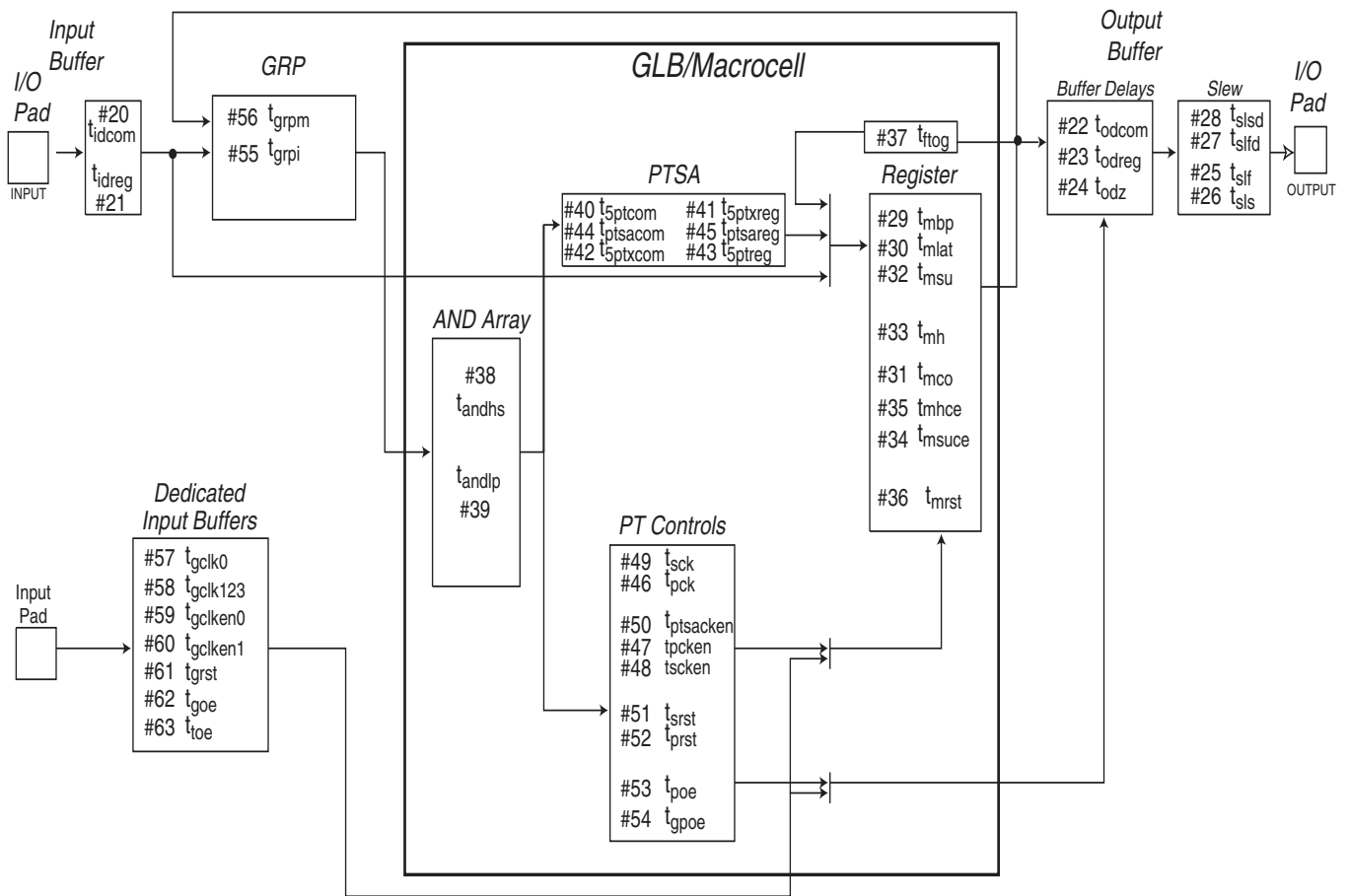
**Internal Timing Parameters<sup>1</sup>**

Over Recommended Operating Conditions

PARAM	#	DESCRIPTION	-110		-100		-70		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
<b>GRP</b>									
t <sub>grpi</sub>	55	GRP Delay from I/O Pad	–	1.7	–	2	–	3	ns
t <sub>grpm</sub>	56	GRP Delay from Macrocell	–	0.5	–	0.5	–	0.5	ns
<b>Global Control Delays</b>									
t <sub>gclk0</sub>	57	Global Clock 0 Delay	–	1.6	–	1.7	–	2.1	ns
t <sub>gclk123</sub>	58	Global Clock 1, 2 or 3 Delay	–	2.6	–	3.2	–	4.1	ns
t <sub>gclken0</sub>	59	Global CLKEN 0 Delay	–	2.1	–	2.4	–	3.1	ns
t <sub>clken1</sub>	60	Global CLKEN 1 Delay	–	3.1	–	3.9	–	5.1	ns
t <sub>grst</sub>	61	Global Set/Reset Delay	–	13.6	–	15.8	–	23.1	ns
t <sub>goe</sub>	62	Global OE Delay	–	5.2	–	6.3	–	9.4	ns
t <sub>toe</sub>	63	Test OE Delay	–	4.7	–	6.2	–	9.4	ns

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

**ispLSI 5512V Timing Model**

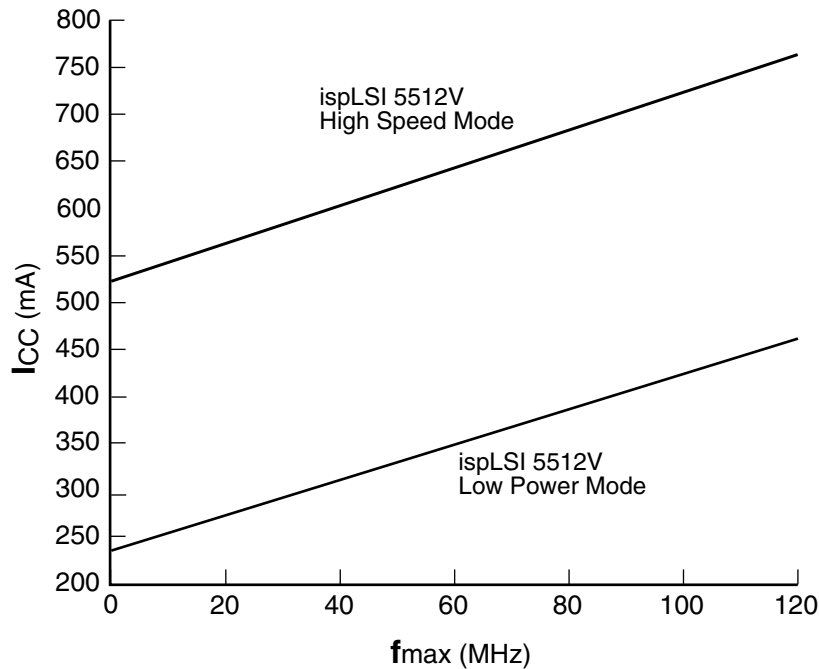


**Power Consumption**

Power Consumption in the ispLSI 5512V device depends on two primary factors: the speed at which the device is operating and the number of product terms used. The product terms have a fuse-selectable speed/power tradeoff setting. Each group of four product terms has a single speed/power tradeoff control fuse that acts on the

complete group of four. The fast "high-speed" setting operates product terms at their normal full power consumption. For portions of the logic that can tolerate longer propagation delays, selecting the slower "low-power" setting will significantly reduce the power dissipation for these product terms. Figure 10 shows the relationship between power and operating speed.

**Figure 10. Typical Device Power Consumption vs fmax**



Notes: Configuration of 32 16-bit Counters  
Typical Current at 3.3V, 25° C

ICC can be estimated for the ispLSI 5512V using the following equation:

**High Speed Mode:**  $ICC = 70 + (\# \text{ of PTs} * 0.4592) + (\# \text{ of nets} * \text{Max. freq} * 0.00391)$

**Low Power Mode:**  $ICC = 70 + (\# \text{ of PTs} * 0.160) + (\# \text{ of nets} * \text{Max. freq} * 0.00391)$

# of PTs = Number of Product Terms used in design

# of nets = Number of Signals used in device

Max. freq = Highest Clock Frequency to the device

The ICC estimate is based on typical conditions (VCC = 3.3V, room temperature) and an assumption of 2 GLB loads on average exists. These values are for estimates only. Since the value of ICC is sensitive to operating conditions and the program in the device, the actual ICC should be verified.

0127/5512



## Signal Descriptions

Signal Name	Description
TMS	Input - This pin is the Test Mode Select input, which is used to control the JTAG state machine.
TCK	Input - This pin is the Test Clock input pin used to clock through the JTAG state machine.
TDI	Input - This pin is the JTAG Test Data In pin used to load Data.
TDO	Output - This pin is the JTAG Test Data Out pin used to shift data out.
TOE / I/O0	Input/Output - This pin functions as either the Test Output Enable pin or an I/O pin based upon customer's design. TOE tristates all I/O pins when a logic low is driven.
GOE0, GOE1	Input - These two pins are the Global Output Enable input pins.
GSET/GRST	Dedicated Set/Reset Input - This pin is available to all registers in the device and can independently be configured as preset, reset or no effect on each register. The global polarity (active high or low input) for this pin is also selectable.
I/O	Input/Output – These are the general purpose I/O used by the logic array.
GND	Ground
NC <sup>1</sup>	No connect.
VCC	Vcc
CLK0, CLK1	Dedicated clock inputs for all registers. Both clocks are muxed before being used as the clock input to all registers in the device.
CLK2 / I/O, CLK3 / I/O	Input/Output - These pins function as either dedicated clock inputs for all registers or an I/O pin based upon customer's design. Both clocks are muxed before being used as the clock input to all registers in the device.
VCCIO	Input - This pin is used if an optional 2.5V output is to be used. Every I/O can independently select either 3.3V or the optional voltage as its output level. If the optional output voltage is not required, this pin must be connected to the Vcc supply. Programmable pull-up resistors and bus-hold latches only draw current from this supply.

1. NC pins are not to be connected to any active signals, VCC or GND.

**Signal Locations (388-Ball Grid Array)**

Signal	Ball
GOE0, GOE1	AF14, AD13
TOE / I/O0	T1
GSET/GRST	L25
TCK	T2
TDI	R3
TDO	N24
TMS	R1
CLK0, CLK1	A13, C14
CLK2 / I/O179	A23
CLK3 / I/O197	B17
VCCIO	M26
GND	A1, A2, A26, B2, B25, B26, C3, C24, D4, D9, D14, D19, D23, H4, J23, L11, L12, L13, L14, L15, L16, M11, M12, M13, M14, M15, M16, N4, N11, N12, N13, N14, N15, N16, P11, P12, P13, P14, P15, P16, P23, R11, R12, R13, R14, R15, R16, T11, T12, T13, T14, T15, T16, V4, W23, AC4, AC8, AC13, AC18, AC23, AD3, AD24, AE1, AE2, AE25, AF1, AF25, AF26
VCC	D6, D11, D16, D21, F4, F23, L4, L23, T4, T23, AA4, AA23, AC6, AC11, AC16, AC21
NC <sup>1</sup>	C9, D2, E24, L1, AC25, AF19

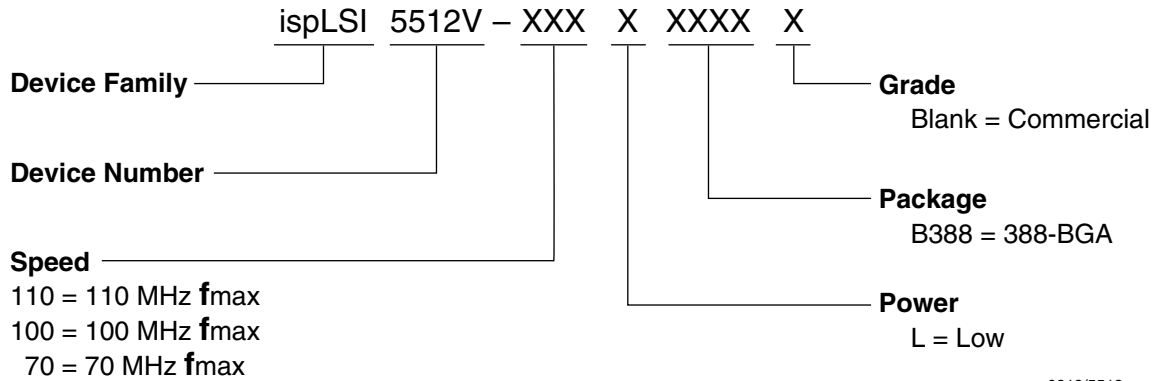
1. NCs are not to be connected to any active signals, VCC or GND.

**I/O Locations (388-Ball Grid Array)**

I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball	I/O #	Ball
0*	T1	48	AC9	96	AE23	144	M24	192	D18	240	B4
1	R4	49	AF8	97	AC22	145	L26	193	A19	241	D5
2	U2	50	AD8	98	AF23	146	M23	194	C19	242	A4
3	T3	51	AE9	99	AD22	147	K25	195	B18	243	C5
4	U1	52	AF9	100	AE24	148	L24	196	A18	244	B3
5	U4	53	AE10	101	AD23	149	K26	197*	B17	245	C4
6	V2	54	AD9	102	AF24	150	K23	198	C18	246	A3
7	U3	55	AF10	103	AE26	151	J25	199	A17	247	B1
8	V1	56	AC10	104	AD25	152	K24	200	D17	248	C2
9	W2	57	AE11	105	AD26	153	J26	201	B16	249	C1
10	W1	58	AD10	106	AC24	154	H25	202	C17	250	D3
11	V3	59	AF11	107	AC26	155	H26	203	A16	251	D1
12	Y2	60	AE12	108	AB25	156	J24	204	B15	252	E2
13	W4	61	AF12	109	AB23	157	G25	205	A15	253	E4
14	Y1	62	AD11	110	AB24	158	H23	206	C16	254	E3
15	W3	63	AE13	111	AB26	159	G26	207	B14	255	E1
16	AA2	64	AC12	112	AA25	160	H24	208	D15	256	F2
17	Y4	65	AF13	113	Y23	161	F25	209	A14	257	G4
18	AA1	66	AD12	114	AA24	162	G23	210	C15	258	F3
19	Y3	67	AE14	115	AA26	163	F26	211	B13	259	F1
20	AB2	68	AC14	116	Y25	164	G24	212	D13	260	G2
21	AB1	69	AE15	117	Y26	165	E25	213	B12	261	G1
22	AA3	70	AD14	118	Y24	166	E26	214	C13	262	G3
23	AC2	71	AF15	119	W25	167	F24	215	A12	263	H2
24	AB4	72	AE16	120	V23	168	D25	216	B11	264	J4
25	AC1	73	AD15	121	W26	169	E23	217	C12	265	H1
26	AB3	74	AF16	122	W24	170	D26	218	A11	266	H3
27	AD2	75	AC15	123	V25	171	C25	219	D12	267	J2
28	AC3	76	AE17	124	V26	172	D24	220	B10	268	J1
29	AD1	77	AD16	125	U25	173	C26	221	C11	269	K2
30	AF2	78	AF17	126	V24	174	A25	222	A10	270	J3
31	AE3	79	AC17	127	U26	175	B24	223	D10	271	K1
32	AF3	80	AE18	128	U23	176	A24	224	B9	272	K4
33	AE4	81	AD17	129	T25	177	B23	225	C10	273	L2
34	AD4	82	AF18	130	U24	178	C23	226	A9	274	K3
35	AF4	83	AE19	131	T26	179*	A23	227	B8	275	M2
36	AE5	84	AD18	132	R25	180	B22	228	A8	276	M1
37	AC5	85	AE20	133	R26	181	D22	229	B7	277	L3
38	AD5	86	AC19	134	T24	182	C22	230	D8	278	N2
39	AF5	87	AF20	135	P25	183	A22	231	A7	279	M4
40	AE6	88	AD19	136	R23	184	B21	232	C8	280	N1
41	AC7	89	AE21	137	P26	185	D20	233	B6	281	M3
42	AD6	90	AC20	138	R24	186	C21	234	D7	282	P2
43	AF6	91	AF21	139	N25	187	A21	235	A6	283	P4
44	AE7	92	AD20	140	N23	188	B20	236	C7	284	P1
45	AF7	93	AE22	141	N26	189	A20	237	B5	285	N3
46	AD7	94	AF22	142	P24	190	C20	238	A5	286	R2
47	AE8	95	AD21	143	M25	191	B19	239	C6	287	P3

\* I/O 179 is multiplexed with CLK2, I/O 197 is multiplexed with CLK3 and I/O 0 is multiplexed with TOE.

**Part Number Description**



**Ordering Information**

**COMMERCIAL**

Family	f <sub>max</sub>	t <sub>pd</sub>	Ordering Number	Package
ispLSI	110	8.5	ispLSI 5512V-110LB388	388-Ball BGA
ispLSI	100	10	ispLSI 5512V-100LB388	388-Ball BGA
ispLSI	70	15	ispLSI 5512V-70LB388	388-Ball BGA