

Introduction

When using the ispMACH 4000 families from Lattice Semiconductor, consideration must be made for the I/O standard associated with the In-System Programmable (ISP™) JTAG pins. A 1.8V ispMACH 4000C device has 1.8V LVCMOS JTAG pins; the ispMACH 4000B has 2.5V JTAG pins. When a JTAG chain of ispMACH 4000C or ispMACH 4000B devices is designed onto a board, the JTAG signals should be driven at 1.8 or 2.5 volts respectively. As a result, several decisions must be made including what voltage a JTAG chain should be driven to and how to mix the ispMACH 4000B/C devices with other JTAG devices that operate at 3.3V signaling levels. This technical note addresses design issues with a multi-voltage JTAG chain that contains one or more ispMACH 4000B/C devices. For other programming design guidelines, please see *In-System Programming Design Guidelines for ispJTAG™ Devices* available at www.latticesemi.com.

JTAG Chain Design Recommendations

Many possible system architectures can be used to support multiple JTAG voltages on the same board. Lattice recommends two possible design approaches for supporting multiple JTAG voltages.

Implement Separate JTAG Chains For Each Voltage

For example, all 3.3V devices are placed in one JTAG chain, all 1.8V devices in a separate JTAG chain. This method reduces the confusion when other vendors have to interface with a JTAG chain. Each chain JTAG LVCMOS standard is supported by all the devices and helps reduce the chance that other devices cannot interface to the LVCMOS standard, (i.e. 1.8V and 3.3V).

Figure 1. 3.3V Programming Chain

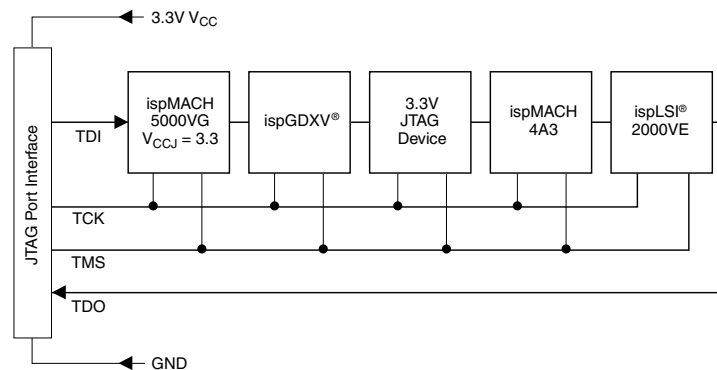


Figure 2. 2.5V Programming Chain

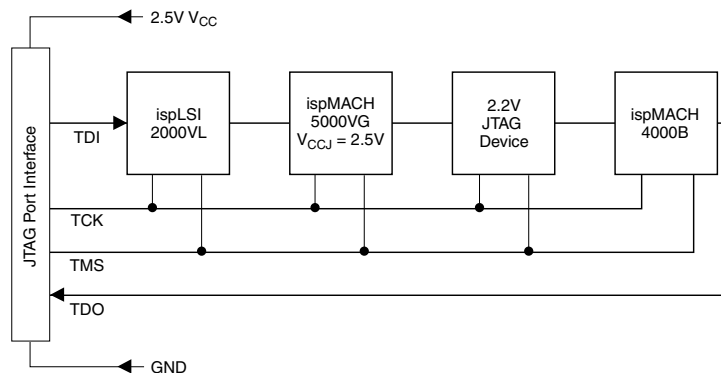
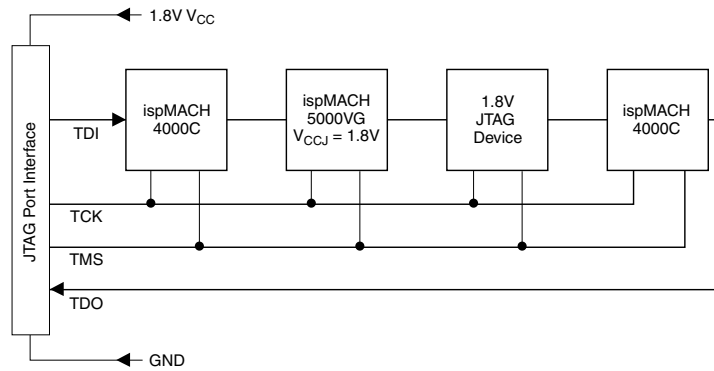


Figure 3. 1.8V Programming Chain



Create A Multi-Voltage JTAG Chain

In many cases, all JTAG devices exist in a single chain. When devices of a differing JTAG voltage are mixed in the same chain, Lattice recommends the following guidelines for layout of the multi-voltage JTAG chain.

1. The highest voltage devices should be placed first in the chain. The next highest voltage placed next, down to the lowest voltage devices being last in the chain. Placing the highest voltage to lowest voltage JTAG signals in order, the TDO output of the proceeding device will be correctly interpreted as a logic high by the input of the next device when it is driven high.
2. Verify that each device is able to tolerate the maximum voltage from the proceeding device. All of the ispMACH 4000 devices can tolerate a maximum of 3.6V on the JTAG inputs.
3. Verify that TDO can be interpreted by the device driven by the last TDO in the chain. The Lattice ispDOWNLOAD[®] cable version 3 and certain ATE systems are able to correctly interpret the TDO from all members of the ispMACH 4000 Family (Figure 4). The V_{CC} connected to the Lattice ispDOWNLOAD cable should not be higher than 3.6V to interpret the lowest JTAG TDO voltage of 1.8V.
4. For systems that cannot interpret the TDO of the ispMACH 4000 Family, a voltage translator can be used to translate the TDO to 3.3V. One possible device to use in this situation is the 74LVC07A, available from Philips or Texas Instruments (Figure 5).

Figure 4. Multi-voltage JTAG Chain Using Lattice Version 3 Cable or Other Device That Can Interpret ispMACH 4000TDO

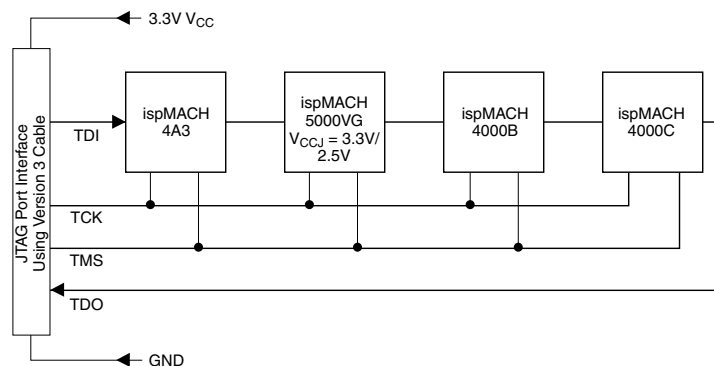
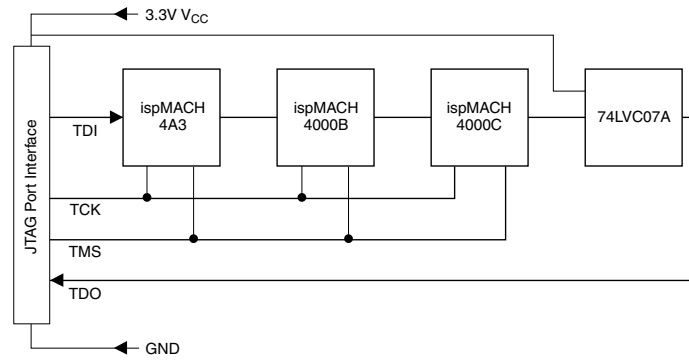


Figure 5. Multi-voltage JTAG Chain with a Translator Chip



Technical Support Assistance

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