CrossLink-NX sysI/O Usage Guide

Technical Note

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Acronyms in This Document

A list of acronyms used in this document.

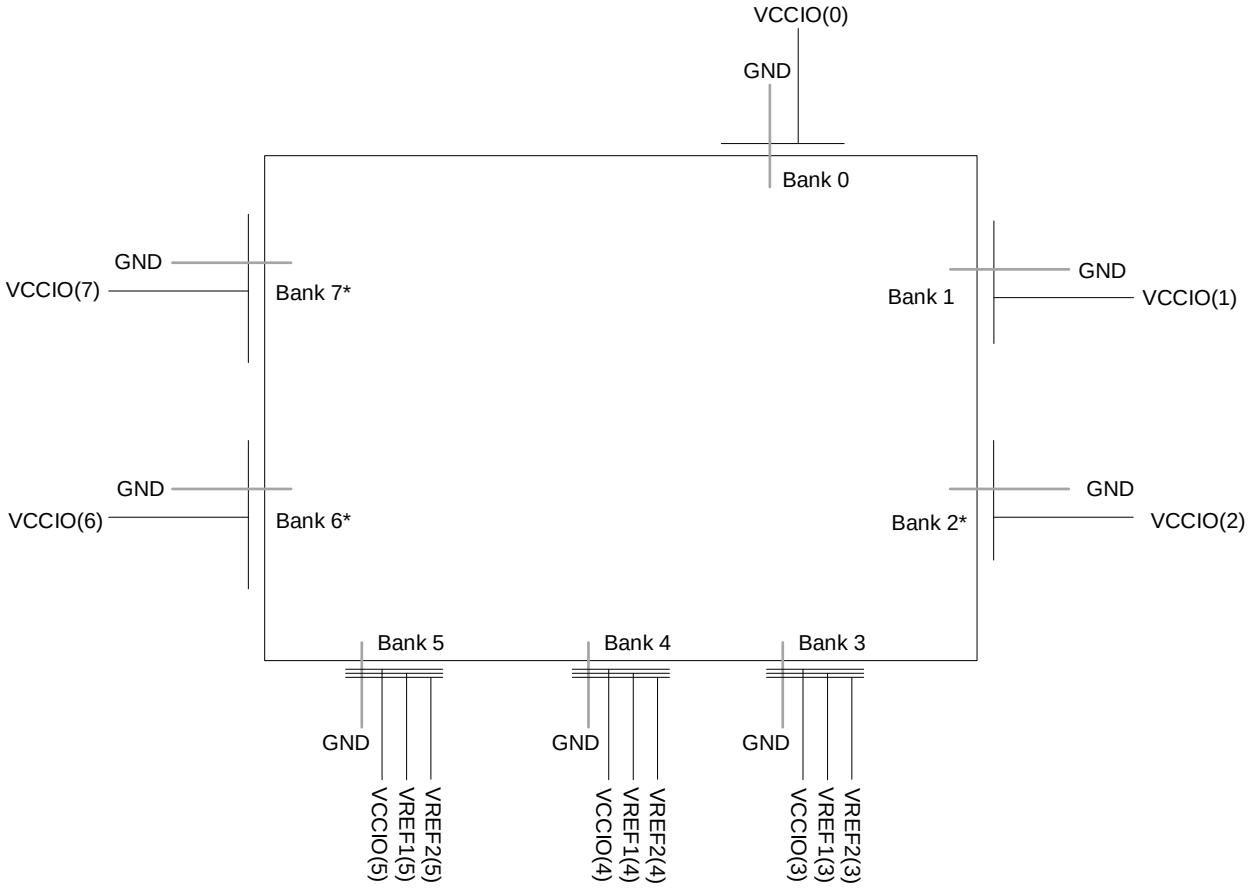
Acronym	Definition
DDR	Double Data Rate
HDL	Hardware Description Language
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
LVTTL	Low Voltage Transistor-Transistor Logic
PIO	Programmable Input/Output
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit

1. Introduction

The Lattice Semiconductor CrossLink-NX™ device family sysI/O™ buffers are designed to support a wide range of interfaces. Two types of I/O are offered, wide range I/O on the top, left and right banks and high performance I/O on the bottom banks only. It gives you the ability to easily interface with other devices using advanced system I/O standards. This technical note provides information on the supported I/O standards and the banking scheme of the CrossLink-NX family. The software attributes/usage are also covered to provide a better understanding of the I/O functionality and placement rules.

2. sysI/O Banking Scheme

All CrossLink-NX devices have 8 banks in total. One bank on top, two on left and right, and three on bottom. The higher density CrossLink-NX device, the more pins there are in each bank. Bank 0, Bank 1, Bank 2, Bank 6, and Bank 7 support up to V_{CCIO} 3.3 V while Bank 3, Bank 4, and Bank 5 support up to V_{CCIO} 1.8 V. In addition, Bank 3, Bank 4, and Bank 5 support two VREF inputs for flexibility to receive two different referenced input levels on the same bank. Figure 2.1 shows the location of each bank.



***Note:** Banks are not available for 17K.

Figure 2.1. sysI/O Banking

2.1. V_{CC} (1.0 V)

This is the core supply. This V_{CC} supply is used to power the control logic. The control signals and data signals from the I/O logic are then translated to higher supply of the I/O buffers.

2.2. V_{CCIO} [0, 1, 2, 6, 7] (1.2 V/1.5 V/1.8 V/2.5 V/3.3 V)

Bank 0, Bank 1, Bank 2, Bank 6, and Bank 7 have a V_{CCIO} supply that operates from 3.3 V down to 1.0 V.

2.3. V_{CCIO} [3, 4, 5] (1.0 V/1.2 V/1.35 V/1.5 V/1.8 V)

Bank 3, Bank 4, and Bank 5 operate with V_{CCIO} of 1.8 V down to 1.0 V. Standards such as LVDS, SSTL HSTL, and SLVS are only supported on these three banks.

2.4. V_{CCAUX} (1.8 V)

In addition to the bank V_{CCIO} supplies and a Vcc core logic supply, CrossLink-NX devices have a VCCAUX auxiliary supply that powers the differential and referenced input buffers D-PHY External Power Supplies (1.2 V).

3. V_{CCIO} Requirement for I/O Standards

Each I/O bank of a CrossLink-NX device has a separate V_{CCIO} supply pin that can be connected to 1.0 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V for bottom banks and 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V for the rest of the banks. These voltages are used to power the output I/O standard and source the drive strength for the output. On the input side, each pad is connected to a set of ratioed input buffers that provide support for the following:

- Fixed threshold 1.0 V/1.2 V input standards
- Ratioed V_{CCIO} input standards
- Ratioed V_{CCAUX} based 1.8/1.5V LVCMOS inputs.

These three buffers are connected to V_{CC}, V_{CCIO} and V_{CCAUX} respectively.

Table 3.1. Input Mixed Mode for Wide Range Input Buffers

	Input Signaling (V)					
V_{CCIO} (V)	LVCMOS10	LVCMOS12	LVCMOS15	LVCMOS18	LVCMOS25	LVCMOS33
	V_{CC} Powered Buffer		V_{CCAUX} Powered Buffer		V_{CCIO} Powered Buffer	
1.2	✓[2]	✓[2]	✓[1,3]	—	—	—
1.5	✓[2]	✓[2]	✓[1,3]	✓	—	—
1.8	✓[2]	✓[2]	✓[1,3]	✓	—	—
2.5	✓[2]	✓[2]	✓[1,3]	✓	✓	—
3.3	✓[2]	✓[2]	✓[1,3]	✓	✓[3]	✓

Notes:

1. Increased ICC due to underdrive.
2. No HYST.
3. Reduced HYST.

Table 3.2. Input Mixed Mode for High Performance Input Buffers

	Input Signaling (V)			
V_{CCIO} (V)	LVCMOS1.0	LVCMOS1.2	LVCMOS1.5	LVCMOS1.8
	V_{CC} Powered Buffer		V_{CCIO} Powered Buffer	
1.0	✓			
1.2	✓	✓		
1.5	✓	✓	✓	
1.8	✓	✓	✓[1,2]	✓

Notes:

1. Increased ICC due to underdrive.
2. Reduced Hysteresis.

4. sysI/O Buffer Configurations

This section describes the various sysI/O features available on the CrossLink-NX device.

4.1. Programmable Drive Strength

All single-ended drivers have programmable drive strength. Table 4.1 and Table 4.2 show the programmable drive strength of all the I/O standards available in CrossLink-NX. The maximum current allowed per bank as well as the package thermal limit current should be taken into consideration when selecting the drive strength.

Table 4.1. Programmable Drive Strength Values at Various VCCIO Voltages for Wide Range Output Driver

I/O TYPE	Drive Strength (mA)
LVCMOS33	2, 4, 8, 12, 16
LVCMOS25	2, 4, 8, 10
LVCMOS18	2, 4, 8
LVCMOS15	2, 4
LVCMOS12	2, 4

Table 4.2. Programmable Drive Strength Values at Various VCCIO Voltages for High Performance Output Driver

I/O TYPE	Drive Strength (mA)
LVCMOS18	2, 4, 8, 12
LVCMOS15	2, 4, 8
LVCMOS12	2, 4, 8
LVCMOS10	2, 4

4.2. Programmable Slew Rate

The single-ended output buffer for each I/O pin has programmable output slew rate control that can be configured for either low noise (SLEWRATE=SLOW) or high speed (SLEWRATE=FAST) or in between, (SLEWRATE=MED).

4.3. Tristate Control

On the output side, each single-ended driver has a separate tristate control. The differential driver has a tristate control as well.

4.4. Open Drain Control

In addition to the tristate control, the single-ended drivers also support open drain operation on each I/O independently. Unlike non-open drain output that consists of a source and sink section, an open drain output is composed of only the sink section of the output driver. You can implement an open drain output by turning on the OPENDRAIN attribute in the software

4.5. Differential Input Termination

The CrossLink-NX devices support a programmable 100 Ω input termination between all pairs on the bottom banks. The input termination of 100 Ω can be programmed between on and off. Figure 4.1 shows the discrete off-chip and on-chip solutions for dedicated, differential input termination.

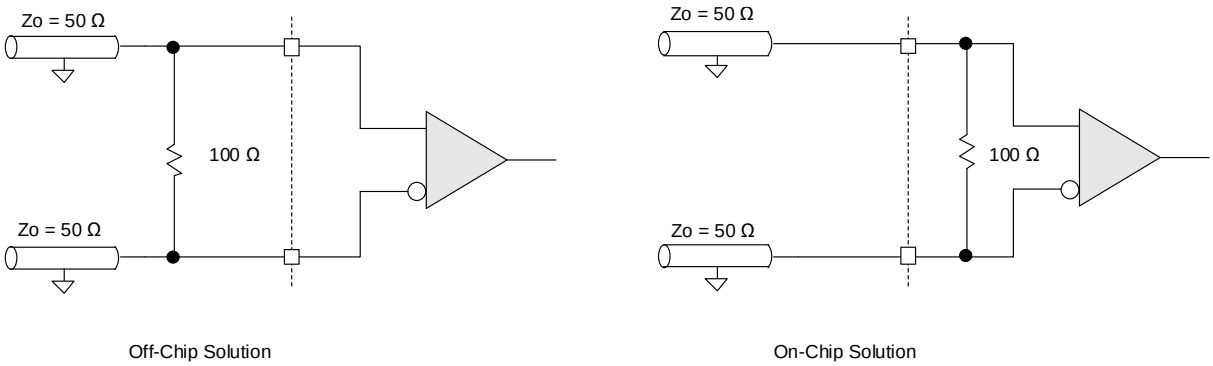


Figure 4.1. Off-Chip and On-Chip Solutions

4.6. Programmable Clamp

The buffers on the bottom sysI/O have optional clamp diodes that can be programmable to ON or OFF.

5. Software sysI/O Attributes

The sysI/O attributes can be specified in the Hardware Description Language (HDL), using Device Constraint Editor, or in Pre/Post Timing Constraint Editor (.ldc/.pdc).

5.1. IO_TYPE

This attribute is used to set the sysI/O standard for an I/O. The V_{CCIO} required to set these I/O standards are embedded in the attribute names. Table 5.1 lists the available I/O types.

Table 5.1. IO_TYPE Attribute Values

sysI/O Signaling Standard	IO_TYPE
Default	LVCMOS18
LVDS 1.8V	LVDS
LVDS 1.8V Emulation	LVDSE
Sub-LVDS	SUBLVDS
Sub-LVDS Emulation	SUBLVDSE
Sub-LVDS Emulation High Speed	SUBLVDSEH
SLVS	SLVS
MIPI_DPHY	MIPI_DPHY
SSTL 1.5V Class I	SSTL15_I
SSTL 1.5V Class II	SSTL15_II
SSTL 1.5V Differential Class I	SSTL15D_I
SSTL 1.5V Differential Class II	SSTL15D_II
SSTL 1.35V Class I	SSTL135_I
SSTL 1.35V Class II	SSTL135_II
SSTL 1.35V Differential Class I	SSTL135D_I
SSTL 1.35V Differential Class II	SSTL135D_II
HSTL 1.5V Class I	HSTL15_I
HSTL 1.5V Differential Class I	HSTL15D_I
HSUL 1.2V	HSUL12
HSUL 1.2V Differential	HSUL12D
LVTTL 3.3V	LVTTL33
LVTTL 3.3V differential	LVTTL33D
LVCMOS 3.3V	LVCMOS33
LVCMOS 3.3V Differential	LVCMOS33D
LVCMOS 2.5V	LVCMOS25
LVCMOS 2.5V Differential	LVCMOS25D
LVCMOS 1.8V Differential	LVCMOS18
LVCMOS 1.8V High Speed	LVCMOS18H
LVCMOS 1.5V	LVCMOS15
LVCMOS 1.5V High Speed	LVCMOS15H
LVCMOS 1.2V	LVCMOS12
LVCMOS 1.2V High Speed	LVCMOS12H
LVCMOS 1.0V	LVCMOS10
LVCMOS 1.0V High Speed	LVCMOS10H
LVCMOS 1.0V Referenced	LVCMOS10R

5.2. PULLMODE

The PULLMODE attribute can be enabled for each I/O independently. This attribute is available for all the LVTLL and LVCMOS inputs and bidirectional I/O.

Values: UP, DOWN, NONE, I3C, FAILSAFE

Default: Down when available, None when not available.

5.3. CLAMP

The CLAMP option can be enabled for each I/O independently.

Values: ON, OFF

Default: ON for Bank 3, Bank 4, Bank 5 and OFF for Bank 0, Bank 1, Bank 2, Bank 6, Bank 7

5.4. HYSTERESIS

The hysteresis option can be used to change the amount of hysteresis for the LVTTL and LVCMOS input and bidirectional I/O standards. LVCMOS12/12H and LVCMOS10/10H do not support hysteresis.

Values: ON, NA

Default: ON for LVTTL, and LVCMOS15/18/33 for input and bidirectional standards. Everything else defaulted to *NA*

5.5. VREF

The VREF option is enabled for referenced LVCMOS10 as well as referenced input buffers such as HSTL, SSTL and HSUL.

Values: OFF, VREF1_LOAD, VREF2_LOAD

Default: *VREF1_LOAD* for standards mentioned above, others defaulted to OFF.

5.6. OPENDRAIN

The OPENDRAIN option is available for all LVTTL and LVCMOS.

An I/O can be assigned independently to be an open drain when this attribute is turned on.

Values: OFF, ON

Default: OFF

5.7. SLEWRATE

Each I/O pin has an individual slew rate control. This allows you to specify slew rate control on a pin by pin basis. Slew rate control is not a valid attribute for inputs.

Values: SLOW, MED, FAST, NA

Default: SLOW

Hardware default: SLOW

5.8. DIFFRESISTOR

This attribute is used to provide differential termination. It is available only for differential I/O types.

Values: OFF, 100

Default: OFF

5.9. TERMINATION

The I/O supports single ended input parallel termination to $V_{CCIO}/2$. All input parallel terminations use a Thevenin termination scheme.

Values: OFF, 40, 50, 60, 75, 150

Default: OFF

5.10. DRIVE

The drive strength attribute is available for the output and bidirectional I/O standards. The default drive value depends on the I/O standard used.

Table 5.2. DIFFRESISTOR Values

Output Standard	Drive	DiffDrive	V_{CCIO}
Single Ended Interfaces			
LVTTL33	8 mA, 2 mA, 4 mA, 12 mA, 16 mA, 50RS	—	3.3
LVCMOS33	8 mA, 2 mA, 4 mA, 12 mA, 16 mA, 50RS	—	3.3
LVCMOS25	8 mA, 2 mA, 4 mA, 12 mA, 50RS	—	2.5
LVCMOS18	8 mA, 2 mA, 4 mA, 50RS	—	1.8
LVCMOS18H	8 mA, 2 mA, 4 mA, 12 mA, 50RS	—	1.8
LVCMOS15	8 mA, 2 mA, 4 mA	—	1.5
LVCMOS15H	8 mA, 2 mA, 4 mA	—	1.5
LVCMOS12	8 mA, 2 mA, 4 mA	—	1.2
LVCMOS12H	8 mA, 2 mA, 4 mA	—	1.2
LVCMOS10H	8 mA, 2 mA, 4 mA	—	1
LVTTL33 (Open Drain)	8 mA, 2 mA, 4 mA, 12 mA	—	—
LVCMOS33 (Open Drain)	8 mA, 2 mA, 4 mA, 12 mA	—	—
LVCMOS25 (Open Drain)	8 mA, 2 mA, 4 mA, 10 mA	—	—
LVCMOS18 (Open Drain)	8 mA, 2 mA, 4 mA	—	—
LVCMOS18H (Open Drain)	8 mA, 2 mA, 4 mA, 12 mA	—	—
LVCMOS15 (Open Drain)	8 mA, 2 mA, 4 mA	—	—
LVCMOS15H (Open Drain)	8 mA, 2 mA, 4 mA	—	—
LVCMOS12 (Open Drain)	8 mA, 2 mA, 4 mA	—	—
LVCMOS12H (Open Drain)	8 mA, 2 mA, 4 mA	—	—
LVCMOS10H (Open Drain)	8 mA, 2 mA, 4 mA	—	—
HSUL12	8 mA, 6 mA, 4 mA	—	1.2
HSTL15_I	8 mA	—	1.5
SSTL15_I	8 mA	—	1.5
SSTL15_II	10 mA	—	1.5
Differential Interfaces			
LVDS	-	3.5 mA	1.8
SLVS	-	2.0 mA	—
SUBLVDSE	8 mA	—	1.8
SUBLVDSEH	8 mA	—	1.8
LVDSE	8 mA	—	2.5
HSUL12D	4 mA, 6 mA, 8 mA	—	1.2
HSTL15D_I	8 mA	—	1.5
SSTL15D_I	8 mA	—	1.5
SSTL15D_II	10 mA	—	1.5

Output Standard	Drive	DiffDrive	V_{CCIO}
SSTL135D_I	8 mA	—	1.35
SSTL135D_II	10 mA	—	1.35
LVTTL33D	8 mA, 2 mA, 4 mA, 12 mA, 50RS	—	3.3
LVCMOS33D	8 mA, 2 mA, 4 mA, 12 mA, 50RS	—	3.3
LVCMOS25D	8 mA, 2 mA, 4 mA, 12 mA, 50RS	—	2.5

Technical Support Assistance

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Revision History

Revision 1.0, November 2019

Section	Change Summary
All	Initial release

www.latticesemi.com