



# Sub-LVDS Signaling Using Lattice Devices

## Technical Note

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December 2019

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## Contents

Acronyms in This Document .....	4
1. Introduction .....	5
2. Differences between LVDS and Sub-LVDS Signals .....	5
Technical Support Assistance .....	12
Revision History .....	13

## Figures

Figure 2.1. Sub-LVDS Output Driving a Lattice Device Input .....	5
Figure 2.2. ECP5/ECP5-5G, LatticeECP3 and LatticeXP2 Typical Differential Input Simulation Waveform .....	7
Figure 2.3. Differential Input Waveform for Hardware Test .....	7
Figure 2.4. Typical Differential Output Waveform from Hardware Test .....	8
Figure 2.5. Lattice Device Generating a Sub-LVDS Signal Level – LatticeXP2, LatticeECP3, ECP5/ECP5-5G, and CrossLink-NX .....	9
Figure 2.6. Lattice Device Generating a Sub-LVDS Signal Level – MachXO2 and MachXO3L/LF .....	9
Figure 2.7. Lattice Device Generating a Low Noise Sub-LVDS Signal – LatticeXP2, LatticeECP3, ECP5/ECP5-5G, and CrossLink-NX .....	10
Figure 2.8. Lattice Device Generating a Low Noise Sub-LVDS Signal – MachXO2 and MachXO3L/LF .....	11

## Tables

Table 2.1. Sub-LVDS Output Signal Voltages and LVDS Input Specifications .....	6
Table 2.2. Sub-LVDS Output Voltages for Rs and Rp 1% Resistor Values .....	10

## Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
BGA	Ball Grid Array
LVC MOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
PCB	Printed Circuit Board

## 1. Introduction

Sub-LVDS is a reduced-voltage form of LVDS signaling, very similar to LVDS. Being similar to LVDS, Lattice FPGA devices can support the sub-LVDS signaling with other differential I/O standards already supported as part of the standard I/O types. This technical note summarizes the main differences between sub-LVDS and LVDS, in order to show how Lattice devices can support the sub-LVDS I/O standard. Knowing the differences, you can then refer back to the Lattice data sheets to both confirm compatibility and choose compatible I/O types to implement sub-LVDS solutions with Lattice devices.

## 2. Differences between LVDS and Sub-LVDS Signals

Devices such as the Lattice CrossLink-NX™, ECP5™/ECP5-5G™, LatticeECP3™, LatticeXP2™, MachXO2™, and MachXO3L/LF™ include the LVDS I/O types. Sub-LVDS is different from LVDS in that the differential and common mode signal levels are reduced yet still within the LVDS input range. As such, a sub-LVDS output can directly drive an LVDS input, as shown in Figure 2.1.

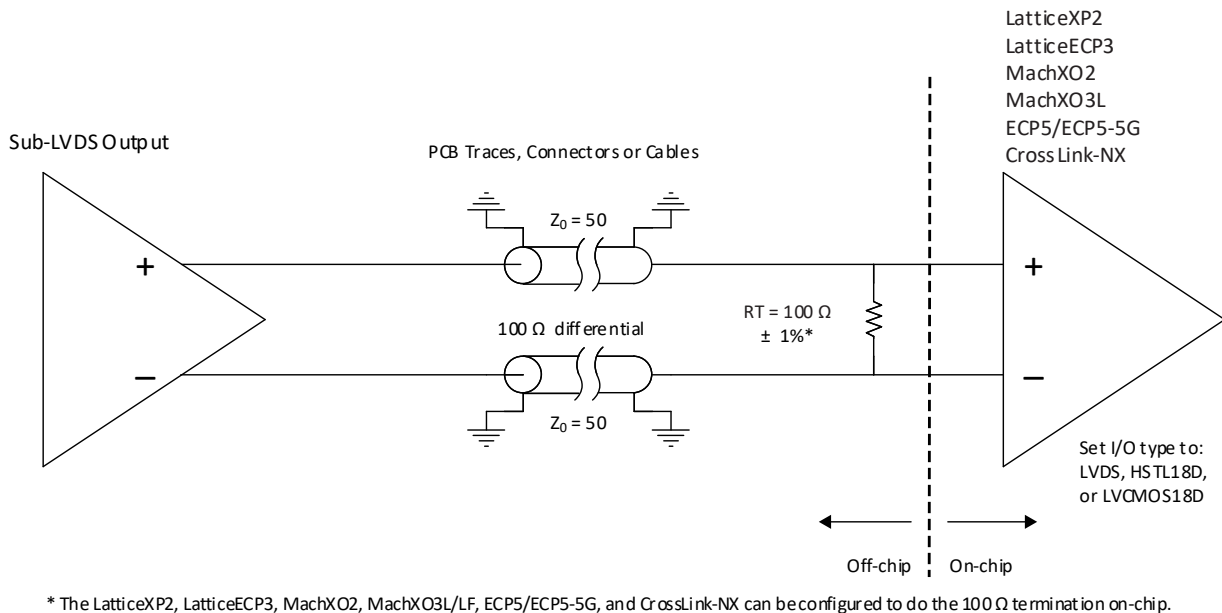


Figure 2.1. Sub-LVDS Output Driving a Lattice Device Input

Table 2.1 shows sub-LVDS output signal voltages, and the Lattice device LVDS input specifications. When comparing the values in the table, it is clear that the Lattice device’s LVDS inputs are compatible to receive sub-LVDS output signals.

**Table 2.1. Sub-LVDS Output Signal Voltages and LVDS Input Specifications**

Characteristic	Sub-LVDS Output	ECP5/ ECP5-5G LVDS Input	LatticeECP3 LVDS Input	LatticeXP2 LVDS Input	MachXO2 and MachXO3L/ LF LVDS Input	MachXO2 HSTL18D_I Input	MachXO3L/LF LVCMOS18D Input	CrossLink- NX	Unit
Common Mode Voltage Min (Vcm)	0.75	0.05	0.05	0.05	0.05	0.05	0.05	0.05	V
Common Mode Voltage Max (Vcm)	1.05	2.35	2.35	2.35	2.0	1.1	1.1	1.55	V
Differential Voltage Min (Vod)	100	100	100	100	100	100	100	100	mV
Differential Voltage Max (Vod)	200	2400	2400	2400	2050	1105	1105	1600	mV

In some instances, a sub-LVDS receiver is expected to detect signals below the sub-LVDS minimum differential output level of 100 mV. Based on simulation and characterization tests, the LatticeXP2, LatticeECP3, ECP5/ECP5-5G family devices LVDS inputs can detect differential signal levels down to 70 mV. Figure 2.2 shows a typical simulation waveform of an ECP5/ECP5-5G device, a LatticeECP3 and LatticeXP2 differential input buffer that is able to properly detect the input differential at 70 mV. Figure 2.3 and Figure 2.4 show a similar hardware test condition to the simulation that shows the input and output signals associated with the differential input voltage at 70 mV.

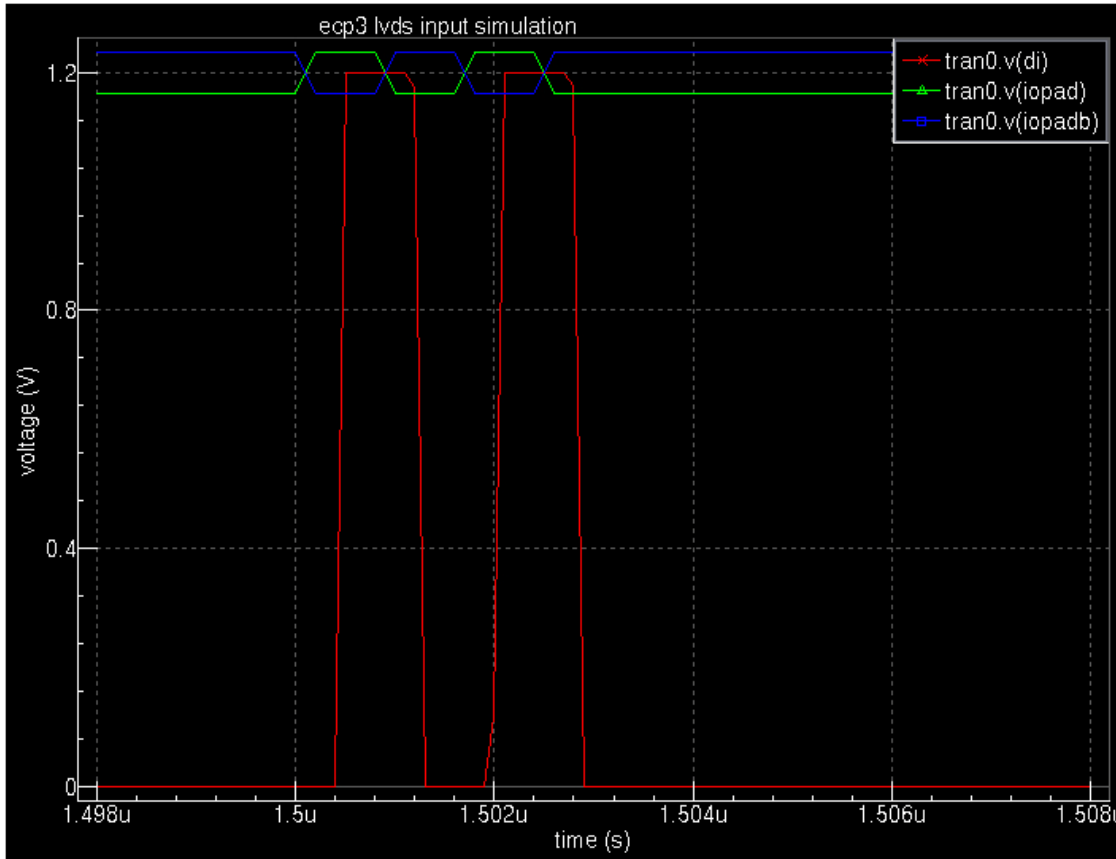


Figure 2.2. ECP5/ECP5-5G, LatticeECP3 and LatticeXP2 Typical Differential Input Simulation Waveform

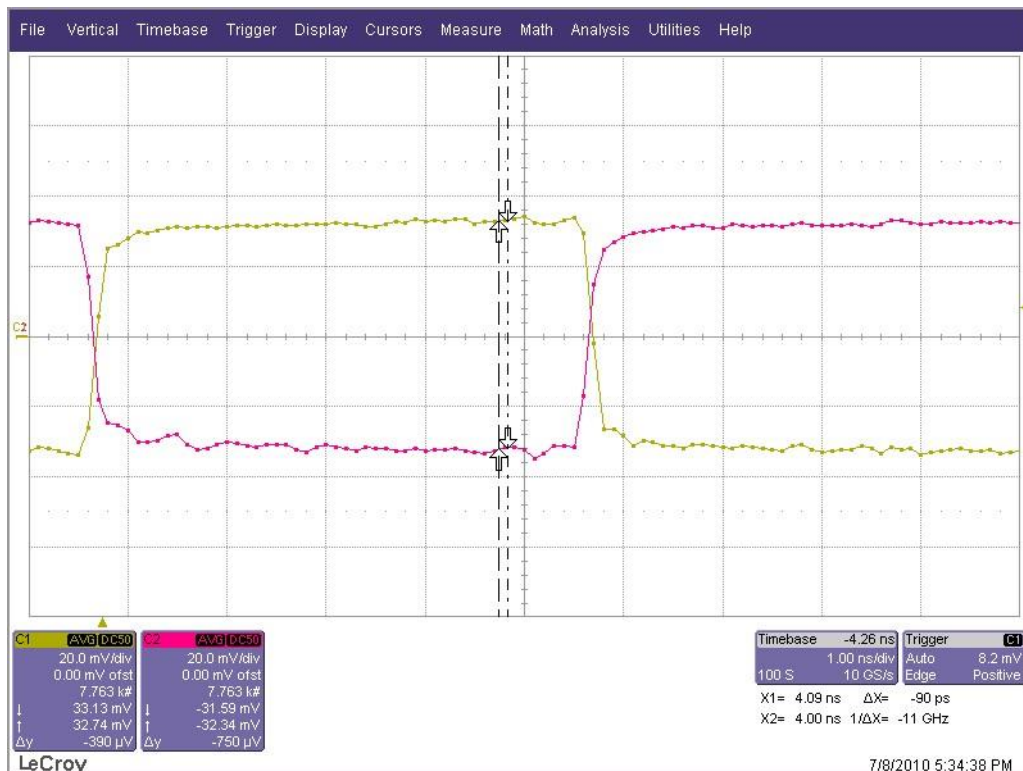


Figure 2.3. Differential Input Waveform for Hardware Test



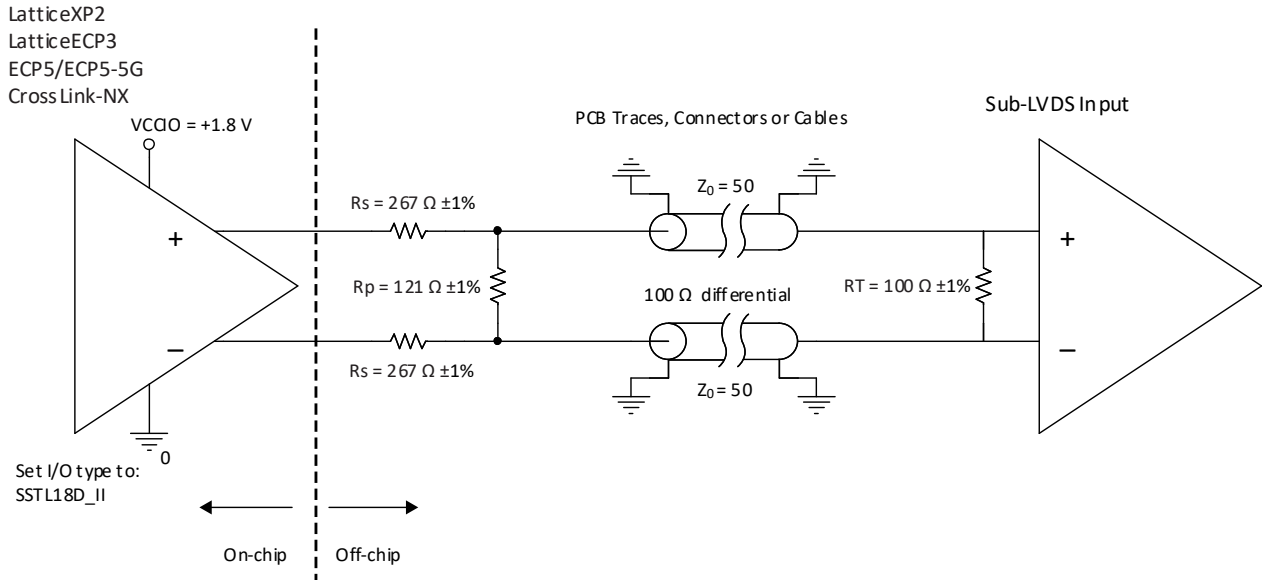
**Figure 2.4. Typical Differential Output Waveform from Hardware Test**

The LatticeECP3 and LatticeXP2 devices, when configured as an HSTL18D input, have the same input differential and common mode performance as the LVDS input type. You can also set the Lattice design software to use the HSTL18D input type to represent a sub-LVDS input. On the MachXO2, the HSTL18D inputs have different specification compared to the LVDS inputs. For the MachXO3L device, it would be the LVCMOS18D inputs that supports the sub-LVDS specifications. See [Table 2.1](#) for values and IO\_TYPES to be used for each of the devices.

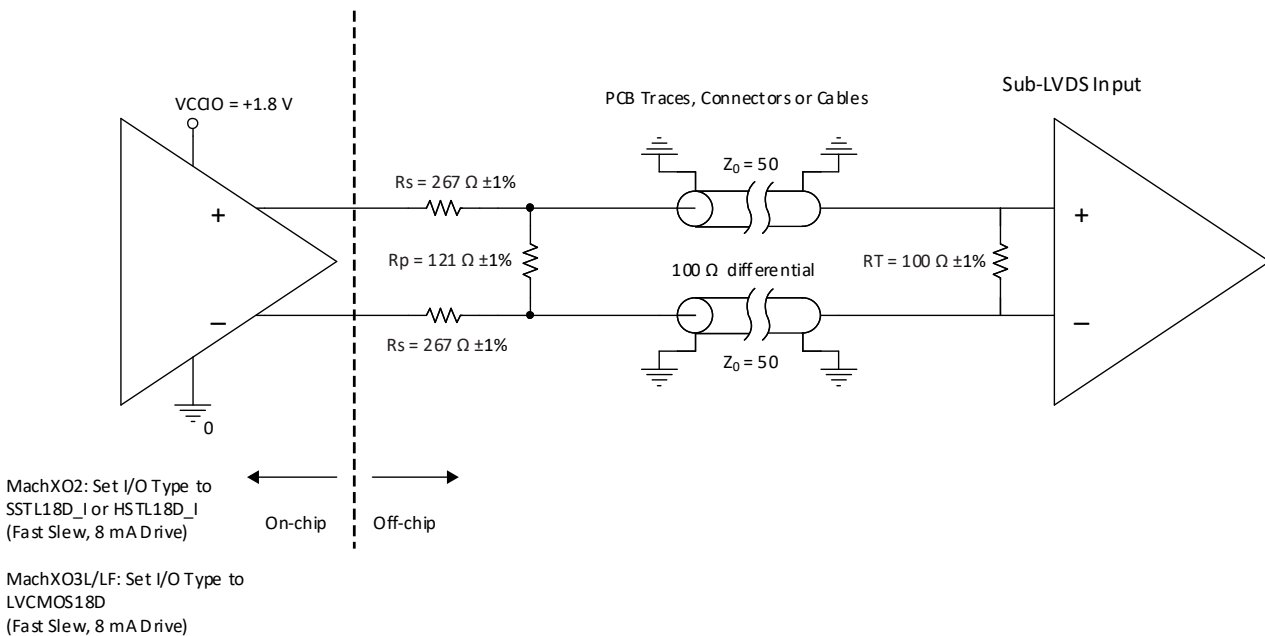
Sub-LVDS, like LVDS, requires 100 Ω termination at the receiver but does not specify that the termination is internal or external to the receiver. The CrossLink-NX and ECP5/ECP5-5G device have internal 100 Ω differential termination that the user can select. The LatticeECP3 device has built-in differential termination with selectable values of 80, 100, 120, or off. The internal differential 100 Ω terminations are only available for inputs on the left and right sides of the device. See [LatticeECP3 Family Data Sheet \(DS1021\)](#) for additional information about on-die termination. The MachXO2 and MachXO3L/LF devices support on-chip 100 Ω (nominal) input differential termination on the bottom edge of MachXO2-640U, MachXO2-1200/U, MachXO2-2000/U, MachXO2-4000, and MachXO2-7000 devices. The LatticeXP2 device has no internal input termination so it does require external 100 Ω differential input terminations. When an external termination is used, the resistor should be either 0402 body size or surface mount resistor packs and placed as close as possible to the input BGA balls on the device.

If you would like to generate sub-LVDS output signals using a LatticeECP3 and LatticeXP2 devices, it is recommended to set the I/O type to SSTL18D\_II, and add the resistor network shown in [Figure 2.5](#) to emulate a sub-LVDS output type.





**Figure 2.5. Lattice Device Generating a Sub-LVDS Signal Level – LatticeXP2, LatticeECP3, ECP5/ECP5-5G, and CrossLink-NX**



**Figure 2.6. Lattice Device Generating a Sub-LVDS Signal Level – MachXO2 and MachXO3L/LF**

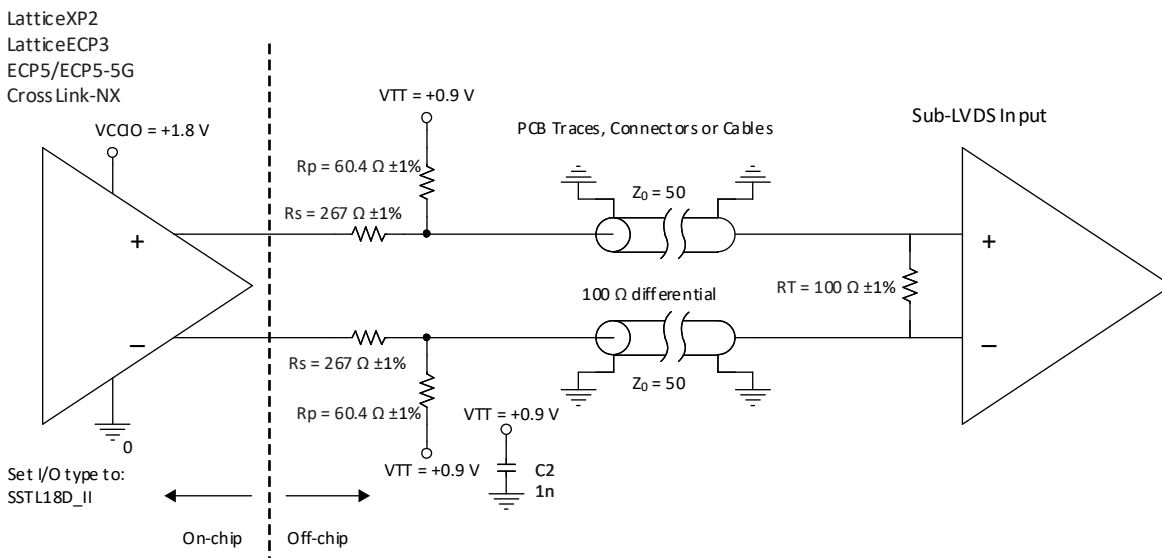
The resistor network shown in [Figure 2.5](#) and [Figure 2.6](#) will produce  $V_{od} = 156$  mV at the  $R_T$  termination. [Table 2.2](#) lists various resistor values that can be used to produce other output voltage levels smaller or larger than 156 mV, while maintaining a 100 Ω differential source termination.

**Table 2.2. Sub-LVDS Output Voltages for Rs and Rp 1% Resistor Values**

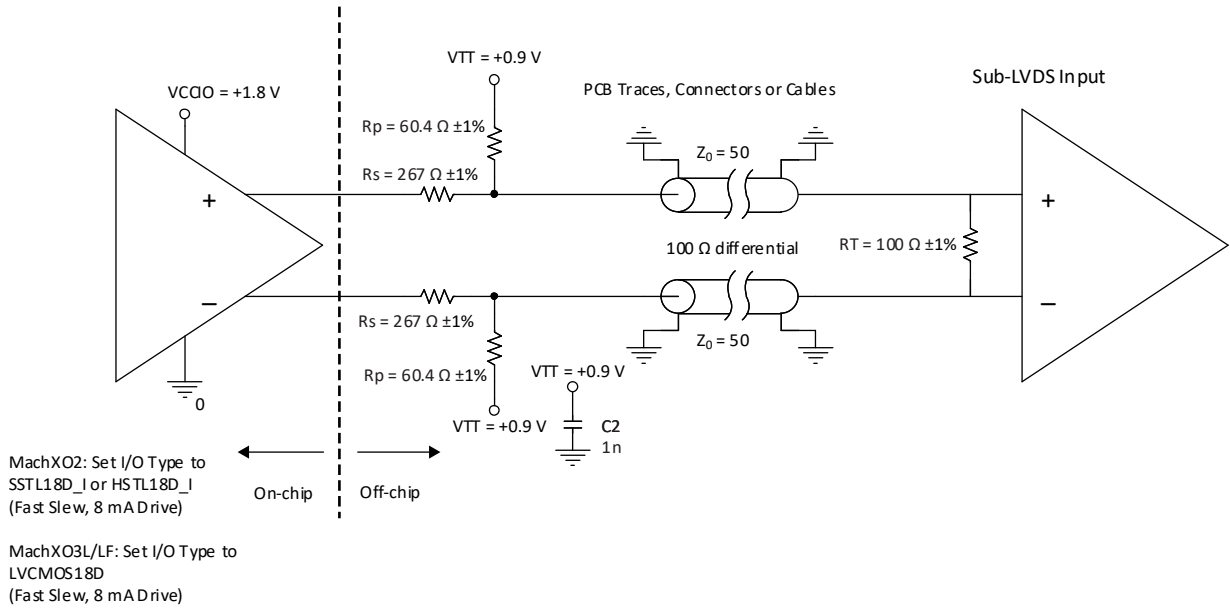
Vod (mV)	Rs (Ω)	Rp (Ω)
104	412	113
136	309	118
156	267	121
174	237	124
207	196	130

The Vcm value for the network shown in Figure 2.5 and Figure 2.6 is by default half the VCCIO voltage. The Rp and Rs resistors should be placed as close as possible to the Lattice device output pins and should be either 0402 body size or surface mount resistor packs with minimal stub length traces to the resistors.

If you need the lowest common mode output noise, you will get the best performance with the output resistor network shown in Figure 2.7 and Figure 2.8 where the original Rp resistor has been split into two resistors of value one-half Rp each with their center connection to a floating, or a 0.9 V VTT, plane island that is itself bypassed to the GND plane. The GND plane should cover the entire extent of the PCB with no major line or area breaks in the plane.



**Figure 2.7. Lattice Device Generating a Low Noise Sub-LVDS Signal – LatticeXP2, LatticeECP3, ECP5/ECP5-5G, and CrossLink-NX**



**Figure 2.8. Lattice Device Generating a Low Noise Sub-LVDS Signal – MachXO2 and MachXO3L/LF**

## Technical Support Assistance

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## Revision History

### Revision 1.7, December 2019

Section	Change Summary
All	<ul style="list-style-type: none"> <li>Changed document number from TN1210 to FPGA-TN-02028.</li> <li>Added support off CrossLink-NX device family.</li> <li>Updated document template.</li> <li>Updated document links.</li> </ul>
Technical Support Assistance	Updated this section.

### Revision 1.6, October 2015

Section	Change Summary
All	Product name adjustment. Included MachXO3LF device.

### Revision 1.5, November 2015

Section	Change Summary
All	Added support for ECP5-5G device family.

### Revision 1.4, June 2015

Section	Change Summary
All	Updated Differences Between LVDS and Sub-LVDS Signals section.
Differences between LVDS and Sub-LVDS Signals	Added MachXO3L/LF in Table 2.1. Sub-LVDS Output Signal Voltages and LVDS Input Specifications.

### Revision 1.3, January 2015

Section	Change Summary
All	Added support for MachXO3L device family.

### Revision 1.2, March 2014

Section	Change Summary
All	Added support for ECP5 device family.

### Revision 1.1, April 2013

Section	Change Summary
All	Added sub-LVDS implementation for MachXO2.

### Revision 1.0, July 2010

Section	Change Summary
All	Initial release.



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